High Speed and Gate at 22nm Metal Gate Strained Silicon Technology

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Abstract— This paper demonstrates a high speed AND gate at 22nm High K metal gate Strained Silicon making use of forward body biasing. The simulations are done with hspice simulator with 'HP ptm' models of Arizona State University, USA. Forward body biasing results in higher speed with shortened propagation time on an average and 'on an average' shortened rise time and fall time. There is deterioration of output voltage if static forward body biasing is beyond a limit. The output voltage levels can be at its best inspite of the forward body biasing with the use of different circuit configuration, which is a future scope of this research paper. Also the other side effects of forward body biasing can be overcome with new techniques The average decrease in rise time and fall time is 4 % and average decrease in propagation delay is 39 % for input low to output low and 13% for input high to output high.

Index Terms—22nm, High Speed AND gate, CMOS AND gate, Forward body biasing, Hi K metal Gate Strained Si, ptm models.

I. INTRODUCTION

There is constant evolution in the semiconductor industry due to evolution in the memory and microprocessor chips. Moore's law is still valid. There are challenges associated with smaller and smaller chip and circuit area or size with ever decreasing demand of supply voltage as the complexity to design increases. CMOS technology has come a long way from .28µ to 10nm and so on with a supply voltage of 1V to 0.8V. With scaling there is increase in:-

(1) Leakage current. (2)Reduction in intrinsic gain. (3)Increased cost of mask. (4) Increased problems of process variations as the transistors used are minimum size and any mismatch in the size results in failure of operation.(5) A big work is going on to accurately model the nano cmos transistors. The BSIM4 model has more than 350 parameters. Following Section tells the details on the circuit simulation result with HSPICE Simulator with Arizona State University, USA's high performance PTM models.

II. CIRCUIT SIMULATIONS AND RESULTS

Following AND circuit of Fig. 1 is simulated with temp 27^0 C with normal reverse body bias and forward body bias. The comparison Table is drawn to understand the impact of reverse body bias (a normal mode of operation) and forward body.

The transient analysis is done with load capacitance of 20ff in both the cases. The NMOS dimensions at 22nm technology mode are near to minimum and PMOS dimension are almost 5-6 times of that of NMOS dimensions. The Simulations are done with Hspice simulator with PTM HP models of 22nm High K metal Gate Strained Si Technology.

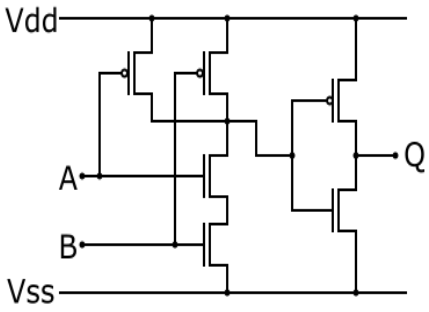

Fig. 1 The AND circuit used for both reverse Body bias and with Forward Body bias.

The following Table 1 helps us in analyzing the AND gate in two modes.

TABLE I
Comparison and output voltage, load cap and power of the AND gate's two configurations.

parameter	NOR With normal reverse body bias	NOR with Forward body bias
Supply voltage	1v	1v
Nsub bias voltage	1v	0.4988v
Psub bias voltage	0v	0.4998v
Ground voltage	0v	0v
Load cap	20ff	20ff
Avgpwr(W)	5.8292E-06	9.6901E-06
Peakpwr(W)	1.0719E-04	1.0606E-04
vmax_ input (v)	1.0000E+00	1.0000E+00
vmin_input(v)	0.0000E+00	0.0000E+00
vmax_out(v)	1.0001E+00	9.9362E-01
vmin_out(v)	5.6289E-04	1.1744E-02
trise_input(v)	0.4ns	0.4ns
tfall_input(v)	0.4ns	0.4ns
trise_output(v)	1.9569E-10	2.1783E-10
tfall_output(v)	3.2407E-10	2.9497E-10
tdelayinputlo_outputlo(v)	1.0885E-10	6.9672E-11
tdelayinputhi_outputhi sec	1.4236E-10	1.3305E-10

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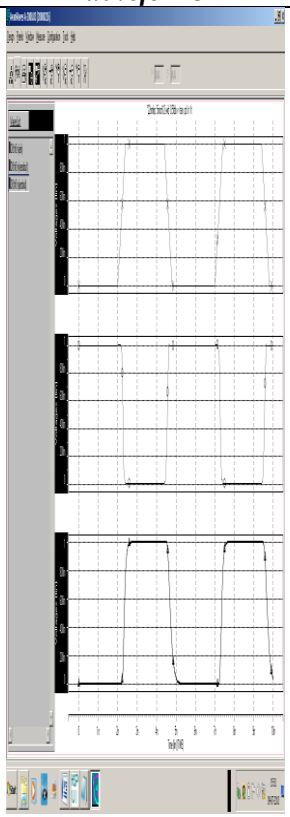
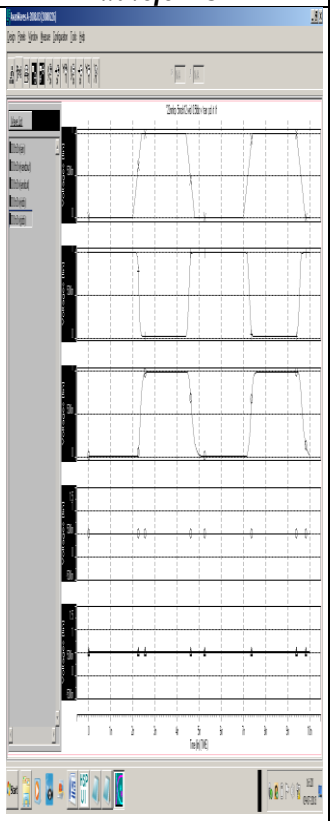
Table II below shows the input, output ,nsubBB,PsubBB and power waveforms of the AND gate under normal Reverse Body Bias condition and under Forward body bias conditions.

TABLE II

NOR With normal reverse body bias	*NOR with Forward body bias*
waveforms	***waveforms***
	
Vinput, voutput, nsubBB, psubBB, power	**Vinput, voutput, nsubBB , psubBB, power**

III. CONCLUSION

The results show that average decrease percentage of rise and fall time of the forward biased AND gate is approximately 4%. The input low to output low propagation delay is reduced by 39% approximately and propagation delay with input hi to output high is decreased by 13%. Also as expected the average power is increased in forward body biased AND gate with the reduction in peak power, as can be seen in the comparison table I and II both.

The future scope of the paper lies in researching a new circuit with Forward Body bias but with minimum area overhead to reduce the power dissipation.

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