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A Novel Domino Logic for Arithmetic Circuits

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Abstract*—This paper presents a low power and high speed ripple carry adder circuit design using a new CMOS domino logic family called feedthrough logic. Dynamic logic circuits are important as it provides better speed and has lesser transistor requirement when compared to static CMOS logic circuits. The proposed circuit has very low dynamic power consumption and lesser delay compared to the recently proposed circuit techniques for the dynamic logic styles. Problems associated with domino logic like limitation of non-inverting only logic, charge sharing and the need of output inverter are eliminated. The feedthrough logic (FTL) performs a partial evaluation in a computational block before its input signals reach a valid level, and performs a quick final evaluation as soon as the inputs arrive, leading to a reduction in the delay. The FTL is well suited to arithmetic circuits where the critical path consists of a large number of gates. A comparison has been done by simulating the proposed logic style based 10-bit ripple carry adder along with previous logic styles based RCAs. The results show that FTL is the simplest, fastest and consumes least power.

***Index Terms*—Domino logic, Dynamic CMOS logic, Feedthrough logic (FTL), Low power ripple carry adder (RCA)**

I. INTRODUCTION

Though the static CMOS logic offers less speed, it is best known for its lowest power dissipation. As the number of inputs increase, the number of transistors required will be doubled. In order to reduce the transistor count, pseudo NMOS is preferred, whereby area is also reduced. But it fails to improve speed and reduce power dissipation. The nominal low output voltage for Pseudo NMOS is not 0V since, there is a fight between the devices in the pull down network and the grounded PMOS load device. This results in reduced noise margins and more importantly static power dissipation [1].

Dynamic logic is well suited for high speed circuit design and requires less number of transistors to implement a given logic, but the major drawback with this logic is, its excessive power dissipation due to the switching activity and clock. Excessive power dissipation of dynamic logic circuit is reduced with a mix of dynamic and static circuit styles [2], use of dual supply voltages [3] and dual threshold voltage (VT) [4] that have been proposed. Circuits having long logic depth need to have better speed and low power dissipation for which a new logic family called feedthrough logic (FTL) is proposed in [5]. Here FTL concept is extended for the design of low power arithmetic circuits.

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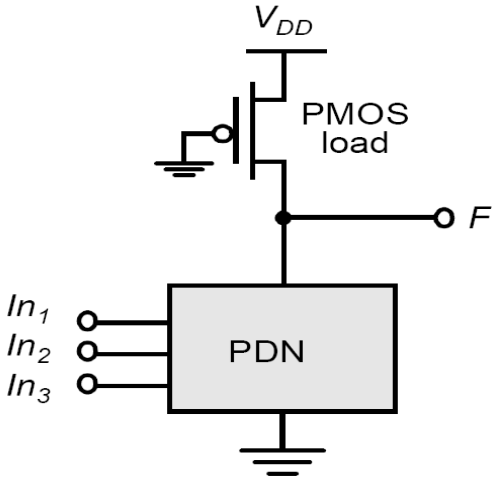

Fig.1. Pseudo NMOS gate

The total power dissipated in a generic digital CMOS gate is given by

$$P_{total} = P_{static} + P_{dynamic} + P_{short\ circuit}$$

$$P_{Total} = V_{dd} I_l + V_{dd} F_{clk} \sum_i V_{i\ swing}\, C_{i\ load} \alpha_i + V_{dd} \sum_i I_{i\ sc}$$

Where F_{clk} denotes the system clock frequency, $V_{i\ swing}$ is the voltage swing at node i, $C_{i\ load}$ is the load capacitance at node i, α_i the activity factor at node i, $I_{i\ sc}$ is the short circuit current and I_l is the leakage current.

The rest of the sections are organized as follows: Section II describes the principle of operation of conventional FTL, referred as HS0 in [5]; Section III presents the description of proposed HS0 in [6], referred as LP0; Section IV presents the proposed modified FTL structure; Section V presents the performance analysis of various inverter logics with respect to power and delay, performance analysis of 10 stage inverter chains, a 10-bit RCA described by various conventional FTL logic styles and the proposed modified FTL. Conclusions are given in section VI.

II. HS0 PRINCIPLE OF OPERATION

The basic structure of conventional FTL, High Speed structure (HS0) is shown in Fig.2. It consists of a PMOS transistor(M1) in pull up network controlled by the clock signal(CLK); a reset transistor NMOS(M2) controlled by clock signal which pulls output to ground, if clock(CLK) is asserted. Here input (IN) is asserted to a NMOS transistor (M3). Its operation is described here.

During CLK =1 (reset phase), the output node (OUT) is pulled to ground via M2. When CLK =0 (evaluation phase), M2 is turned off and M1 conducts. The output node is conditionally evaluated to either logic *high* or *low* level depending upon input (IN) to M3. If the IN=0, the output node is pulled towards V_{DD}, otherwise it stays at logic *low*.

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This logic is faster because the output makes transition from V_{TH} to V_{OH} or V_{OL} only [5], but it suffers from more power consumption due to the fact that V_{OL} is not 0 V. This is because M1 is always ON.

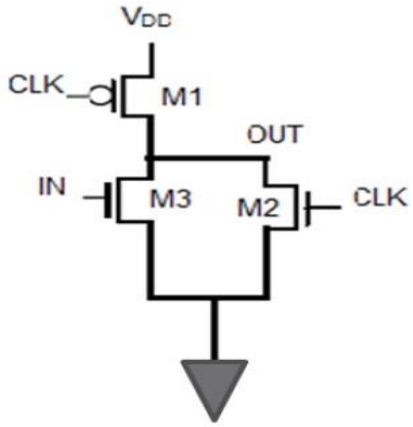

Fig.2. HS0 structure for inverter [5]

III. LP0 CIRCUIT DESCRIPTION

Another form of FTL, known as LP0 (Low Power structure) was proposed in [6] has one more additional PMOS transistor (M4) in series with M1, which is also controlled by CLK. It is shown in Fig.4. As two PMOS transistors are in series, it further reduces leakage through M1 transistor and hence it helps in reducing V_{OL} as compared to HS0 [5].This reduction in V_{OL} helps in reducing dynamic power dissipation. During reset phase the LP0 circuit operation is same as that of HS0 [5].

IV. PROPOSED MODIFIED FTL STRUCTURE

The proposed modified circuit is shown in Fig.4. It consists of same pull-up network as that of LP0 in [6]. In order to improve the speed, one or more additional NMOS transistors in the reset block are connected in series with M2. Controlling inputs to the gate terminals of these NMOS transistors are the inputs which have the important role in making the output to 0 V during evaluation phase.

During reset phase (when CLK=1), depending upon inputs (IN), the parallel NMOS transistors in the reset block pulls output node (OUT) to ground or leave it remains unchanged. During evaluation phase (when CLK=0) according to inputs to the NMOS block OUT node is evaluated to V_{OH} or V_{OL}.

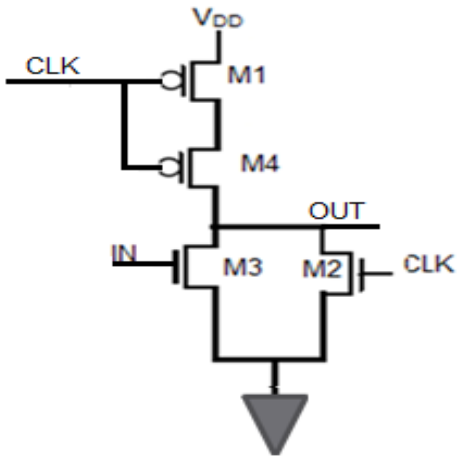

Fig.3. LP0 structure for inverter [6]

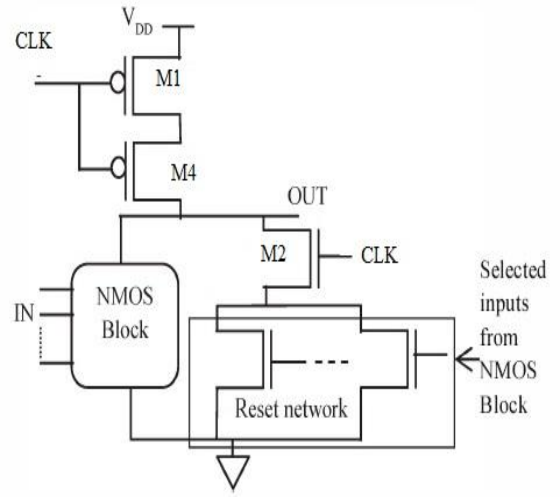

Fig.4. Proposed modified FTL for low power and high speed

V. PERFORMANCE ANALYSIS OF PROPOSED STRUCTURE

A. *Design of long chain of inverter*

A long chain of inverter (10-stages) designed by using the proposed structure in Fig.5 is compared with various logics such as static CMOS, pseudo NMOS and conventional FTL structures (HS0, LP0) in [5, 6]. The circuit is simulated using 180nm CMOS process technology. Power supply V_{DD} is 1.8V for all simulation. Circuits are drawn using Tanner S-edit. Net list obtained from T-spice for the schematic circuit are used with 180nm technology model files to simulate on HSPICE simulator.

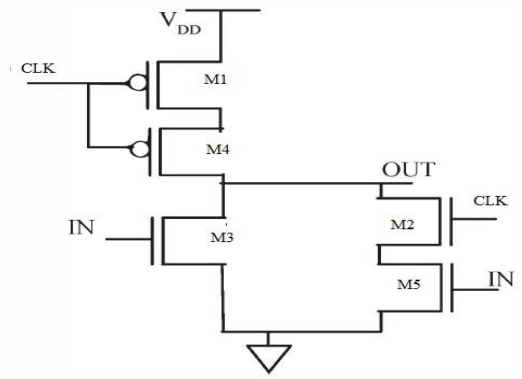

Fig.5. Inverter circuit using proposed structure

TABLE I simulation results for proposed modified structure (10-inverter chain)

Logic style	$P_{avg}(\mu W)$	$t_p(ns)$	PDP(µW*ns)
Static CMOS	42.84	0.223	9.57
Pseudo NMOS	3394.2	0.140	477.66
HS0 in [5]	1583	0.135	214.33
LP0 in [6]	911.48	0.195	178.22
Proposed MFTL	910.25	0.149	136.30

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Table I shows the average dynamic power dissipation and propagation delay comparison among the various logic styles with the proposed modified structure of FTL for a chain of 10 inverter stages at 10fF capacitive load and 50MHz clock frequency.

For a given technology and gate topology, the product of power consumption and propagation delay is generally a constant. This product is called the power delay product (or PDP) and can be considered as a quality measure for a switching device. It can be seen that though static CMOS exhibits low power dissipation, it is comparatively slower than other logics. Apart from Static CMOS, the results show that the proposed structure reduces the delay besides reduction in the average power consumption.

B. Design of 10-bit RCA

The sum and carry cell structure used for the design of 10-bit RCA is shown in Fig.6 (a, b). These basic cells are designed by the proposed modified FTL structure. The reset block for sum cell is shown in Fig.6(a), consists of two parallel NMOS transistors whose gates are controlled by *ci*(carry in) and *cob* (carry out-active low).This is because these two are the effective inputs in making output node *sumb* to *high* or *low*. The reset block for carry cell is controlled by *ci* and *a*.

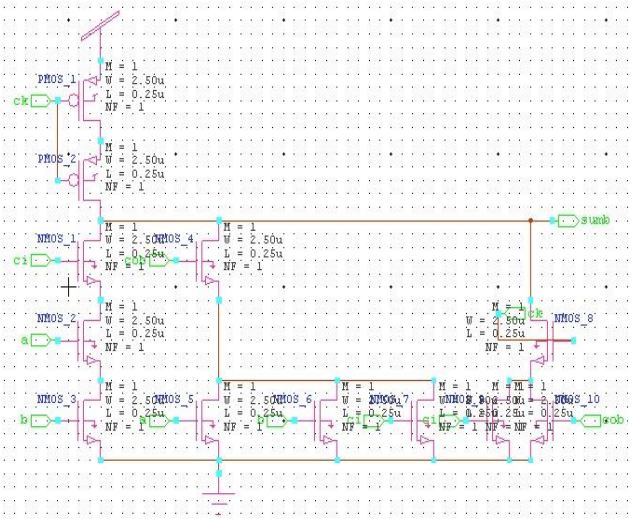

Fig.6 (a) sum cell structure using modified FTL

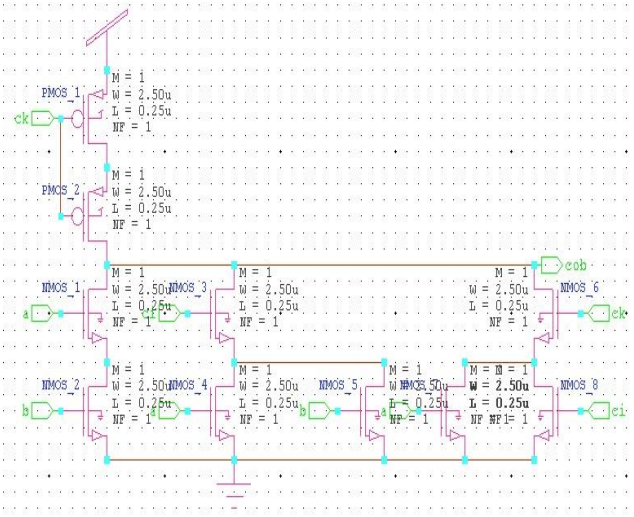

Fig.6(b) carry cell structure using modified FTL

TABLE II SIMULATION RESULTS FOR 10-BIT RIPPLE CARRY ADDER

Logic style	$P_{avg}(mW)$	$t_p(ns)$
LP0 in [6]	2.32	1.910
Proposed MFTL	1.73	1.004

A 1-bit full adder cell using modified FTL structure is created and is used to construct a 10-bit RCA. The 10-bit RCA is designed with VDD equa lto 1.8V at 180nm technology. The power and delay comparison at 10fF capacitive load at the output of sum and carry cell at 50MHz clock is shown in table II. Simulation results for 10-bit ripple carry adder using modified FTL structure is shown in Fig.8, where input signals are not shown.

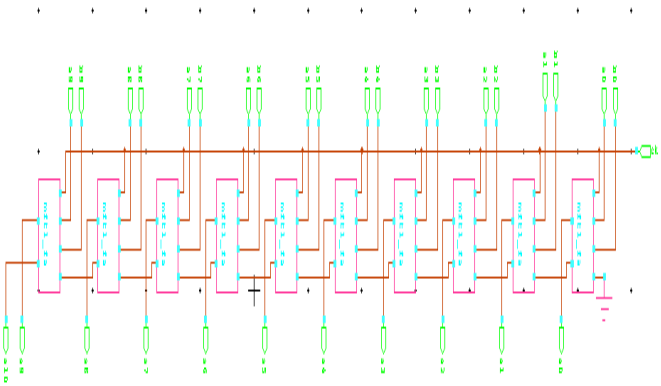

Fig.7. 10-bit RCA using modified FTL

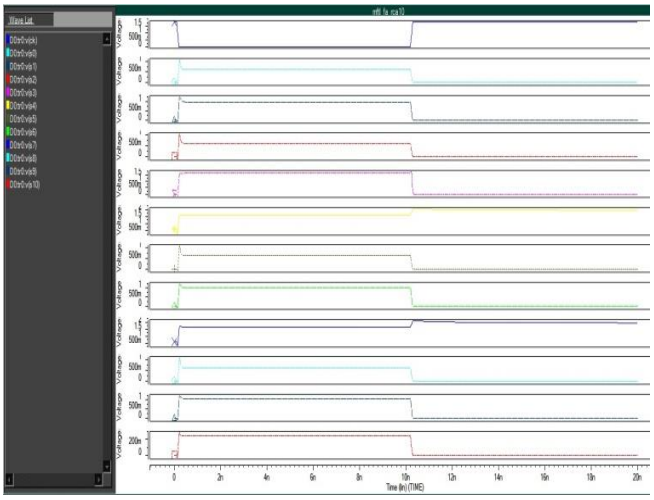

Fig.8. Simulation results for 10-bit RCA using modified FTL (input signals are not shown)

VI. CONCLUSION

In this paper, we proposed a low power and high speed ripple carry adder design using a new domino logic style, known as modified FTL structure. From the simulation result, we can conclude that the power delay product is improved by 60.80% as shown in Fig.9 compared to LP0 in [6].

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It emphasises that the proposed strucure further reduces power dissipation besides delay compared to that of HS0 in [5]. Though it improves the performance of a circuit, it is achieved at the cost of increased number of NMOS transistors in reset block.

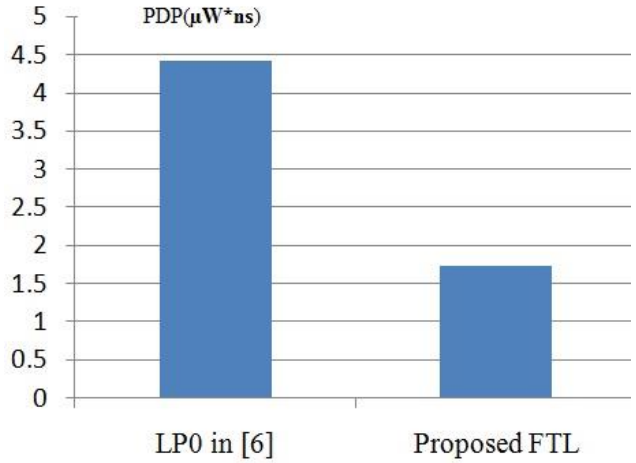

Fig.9. Power delay product Vs logic styles for 10-bit RCA

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