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Strained Silicon High-K Metal Gate 22nm CMOS High Speed OR Gate

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Abstract—This paper demonstrates a high speed OR gate in CMOS technology with strained Silicon Metal gate 22nm technology node. The CMOS circuit uses forward body bias instead of reverse body bias which results in high speed .The excessive increase in forward body bias results in ouput level degradation. The simulations are done with HSPICE simulator with Arizona state University's (USA) 'HP ptm ' model of level54. The average decrease in rise and fall time of output voltage is approximately 6% and decrease in propagation delay is 47 % in the forward body biased OR cmos gate. The present circuit can further be modified to preserve the output levels to their maximum levels inspite of very high Forward body bias in order to have higher speed, and this is the future scope of this paper.

Index Terms—22nm, High Speed AND gate, CMOS AND gate, Forward body biasing, Hi K metal Gate Strained Si, ptm models.

I. INTRODUCTION

With scaling, the heterogeneous components continue to be on a single chip. Analog, Digital and mixed signal devices continues to be on a single die for optimum cost and optimum performance.1 2 3

The complexity of the system made out of nano cmos/other technology transistors have increased up to gigascale measures. There are huge complex systems and 'product-time' requirement is further reduced along with highly complex specifications. The whole scenario is complex as the market is overcrowded.

There are tools which are only for analog, or only for digital or with hardware –software design. 456

The main focus remains as an issue that how quickly, the design be done and layout generation can be done.

This paper presents the high speed OR gate where substrate biasing is utilized to achieve the high speed but at the cost of higher power consumption. Hence this circuit is useful where speed is the first priority. The continued increase in forward body bias results in lower output levels of the voltage and hence a limitation. The deterioration is in the lower level of the output voltage as well if the forward body bias is too much.

II. CIRCUIT SETUP AND SIMULATIONS

Following circuit of CMOS OR gate is used with 20fF of load at the output

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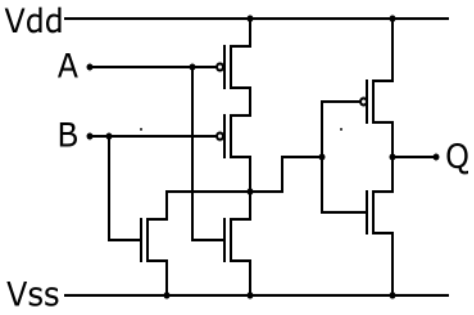

Fig.1 CMOS OR gate circuit with 20fF load at output Q

With normal Reverse body bias configuration and forward body bias.

The following Table I is showing the comparison between normal reversed body biased CMOS OR gate and Forward body biased CMOS OR gate with all other parameters and factors remaining the same.

Table 1.

The size of nmos is near to minimum and that of pmos is almost 5-6 times that of pmos. CL is 20fF.

Parameters of two CMOS OR gate configurations with normal reversed body bias and forward body bias.

TABLE1

parameter	reverse body bias	Forward body bias
Supply voltage Volts	1	1
Nsub bias voltage	1v	0.48999V
Psub bias voltage	0v	0.48989V
Ground voltage	0v	0v
Avgpwr (W)	5.6223E-06	9.4157E-06
Peakpwr(W)	1.0741E-04	1.3741E-04
vmax_ input (v)	1V	1V
vmin_input(v)	0V	0V
vmax_out(v)	1V	9.9403E-01
vmin_out(v)	5.6570E-04	1.2371E-02
trise_input(v)	0.4V	0.4V
tfall_input(v)	0.4V	0.4V
trise_output(v)	1.7349E-10	1.7238E-10
tfall_output(v)	3.2600E-10	2.9114E-10
tdelayinputhi_outputhi(v)	3.9768E-10	5.0372E-11
tdelayinputlo_outputlo	1.9480E-10	1.7988E-10

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Table II
OR gate normal reversed biased configuration

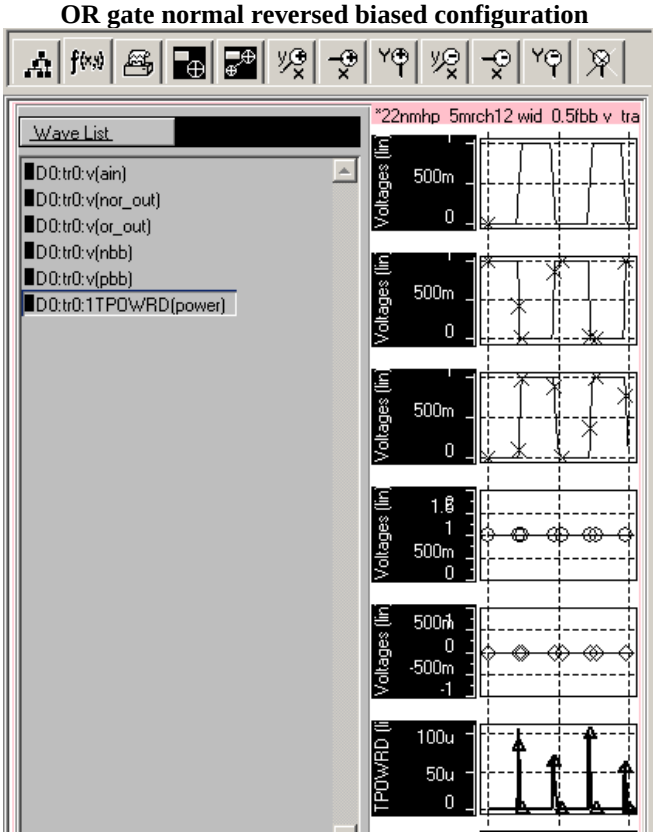

TABLE III
OR gate with forward body biased configuration

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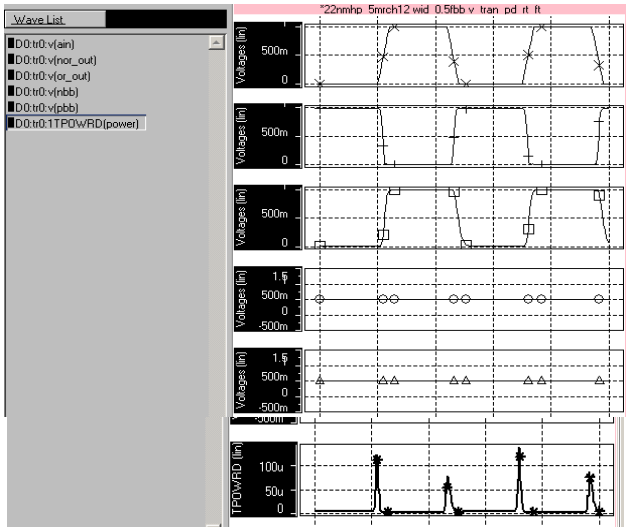

III. CONCLUSION

An average decrease of output rise and fall time approximately 6% and hence adding to higher speed. The average decrease in propagation delay for high and low input-output is approximately 47% but at the cost of slight increase in power. Reduction of this increased power due to forward body biasing is the future scope of this research paper.

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