A New topology of Single-Phase Seven-Level Inverter with Less Number of Power Elements for Grid Connection

G.Gopal, B.Shankaraiah, M.Chinnalal, K.Lakshmi Ganesh, G.Satyanarayana, D.Sreenivasa Naik

Abstract— recently, the evolution of single phase multilevel inverters has been escalation due to its preference over traditional one. In this paper proposed a new topology of single phase seven level inverter with less number of power elements for grid connection. In this proposed inverter have eight switches and their switches operate with fundamental frequency. The proposed inverter produced seven level output voltage from two input voltage sources. The proposed inverter reduced the switching losses (because of all switches operate with fundamental frequency), complexity, control circuit and place requirement. The proposed inverter compared to a single-phase five level pulse width modulation (PWM) inverter for grid connection. The proposed inverter compared to conventional inverter has PWM technique have two triangular carrier signals identical to each other with an offset equivalent to the amplitude of the reference signal were used to generate PWM signals for the switches. The proposed inverter compared to conventional inverter has some switches operate at fundamental frequency and other operates at switching frequency.

Index Terms—Multilevel inverters, Grid connection, Pulse generation, PWM.

I. INTRODUCTION

Multilevel inverters (MLI) started with the neutral point clamped inverter topology proposed by Nabae et al. [1]. Presently multilevel inverters have become more attractive for researchers due to their advantages over conventional three-level Pulse width-modulated (PWM) inverters. MLI has two main advantages compared with the conventional H-bridge inverters [2]-[4], the higher voltage capability and the reduced harmonic content in the output waveform due to the multiple dc levels. MLI is now preferred in high power medium voltage applications due to the reduced voltage stresses on the devices. MLI incorporates a topological structure that allows a desired output voltage to be synthesized among a set of isolated or interconnected distinct the voltage sources.

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Numerous topologies realize this connectivity and can be generally divided into three major categories namely, diode clamped MLI, flying capacitor MLI and separated dc sources (cascaded voltages) MLI [5].

Recently nonconventional energy sources for grid connected applications are increased due to the world energy crisis. Injecting power to the utility must meet the world harmonic standards. Therefore, single phase MLIs become a good solution for most particular demerits of MLI is the large number of the required power semiconductor switches. Although low voltage rate switches can be utilized in a multilevel inverter, each switch requires a related gate drive circuit. This may be problem occurs, the overall system to be more expensive and complex. So, in practical implementation, decreasing the number of switches and gate driver circuits have become an essential point.

Recently, so many topologies of the MLI and its control techniques have been published. The MLI technique is implemented in [8] by adding one switch and four power diodes to the H-bridge single phase inverter. Another solution can be found in [9] by using two switches and two power diodes with the H-bridge single phase inverter. Those two systems can generate only five levels in the output voltage with less harmonic contents. The other solution, shown in [10], is a modular inverter that can each to any required voltage levels. But these inverters topologies can be improved by reducing their switches without affecting their performances.

This paper presents a conventional inverter single-phase five-level PWM inverter with less number of power elements and hence less gate drive circuits in addition to less circuit layout complexity. Its output voltage has the following five levels: zero, $+V_{dc}$, $+0.5V_{dc}$, $-0.5V_{dc}$ and $-V_{dc}$. As the number of output levels increases the harmonic content can be reduced. This inverter topology uses two carrier signals to generate PWM signals for the switches. Some switches operate at fundamental frequency and others operate at switching frequency. Sections II and III explain the principle of operation and PWM strategy for the proposed inverter respectively. The switching algorithm that used in PWM is presented in section IV.

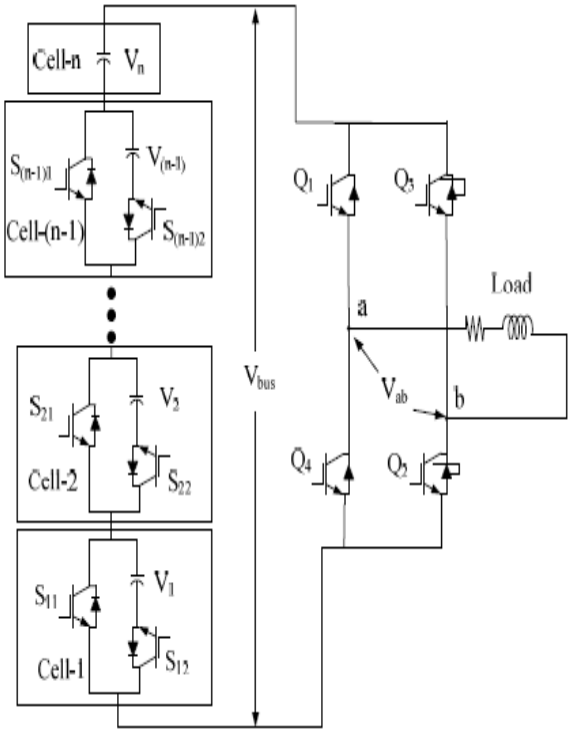
In this paper proposed a new topology of single phase seven level inverter with less number of power elements for grid connection.

The proposed inverter produced seven level output voltage from two input voltage sources. The seven level output voltages produces are zero, $+1.5V_{dc}$, $+V_{dc}$, $+0.5V_{dc}$, $-0.5V_{dc}$, $-V_{dc}$ and $-1.5V_{dc}$. In this proposed inverter have eight switches and their switches operate with fundamental frequency compared to the seven level produced by 12 switches in cascaded H-bridge configuration.

The proposed inverter reduced the switching losses (because of all switches operate with fundamental frequency), complexity, control circuit and place requirement. The THD analysis is as shown in MATLAB/Simulink.

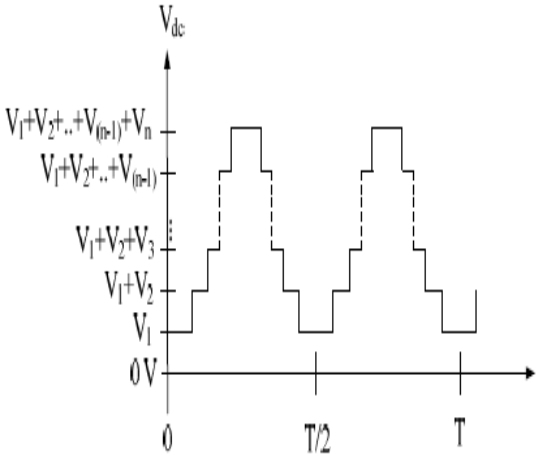
II. OPERATIONAL PRINCIPLES OF THE CONVENTIONAL INVERTER

Figure 1 shows the conventional structure single phase MLI inverter. It consists of 'n' cells of switch circuits. For cells from '1' to (n-1), each k-cell is composed of one dc voltage source and two switches (S_{k1},S_{k2}); one switch (S_{k2}) is connected in series with a dc voltage source and the other switch (S_{k1}) is connected in parallel with both the dc voltage source and the series switch. Based on this configuration, each cell can generate two states (0V) and the dc voltage source associated with the considered cell. Cell 'n' is composed of only the dc source voltage resulting in generating only one state (V_n). As a result, the dc link voltage V_{bus} has (n-1) states, they are (V1, V2…., V_n), as shown in Fig.2.



Figrue.1 Structure of the conventional cascaded dc link MLI

The above figure shows Structure of the conventional cascaded dc link MLI



Figrue.2 Typical output waveform of Vdc

The above figure shows typical output waveforms of V_{dc} It can be noted that the dc link voltage has no zero state voltage (0v) which needs extra two main switches. The H-bridge inverter composes of four switches (Q_1, Q_2, Q_3 and Q_4). The H-bridge inverter has two functions; it has to synthesis the inversion voltage of the dc link voltage in addition to generating the zero state voltage (0v) at the output voltage (V_{ab}) by connecting the upper two switches (Q_1, Q_3) or the lower switches (Q_2, Q_4). Obviously, this structure can reduce the number of switches compared to the conventional topologies without affecting the inverter performances. This is due to that; the zero voltage can be generated using the idea of the upper or lower H-bridge inverter to generate this state.

The pulse width modulation (PWM) control algorithm can be applied also for this topology. The PWM control algorithm, which adopted in this paper, consists of one modulation signal with amplitude (A_r) an n (number of dc link cell) carriers with same amplitude (Ac) from the former one. The amplitude (A_r) can be changed from 0 to n*Ac according to changing modulation index from 0 to 1.

III. SINGLE-PHASE FIVE –LEVEL PWM INVERTER

In order to generate five levels, the number of the required cascaded cell is n-2. One cell uses two switches with the dc source while the other cell is only the dc source as shown in Fig.3. Assume that the dc voltage sources are equal; $V_1=V_2=V_{dc}$. The dc link bus voltage V_{bus} will have two states, V_{dc} or $2V_{dc}$ and the load output voltage will have five states $0.5V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-0.5V_{dc}$. The zero state can be generated either by switching the upper switches together or the lower switches together. The other four states can be generated from the dc bus voltage V_{bus} based on folded cascade unit operation.

The operation of the single-phase five-level inverter, employing PWM, can be divided into 10 switching states based on the direction of the output current as given by table 1. The signal generation waveforms are generated using one modulating signal and two carriers. The amplitude of the modulating signal is (A_r) and the amplitude of each carrier is (A_c). In addition, each carrier is shifted with the carrier amplitude (A_c) from the former one, as shown in Fig.4.

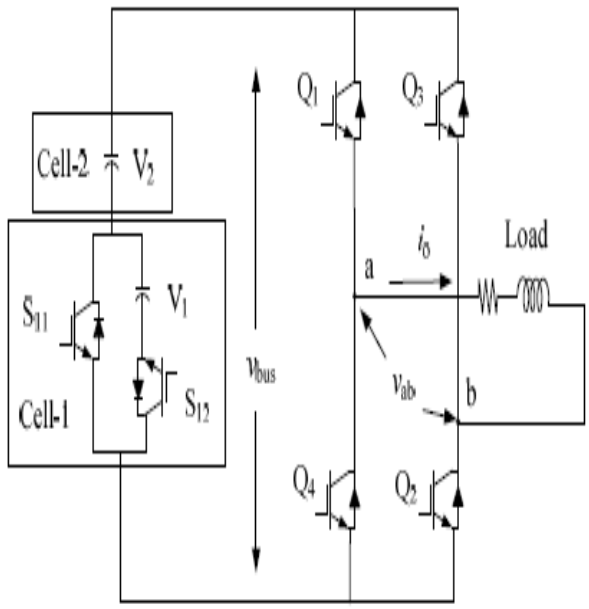


Figure.3 Conventional single-phase Five-level inverter configuration

The above figure shows conventional single-phase five-level inverter diagram.

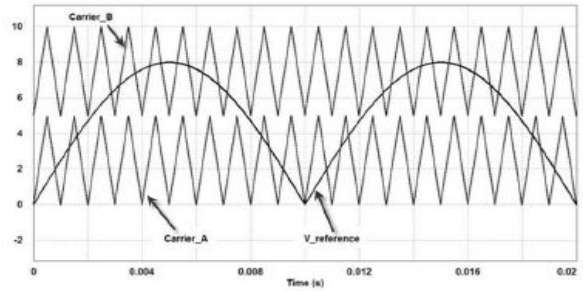


Figure.4 PWM switching strategy

The above figure shows PWM strategy for conventional inverter

TABLE I. OPERATIONAL STATES ACCORDING TO THE SWITCH ON CONDITIONS AND THE DIRECTION OF THE LOAD CURRENT

Switching states	The output voltage (V_{ab})	The Direction of the output current (i_0)	ON states Switches
1	V_{dc}	positive	Q_1, Q_2 and S_{11}
2	V_{dc}	negative	D_1, D_2 and S_{11}
3	$2V_{dc}$	positive	Q_1, Q_2 and S_{12}
4	$2V_{dc}$	negative	D_1, D_2 and S_{12}
5	0	positive	Q_1, D3 or Q_2,D_4
6	0	negative	D_1, Q_3 or D_2,Q_4
7	$-2V_{dc}$	positive	D_3, D_4 and S_{12}
8	$-2V_{dc}$	negative	Q_3, Q_4 and S_{12}
9	$-V_{dc}$	positive	D_3, D_4 and S_{11}
10	$-V_{dc}$	negative	Q_3, Q_4 and S_{11}

IV. SWITCHING ALGORITHM FOR THE CONVENTIONAL INVERTER USING PWM

The Switching patterns employed in the conventional inverter are illustrated in fig.5.The output Voltage levels, according to the switch ON/OFF conditions, are shown in Table II. The switching strategy used to generate the gate signals is accomplished by comparing the reference signal, which is rectified sinusoidal, with two triangular carrier wave forms having the same frequency and phase angle, but with different offset voltages. When the lower carrier signal is compared with the reference signal, the first level of output voltage will be generated. This means that the modulation index (MI) is less than pre equal 0.5 (50%). The behavior of conventional inverter is similar to the full-bridge three levels PWM inverter. The distribution of the harmonic components in output voltage is similar to that of the conventional inverter having the values of two times the modulation index. The mentioned above is the first operational mode. On the other hand, if the required output voltage is increased beyond the modulation index 0.5, the output will result from comparing the upper carrier signal with the same reference signal. Therefore, the second level of the output voltage will be generated and it will be the second mode. According to the amplitude of the voltage reference, the operational interval of each mode varies within a certain period.

Thee modes are determined as the phase angle depends on the modulation index.

Mode A: $0 < wt < \theta_1$, $\theta_2 < wt < \pi$
Mode B: $\theta_1 < wt < \theta_2$
Mode C: $\pi < wt < \theta_2$, $\theta_4 < wt < 2\pi$
Mode D: $\theta_3 < wt < \theta_4$ (1)

The modulation index MI of the conventional five levels PWM inverter is defined as follows [11]:

$$MI = \frac{A_M}{2A_C} \quad (2)$$

Where:

A_M The peak value of the modulating (sinusoidal) signal, i.e. the voltage reference (V_{ref}).

A_C The peak-to-peak value of the carrier (triangular).

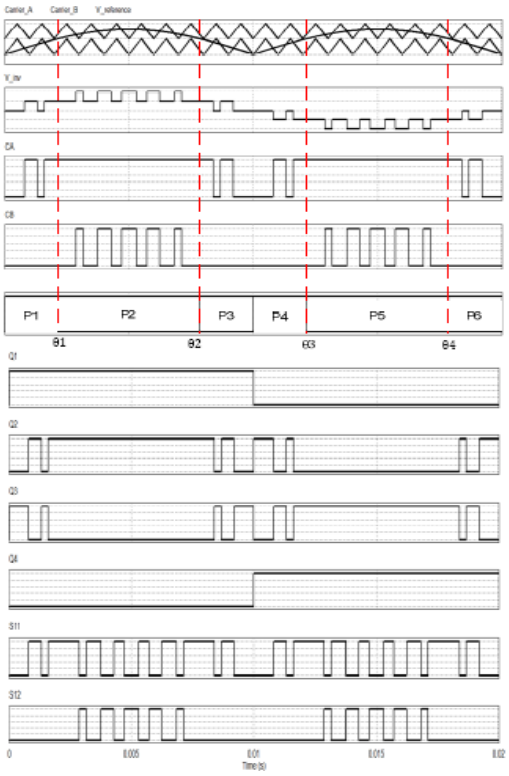


Figure.5 Switching Patterns of the proposed inverter

The above figure show switching pattern of the proposed inverter for conventional inverter

Also, the frequency ratio, m_f is defined as follows:

$$m_f = \frac{f_c}{f_m} \qquad (3)$$

Where:

f_c The frequency of the carrier (triangular) signal.

f_m The frequency of the modulating (sinusoidal) signal.

TABLE II. OUTPUT VOLTAGE ACCORDING TO THE SWITCH ON/OFF CONDITIONS

V_{ab}	Switching states					
	Q_1	Q_2	Q_3	Q_4	S_{11}	S_{12}
$+V_{dc}$	ON	ON	OFF	OFF	OFF	ON
$+0.5\ V_{dc}$	ON	ON	OFF	OFF	ON	OFF
0	ON	OFF	ON	OFF	OFF	OFF
0	OFF	ON	OFF	ON	OFF	ON
$-0.5\ V_{dc}$	OFF	OFF	ON	ON	ON	OF
$-V_{dc}$	OFF	OFF	ON	ON	OFF	ON

V. PROPOSED INVERTER

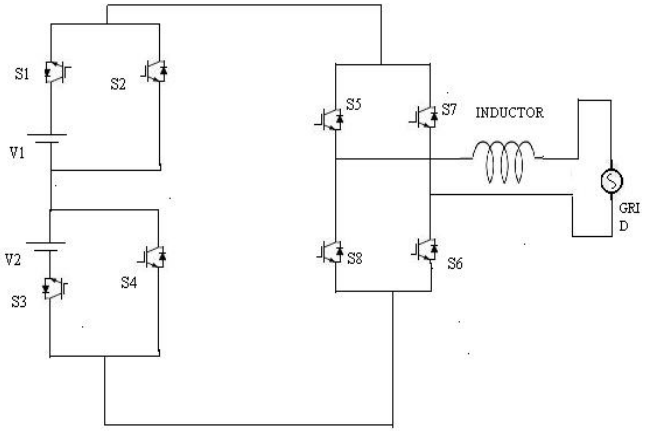


Figure.6 proposed inverter of a new topology of single-phase seven-level inverter with less number of power elements for grid connection

The above figure shows that multilevel inverter is a new topology of a single-phase seven level inverter with less number of power elements for grid connection. The seven level output voltage produced by the above inverter. This topology of an inverter has eight switches and two sources and grid connection. This inverter output voltage is connected to the grid. In the cascaded H-bridge configuration, seven level output voltage produced by using 12 switches. But in this new topology, seven level output voltage produced by using 8 switches. The seven level output voltage switching strategy as shown in the below table III.

TABLE III THE 7 LEVEL OUTPUT VOLTAGE SWITCHING STATES

Output voltage levels	Switching states							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
+1.5Vdc	ON	OFF	ON	OFF	ON	ON	OFF	OFF
+Vdc	OFF	ON	ON	OFF	ON	ON	OFF	OFF
+0.5Vdc	ON	OFF	OFF	ON	ON	ON	OFF	OFF
0	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
-0.5Vdc	ON	OFF	OFF	ON	OFF	OFF	ON	ON
-Vdc	OFF	ON	ON	OFF	OFF	OFF	ON	ON
-1.5Vdc	ON	OFF	ON	OFF	OFF	OFF	ON	ON

The switching sequence of seven level output voltage produced in the proposed inverter explain below.

1. The $+1.5V_{dc}$ output voltage produced by using the switches are S_3, S_5 and S_6 are ON position in the proposed inverter.
2. The $+V_{dc}$ output voltage produced by using the switches are S_3, S_2 and S_5 are ON position in the proposed inverter.
3. The $+0.5V_{dc}$ output voltage produced by using the switches are S_1,S_4, S_5 and S_6 are ON position in the proposed inverter.
4. The 0 Volts voltage produced by using switches are S_5, S7 are ON position in the proposed inverter.
5. The $-0.5V_{dc}$ output voltage produced by using the switches are S_1,S_4, S_7 and S_8 are ON position in the proposed inverter.
6. The $-V_{dc}$ output voltage produced by using the switches are S_2, S_3, S_7 and S_8 are ON position in the proposed inverter.
7. The $-1.5V_{dc}$ output voltage produced by using the switches are S_1, S_3, S_7 and S_8 are ON position in the proposed inverter.

The advantages of proposed inverter is

1. The seven level output voltage produced by using 8 switches.
2. All switches are operated with fundamental frequency.
3. Switching losses are reduces.
4. Circuit complexity reduces.
5. Control circuit reduces.
6. Number of cooling equipment, protection circuit reduces.

The seven level output voltage as shown below figure.

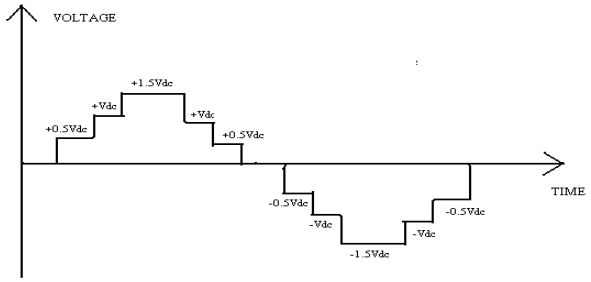


Figure.7 the seven level output voltage produced by the proposed inverter

VI. MATLAB/SIMULATION RESULTS

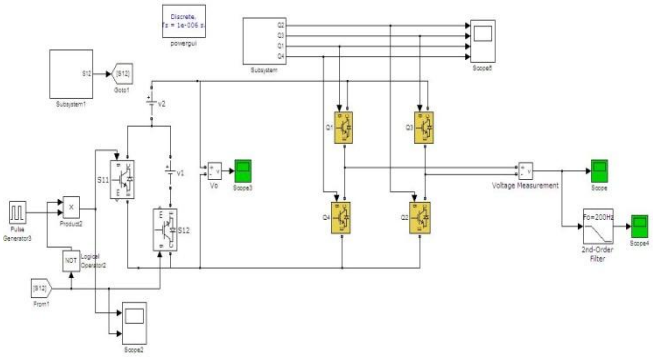


Figure.8 Conventional five-level multilevel inverter simulation diagram

The above figure shows the simulation diagram of conventional five-level multilevel inverter.

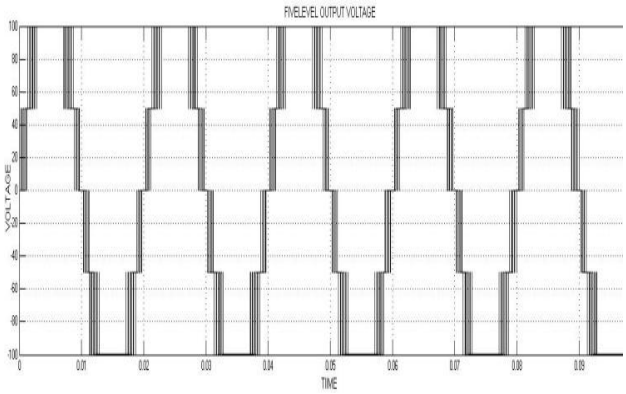


Figure.9 Five level output voltage of conventional five-level multilevel inverter

The above figure shows five-level output voltage produced from conventional five-level inverter.

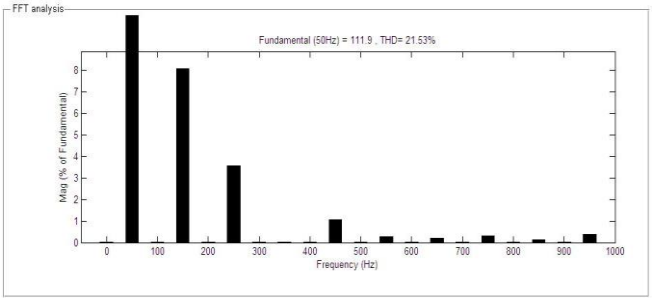


Figure.10 THD value of five-level output voltage from conventional five-level inverter

The THD value is 21.57% of five-level output voltage from conventional five-level inverter as shown above.

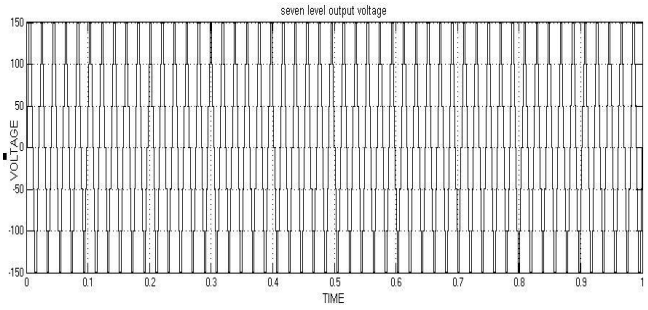


Figure.11. the seven level output voltage produced from proposed inverter

The above figure shows seven level output voltage produced from a new topology of single phase seven-level inverter with less number of power elements for grid connection.

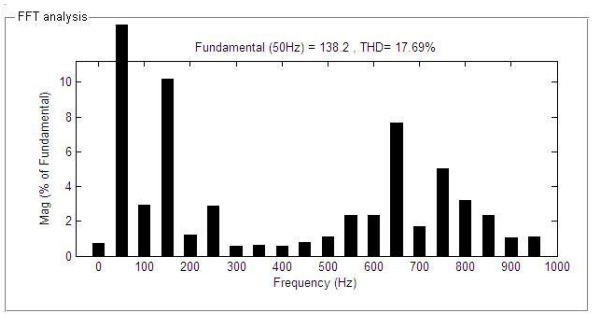


Figure.12 the THD value of proposed inverter

The above figure shows THD value of 17.69% of seven level output voltage from a new topology of single phase seven-level inverter with less number of power elements for grid connection

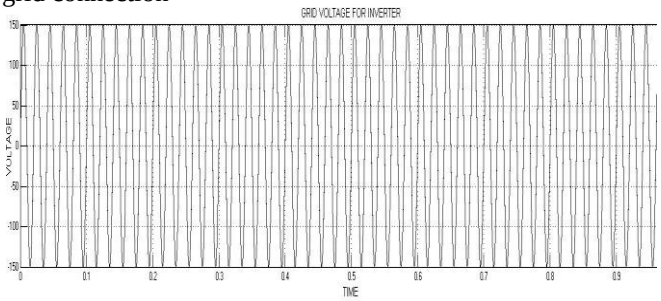


Figure.13 the grid voltage of proposed inverter

The above figure shows the proposed inverter output voltage is connected to the grid

The proposed inverter produces the seven level output voltage from 8 switches and their THD value is 17.69%. The conventional inverter produced the five level output voltage form 6 switches and their THD value is 21.53%. The THD value is low in proposed inverter compared to conventional inverter.

The proposed inverter all switches operated with fundamental frequency, so the switching losses are low. The conventional inverter two switches operated with fundamental frequency and remaining switches operated with switching frequency, so the switching losses are high. The switching losses are low in proposed inverter compared to conventional inverter.

VII. CONCLUSION

This paper has presented "A New topology of Single-Phase Seven-Level Inverter with Less Number of Power Elements for Grid Connection". The control technique is pulse generation for switches in the proposed inverter. All switches in proposed inverter operated with fundamental frequency. So, switching losses and THD value are low in the proposed inverter.

The future scope is photovoltaic arrays, fuel cells used in this proposed inverter.

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