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High Performance Low power Dynamic Multiplier

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Abstract:-The DPST has been applied on both the modified Booth decoder and the compression tree of multipliers to enlarge the power reduction. This paper provides the experience of applying an advanced version of our former dynamic power suppression technique (DPST) on multipliers for high-speed and low-power purposes. To filter out the use-less switching power, there are two approaches, i.e., using registers and using AND gates, to assert the data signals of multipliers after the data transition. The simulation results show that the DPST implementation with AND gates owns an extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of DPST but also leads to a 40% speed improvement. Adopting a Xilinx Spartan 3 Xc3s200 board the proposed DPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding applications, and obtains a 40% power reduction and the overall utilization of the resources reduced to 26%.

Keywords- (DPST), AND, H.264.

I. INTRODUCTION

With the recent rapid advances in multimedia and communication systems, real-time signal processing's like audio signal processing, video/image processing, or large-capacity data processing are increasingly being demanded. Most digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transform (DWT). Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic's determines the execution speed and performance of the entire calculation. Because the multiplier requires the longest delay among the basic operational blocks in digital system, the critical path is determined by the multiplier, in general. For high-speed multiplication, the modified radix-4 Booth's algorithm (MBA) is commonly used. The most effective way to increase the speed of a multiplier is to reduce the number of the partial products because multiplication proceeds a series of additions for the partial products. To reduce the number of calculation steps for the partial products, MBA algorithm has been applied mostly where Wallace tree has taken the role of increasing the speed to add the partial products. To increase the speed of the MBA algorithm, many parallel multiplication architectures have been researched. Multipliers are key components of many high performance systems such as FIR filters, microprocessors, digital signal processors, etc. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest clement in the system. Furthermore, it is generally the most area consuming.

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Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. As a result, whole spectrums of multipliers with different area-speed constraints are designed with fully parallel processing. In between are digit serial multipliers where single digits consisting of several bits are operated on. These multipliers have moderate performance in both speed and area. However, existing digit serial multipliers have been plagued by complicated switching systems and/or irregularities in design. Radix 2^n multipliers which operate on digits in a parallel fashion instead of bits bring the pipelining to the digit level and avoid most of the above problems. They were introduced by M. K. Ibrahim in 1993. These structures are iterative and modular. The pipelining done at the digit level brings the benefit of constant operation speed irrespective of the size of‟ the multiplier. The clock speed is only determined by the digit size which is already fixed before the design is implemented.

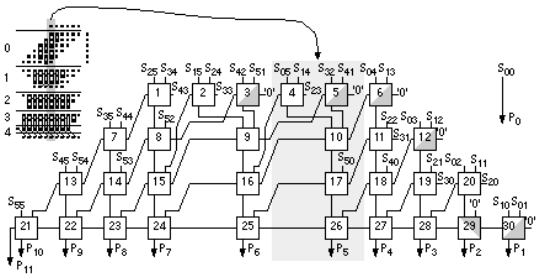

Fig 1: CSA Implementation

The SPST (Spurious Power Suppression Technique) is used for digital signal processing (DSP), Transformations of Digital Image Processing and versatile multimedia functional unit (VMFU) etc. The Booth's radix-4 algorithm, Modified Booth Multiplier, 34-bit CSA are improves speed of Multipliers and SPST adder will reduce the power consumption in addition process.

II. PROPOSED DYNAMIC POWER SUPPRESSION TECHNIQUE (DPST)

The main contribution of this paper is exploring two implementing approaches for the DPST and comparing their efficiency, which provide diverse reference materials for applying the DPST. For completeness of this paper and easy understanding for the readers, we simply review the former DPST first. In Fig. 2, the DPST is illustrated through a low-power adder/subtract or design example. The adder/subtract or is divided into two parts, i.e., the most significant part (MSP) and the least significant part (LSP).

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The MSP of the original adder/subtract or is modified to include detection logic circuits, data controlling circuits, denoted as latch-A and latch-B in Fig. 1, sign extension circuits, and some glue logics for calculating the carry in and carry out signals. The most important part of this study is the design of the control signal asserting circuits, denoted as asserting circuits in Fig. 2, following the detection logic circuits.

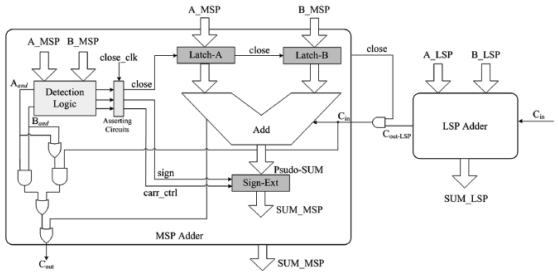

Fig 2 :DPST Adder

III. LOW POWER MULTIPLIER DESIGN

The proposed low-power multiplier is designed by equipping the DPST on a tree multiplier. There are two distinguishing design considerations in designing the proposed multiplier, as listed in the following by applying the DPST on the Modified Booth Encoder Fig. 3 shows a computing example of Booth multiplying two numbers "2AC9" and "006A," where the shadow denotes that the numbers n this part of Booth multiplication are all zero so that this part of the computations can be neglected. Saving those computations can significantly reduce the power consumption caused by the transient signals.

According to the analysis of the multiplication shown in Fig. 3, we propose the DPST-equipped modified-Booth encoder, which is controlled by a detection unit.

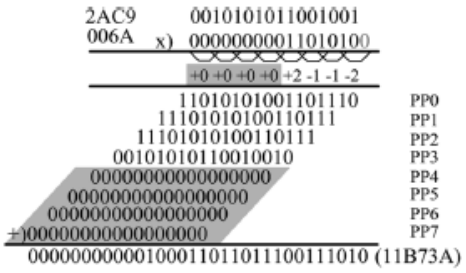

Fig 3:Example multiplication of two numbers

The detection unit has one of the two operands as its input to decide whether the Booth encoder calculates redundant computations. The second design considerations in designing the proposed multiplier is by applying the DPST on the Compression Tree.

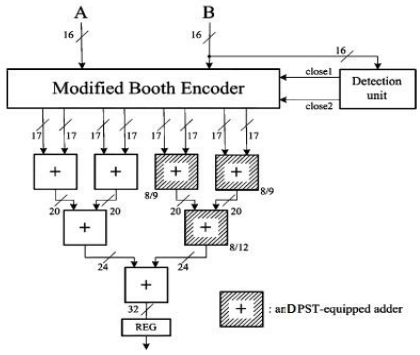

Fig 4: Multiplier equipped with DPST adder.

IV. MODIFIED BOOTH ALGORITHM

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI The common multiplication method is "add and shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Modified Booth algorithm is one of the most popular algorithms. It is a powerful algorithm for signed-number multiplication, which treats both positive and negative numbers uniformly. For the standard add-shift operation, each multiplier bit generates one multiple of the multiplicand to be added to the partial product. If the multiplier is very large, then a large number of multiplicands have to be added. In this case the delay of multiplier is determined mainly by the number of additions to be performed. If there is a way to reduce the number of the additions, the performance will get better. Booth algorithm is a method that will reduce the number of multiplicand multiples. For a given range of numbers to be represented, a higher representation radix leads to fewer digits.

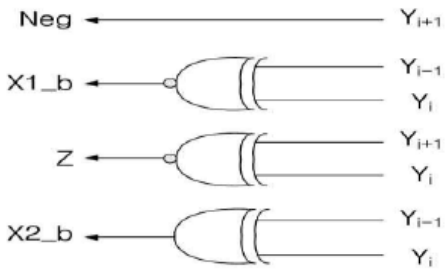

Fig 6: Booth Encoder

V. PERFORMANCE EVALUATION

The DPST-equipped multiplier design has been realized by following the standard cell-based design flow. The efficiency of applying the DPST on modified Booth encoder is described above.

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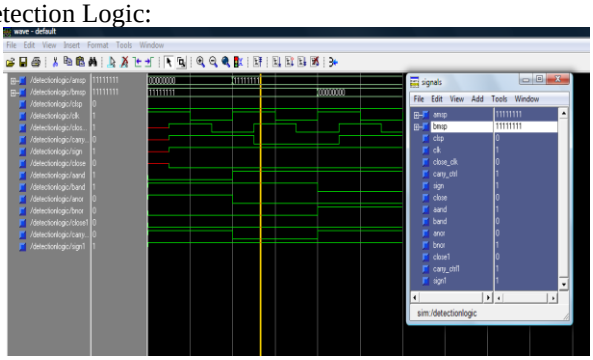
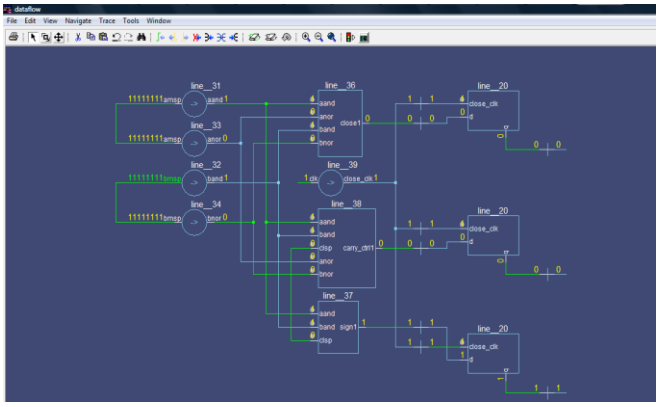
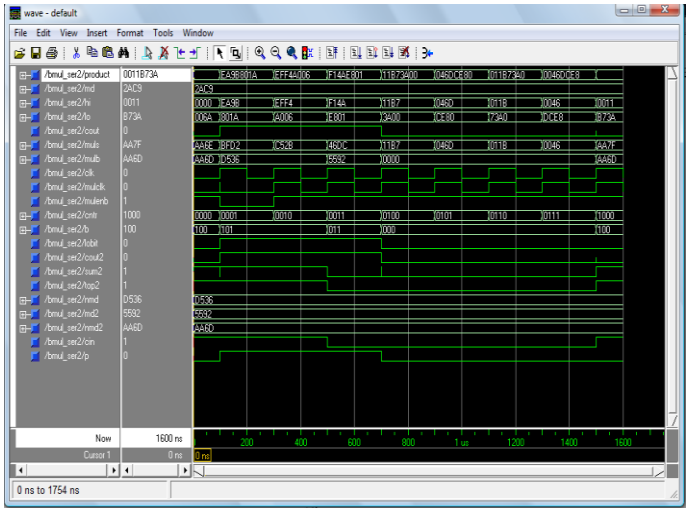
The proposed DPST, 65.67% power dissipation and 28.02% area cost are saved. The simulation results of the original tree multiplier and the two DPST-equipped multipliers with different implementing approaches are listed in Table I.

Detection Logic:



Data Flow of Detection logic circuits using registers:





Multiplier with 16 Bit full Adder equipped with DPST wiith lo=006A

TABLE 1

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	43	1920	2%
Number of Slice Flip Flops	35	3840	1%
Number of 4 input LUTs	77	3840	2%
Number of bonded IOBs	32	173	18%
Number of GCLKs	1	8	12%

From Table I, we can know that both the DPST-equipped multipliers using registers and that using AND gates save about 40% power dissipation of the original tree multiplier. However, the maximum operating frequency of the DPST-equipped multipliers using AND gates is 40% higher (200=142 □ 1) than that using registers. Besides, Table also shows that the proposed DPST-equipped multiplier dissipates only 0.0121 mW per MHz when computing the multiplication of texture coding in H.264. The precision analysis of the test pattern “Stefan” sequence is shown in the figure.

VI.CONCLUSION

In this paper, we propose a multiplier adopting the new DPST implementing approach, i.e., using AND gates in the detection logic unit. The simulation results show that the power reduction of the new approach, i.e., a 40% saving, is very close to that of the former approach. Besides, the new approach leads to a 40% speed improvement when compared with the former one. When implemented in a 0.18-_m CMOS technology, the proposed DPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding. In addition, this paper explores the performance of the proposed design under the conditions of different bit-width input data. The results also show that the new DPST approach not only owns equivalent low-power performance but also leads to a higher maximum speed when compared with the former DPST approach. Moreover, the proposed DPST-equipped multiplier also has better power efficiency when compared with the existing modern multipliers.

REFERENCES

1. J. Choi, J. Jeon, and K. Choi, “Power minimization of functional units by partially guarded computation,” in Proc. IEEE Int. Symp. Low Power Electron. Des., 2000, pp. 131–136.
2. O. Chen, R. Sheen, and S. Wang, “A low-power adder operating on effective dynamic data ranges,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 4, pp. 435–453, Aug. 2002.
3. O. Chen, S.Wang, and Y. W.Wu, “Minimization of switching activities of partial products for designing low-power multipliers,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 11, no. 3, pp. 418–433, Jun.2003.
4. L. Benini, G. D. Micheli, A. Macii, E. Macii, M. Poncino, and R. Scarsi, “Glitching power minimization by selective gate freezing,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 8, no. 3, pp. 287–297, June 2000.
5. S. Henzler, G. Georgakos, J. Berthold, and D. Schmitt-Landsiedel, “Fast power-efficient circuit-block switch-off scheme,” Electron. Lett., vol. 40, no. 2, pp. 103–104, Jan. 2004.
6. Z. Huang and M. D. Ercegovac, “On signal-gating schemes for lowpower adders,” in Proc. 35th Asilomar Conf. Signal, Syst., Comput., 2001, pp. 867–871.
7. Z. Huang, “High-level optimization techniques for low-power multiplier design,” Ph.D. dissertation, Dept. Comput. Sci., Univ. California, Los Angeles, 2003.
8. Z. Huang and M. D. Ercegovac, “High-performance low-power left-toright array multiplier design,” IEEE Trans. Comput., vol. 54, no. 3, pp. 272–283, Mar. 2005

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