# High Performance Current-Mode Multiplier Circuit

**Abdolhamid Sohrabi, AzimRezaei Motlagh, Habib Rostami, Ayat Akbari**

***Abstract— Multiplier-divider circuits is using in digital signal processing base on neural networks and communications (amplifiers with variable gain, modulators, detectors and,…).In Most of CMOS analog circuit, transistors are only in triode or saturate regions; till now both regions not used. In this one kind of current mode multiplier-divider circuits is intrudused.it is very simple, has low die area and wide range in low voltage . all tough this circuit has no sense to temperature variation and varying parameters.***

***A CMOS current-mode analog multiplier/divider circuit is presented. It is suited to standard CMOS fabrication and can be successfully employed in a wide range of analog signal processing applications The circuit power consumptions is 75 µW respectively, while its frequency bandwidths is 59.7 MHz.***

***Index terms— Analog signal processing, current-mode operation, multiplier, reconfigurable circuits.***

## I.INTRODUCTION

Signal processing circuits find a multitude of plications in many domains such as telecommunications, medical equipment,hearing devices, and disk drives [1]–[4], the preference for an analog approach of signal processing systems being mainly motivated by their low-power operation and high speed that allows a real-time signal processing.Multiplier circuits represent intensively used blocks in analog signal processing structures.

The motivation for designing these computational structures is related to their extremely wide range of applications in analog signal processing, such as adaptive qualization, frequency translation, waveform generation and curve-fitting generators, amplitude modulation, automatic gain control, squaring and square rooting, rms-dc conversion, neural networks, and VLSI adaptive filters, or measurement equipment. Based on subthreshold-operated MOS transistors, the realization of multiplier/dividers [5]–[10] requires simple architectures. In order to improve the frequency response of the computational structures and to increase their −3 dB bandwidth, many analog signal processing functions can be achieved by exploiting the squaring characteristic of MOS transistors biased in saturation. In [11]–[15], multiplier structures were presented with single-ended input voltages, the linearization of their characteristics being obtained using proper squaring relations between the input potentials. In order to implement the multiplication of two differential-input voltages, in [16]–[18] multiplier circuits were described based on mathematical principles, similar to the methods used for multipliers with single- input voltages.

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**Abdolhamid Sohrabi,** Department of ElectronicsIslamic Azad University of Bushehr, Boushehr, Iran.

**AzimRezaei Motlagh**, Department of ElectronicsIslamic Azad University of Bushehr, Boushehr, Iran.

**Habib Rostami**, Computer Engineering Department, School of Engineering, Persian Gulf University, Bushehr, Iran.

**Ayat Akbari,** Technical and vocational university, Bushehr Branch, Bushehr, Iran.

The biasing of the multiplier differential core at a current equal to the sum of a constant component and a current proportional to the square of the differential input voltage waspresented in [19] and [20] and allows us to obtain a linear behavior of the implemented multiplier circuits. In another class of multipliers [21]–[23], currents are used as input variables. In this case, the designed circuits present the advantage of an independence of the circuit performances on technological errors. These circuits can implement, based on the same configuration, both multiplying, and dividing functions. Multiplier structures were also reported [24]–[28] with increased linearity, designed using different mathematical principles.

## II.THEORETICAL ANALYSIS

original implementations of current-mode multiplier/divider structure will be presented. The main goal of the proposed design is related to the accuracy of implemented function. The current-mode approach of the multiplier/divider circuits strongly increases its frequency response. A further advantage of the independence of the computational circuit' output currents on technological parameters is that it contributes to an important increase in the accuracy of the multipliers and dividers. Additionally, the operation of the proposed circuits is not affected by the temperature variations.

### *A.Multiplier/Divider Circuit*

The second original realization of the multiplier/divider circuit is presented in Fig. 1. The equation of the functional loop containing M1, M2, M4, and M5 gate-source voltages can be expressed asfollows:

$$2V_{GS}(I2) = VGS\ (I_{OUT1}) + V_{GS}[I_{OUT1} + 2\ (I1 + IO)] \quad (1)$$

resulting

$$I_{OUT1} = I_2 - \frac{2\,(I_1 + I_O)}{2} + \frac{4\,(I_1 + I_O)^2}{16 I_2}. \quad (2)$$

A similar expression can be obtained for the *I*OUT2 current,replacing in (4) the *(I*1 + *IO)* current with *(I*1 −*IO)* current. The expression of the output current of the multiplier/ divider circuit from Fig. 2 is $I_{OUT}= I_{OUT1}-I_{OUT2}+2IO$, resulting $I_{OUT}= (IO\ I1)\ /I2$.The aspect ratios of MOS transistors from Fig. 2 are asfollows: M1–M5, M7–M11, M13–M15, M18–M23 4.5/0.9; M6, M12 10.8/0.9; M16, M17 9/0.9. The chip area of the multiplier/divider implemented in 0.18-$\mu$m CMOS technology, shown in Fig. 1, equals approximately 800 $\mu$m2 (including pads). The negative feedback loops that enforce M4 and M15 transistors and, respectively, M8 and M18 transistors to have the same current are stable, since their speed is suitable for obtaining the requested frequency response for the designed circuits.

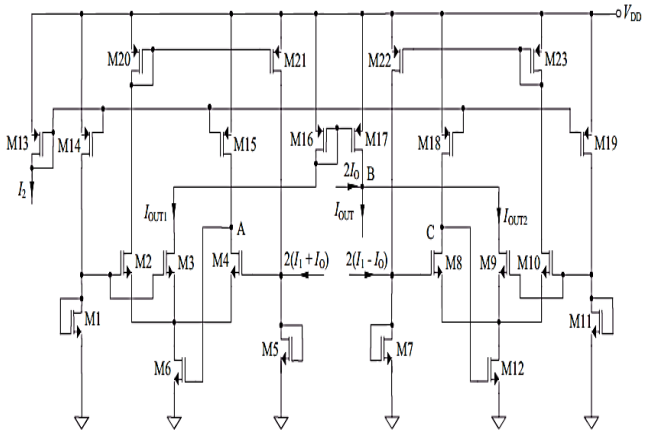


Fig. 1.implementation of the multiplier/divider circuit.

### *B. erors Introduced by Second-Order Effects*

The most important errors introduced in the multiplier/ divider circuits' operation are represented by the mismatches, channel effect modulation, body effect, and mobility degradation. As a result of these undesired effects, the proper functionality of previous circuits will be affected by additive errors. The values of these errors are relatively small (because second-order effects are smaller with afew order of magnitude than the main squaring characteristic that models the MOS transistor operation). Additionally, a multitude of specific design techniques exist that are able to compensate the errors introduced by the second-order effects. The practical realization oftranslinear loops using common-centroid MOS transistors strongly reduces the errors introduced by the mismatches between the corresponding devices. The design of current mirrors using cascade configurations allows an important reduction of the errors caused by the channel length modulation. In this situation, a tradeoff between the impact of the second-order effects and the minimal value of thesupply voltage must be performed. Because the bulks of an important number of MOS transistors from Fig. 1 can be connected totheir source (as a result of the original proposed circuit architectures), the errors introduced by the bulk effect can be canceled out for these devices.

### *C.Small-Signal Frequency Response of Multiplier/Dividers*

The multiplier/divider circuit proposed in Fig. 1 is designed for allowing a high bandwidth. In order to achieve this goal, there exists a single high-impedance node, noted with A, which will impose the maximal frequency of operation. The frequency response of the multiplier/divider circuit presented in Fig. 2 is poorer than the frequency response of the circuit from Fig. 1, because in Fig. 2 there exist three high-impedance nodes (A, B, and C). As most of the nodes in a circuit represent low-impedance nodes, it is expected that the proposed circuits to have relatively high maximal frequencies of operation (79.6 and 59.7 MHz, respectively, obtained after simulations).

## III. SIMULATED RESULTS

The $I_{OUT}(I1)$ simulation for the first multiplier/divider circuit proposed in Fig. 1, for an extended range of $I1$ current (between0 and 10 $\mu$A), is presented in Fig. 2. The $IO$ current is set to be equal to 40 $\mu$A, while the $I2$ current has a parametric variation: 1) 10 $\mu$A; 2) 20 $\mu$A; 3) 30 $\mu$A; and 4) 40 $\mu$A.

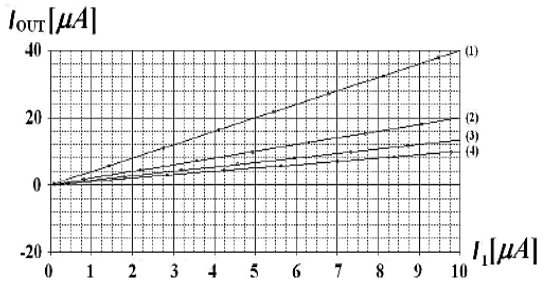


Fig. 2.$I_{OUT}(I1)$ simulation for the multiplier/divider circuit.

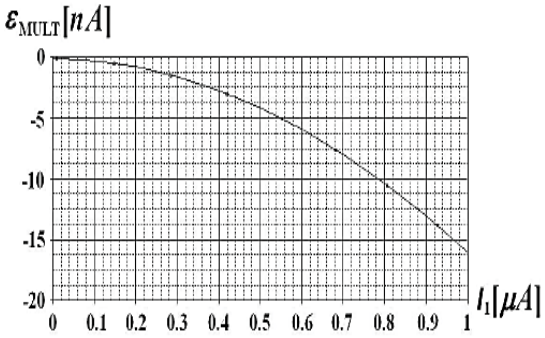


Fig. 3.Simulated linearity error for the multiplier/divider circuit.

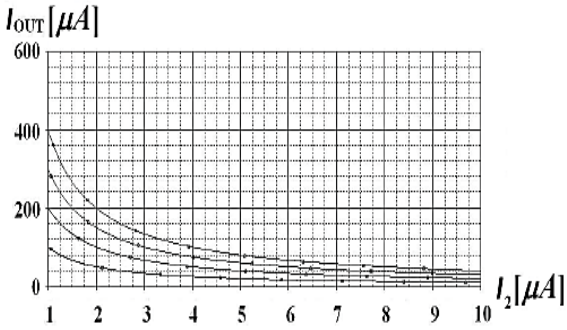


Fig. 4.$I_{OUT}(I2)$ simulation for the multiplier/divider circuit.

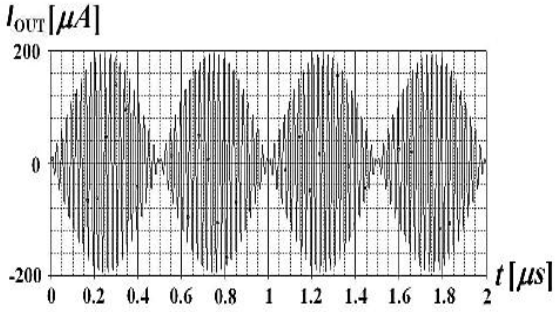


Fig. 5.$I_{OUT}(t)$ simulation for the multiplier/divider circuit.

The simulated linearity errors of the $I_{OUT}(I1)$ characteristic for the multiplier/divider circuits are shown in Fig3. The $\varepsilon_{MULT}$ error is defined as the difference between the ideal linear characteristic of the multiplier/ divider structure and its real characteristic,implemented using the original proposed computational structure. Taking into account PVT and Monte Carlo analysis (performed for 2 standard deviations), the linearity errors of the circuits are smaller than 0.75% (first multiplier/divider) and smaller than 0.9% (secondmultiplier/divider). The $IOUT$ $(I2)$ simulation is

presented in Figs. 4. The *IO* current is set to be equal to 10 $\mu$A, while the *I*1 current has a parametric variation: 1) 10 $\mu$A; 2) 20 $\mu$A; 3) 30 $\mu$A; and 4) 40 $\mu$A. The range of *I*2 current was chosen to be between1 $\mu$A and 10 $\mu$A.

The simulation of the multiplier/divider frequency response shows a −3 dB bandwidth of approximately 59.7 MHz. The transient analysis for the multiplier/divider circuit proposed in Fig. 1 is shown in Fig. 5. The *IO* current is a sinusoidal current with a frequency of 1 MHz and an amplitude equal to 200 $\mu$A, the *I*1 current is a sinusoidal current having a frequency of 60 MHz and an amplitude equal to 300 $\mu$A, while *I*2 is a constant current equal to 300 $\mu$A. The simulations were made using the BSIM4 model, associated with a 0.18-$\mu$m CMOS process, MOS active devices having $fT$= 3.5 GHz.

Comparing with alternative implementations in 0.35-$\mu$m CMOS technology of the proposed multiplier/divider structures, some important advantages can be achieved. The supply voltage can be decreased from 3 to 1.2 V, correlated with a relatively important decrease of the circuits' power consumption. Additionally, the circuits' bandwidths can be increased by their implementation in 0.18-$\mu$m CMOS technology. A comparison between the performances of multiplier circuits reported in the previous works and the multiplier/divider circuits in Figs. 1 and 2 is presented in Table I. The proposed multiplier/divider structures have the most important advantages, such as the smallest linearity error and an increased bandwidth, compared with previously reported circuits. The circuits were designed for implementing in 0.18-$\mu$m CMOS technology, being supplied at 1.2 V. If the range of input currents is limited to 0–5 $\mu$A, the power consumptions of both proposed multiplier/divider circuits (60 and 75 $\mu$W, respectively) are smaller than the power consumption of most previously reported circuits. The input referred noiseis smaller than 0.6 $\mu$V/$\sqrt{}$ Hz for both proposed multiplier/divider structures.

Table I
comparison between the proposed multiplier/divider circuits and previous reported works

| Reference no./Parameter | Technology [$\mu$m] | SupplyVoltage [V] | Linearity Error [%] | Power Consumption [$\mu$W] | Bandwidth [MHz] |
|---|---|---|---|---|---|
| [10] | 0.35 | 2 | 0.9 | 5.5 | 0.2 |
| [15] | | | 1 | 130 | 4.3 |
| [22] | 0.35 | 3.3 | 1.15 | 240 | 44.9 |
| [23] | 0.35 | 3.3 | 1.1 | 340 | 41.8 |
| Fig. 1 | 0.18 | 1.2 | 0.75 | 60 | 79.6 |

## IV. CONCLUSION

This brief presented one original improved accuracy multiplier/ divider circuit. The current-mode operation of the proposed computational structure further increases the circuit' accuracy, while the removal of the impact of temperature variations on the circuit' operation additionally contributes to the increase of the multiplier/divider' performance. The proposed structure have extremely low linearity error (0.9%). The minimal value for the supply voltage of 1.2 V was obtained for implementing the proposed computational structure in 0.18-$\mu$m CMOS technology and was correlated with the model parameter associated with this technology. It is possible to also implement the proposed circuit in processes of 40 or 28 nm, having much lower value of the threshold voltage and, in consequence, allowing a much smaller value of the minimal supply voltage (even less than 1 V). Another important factor that contributes to the small value of the minimal supply voltage is represented by the proposed architectures of the multiplier/divider circuit, compatible with low-voltage operation (avoiding any cascode stages and having a current-mode operation). The circuit bandwidth is 59.7 MHz, while their power consumption is extremely low (75 $\mu$W).

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