Current Follower Trans Conductance Amplifierscurrent-Mode Multiplier Circuit

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Abstract— Multiplier-divider circuits is using in digital signal processing base on neural networks and communications (amplifiers with variable gain, modulators, detectors and,…).In this paper, the design of a simple analog current mode multiplier/divider circuit using only two current followertrans conductance amplifiers (CFTAs) is presented. With the selection of the applied input currents, the proposed circuit can perform four-quadrant current multiplication, division and current-controlled current amplification, all from the same circuit configuration. The circuit is also insensitive to ambient temperature variations. Additionally, the CFTA non-ideality effects and the non-ideal gain and parasitic component effects onthe proposed circuit are studied. The performances of therealized circuit are examined by PSPICE simulations.

Index terms— Analog signal processing, CFTA, multiplier, reconfigurable circuits.

I. INTRODUCTION

Analog multipliers and dividers are pivotal cells in widerange of analog VLSI signal and information processingapplications [1]. They have been found ubiquitously in manyapplications, such as conventional RMS-to-DC converters,A/D-D/A converters, peak detectors, modulators, phasedetectors and synthesizers, and to more recent ones, such asartificial neural networks and fuzzy logic controllers [2]-[4]. Recently, a relatively reported active building block, the so calledcurrent follower trans conductance amplifier (CFTA) wasintroduced [5]. The CFT A device is a combination of a currentfollower and a trans conductance amplifier, providing electronic tuning ability through its trans conductance gain (gm).Therefore, the CFT A is quite suitable for the synthesis of current-mode circuits. Moreover, the use of the CFTA as anactive element provides the circuits with lesser number of passive elements than its counterparts, thereby leading to compact structures in some applications [6]. Although several implementations based on CFT As have been proposed in technical literature [5]-[11], there is not much reported in theliterature on the use of CFT As for realizing analog currentmultiplier/divider circuit.

It is the major goal of this paper to present a simple currentmodeanalog multiplier/divider circuit using only two CFTAswithout any external passive element requirement.

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The proposed circuit presented here can perform four-quadrant multiplication and division all from the same configuration with the selection of the applied current signals. Moreover, the circuit can also perform a current-controlled current amplifier, which its transfer gain can be adjusted electronically by the external bias currents. The circuit is ideally insensitive to temperature variations. The effects of the CFTA non-idealities on the performance of the proposed circuit are investigatedindetail. The PSPICE simulation results for the proposed circuit are included to demonstrate the performance.

II. THEORETICAL ANALYSIS

A.CFTA

An electrical symbol of the CFT A is shown in Fig. 1 ,where is an input terminal and z and x are output terminals. The terminal relation of this device can be expressed by the following equations [5] :

$$v_f = 0 \quad i_z = i_f \quad and \quad i_x = g_m v_z = g_m Z_z i_z \quad (1)$$

where gm is the trans conductance gain of the CFT A, and Z_z isan impedance connected at the terminal z. From equation (1),the current through the terminal z (i_z) follows the input currentthrough the terminal f (i_t), and flows from the terminal z into anoutside impedance Z_z. The voltage drop at the terminal z is transferred to a current at the terminal x (i_x) by atrans conductance gain (g_m), which is usually controlled byelectronic means.

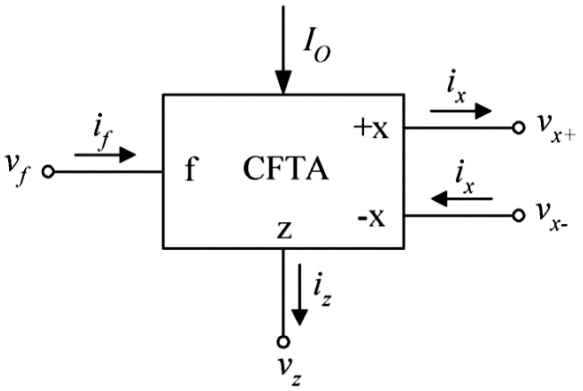

Figure 1.Electrical symbol of the CFTA.

The possible technique to realize the CFT A using bipolar transistor technology is shown in Fig.2 [7], [9]. It mainly comprises a current follower circuit formed by transistors Q_1-$Q_6$and DC bias current I_B" and a multiple-outputtrans conductance amplifier Q_7-Q_{29}. In this case, the trans conductance gain gm of the CFT A is directly proportionalto the external bias current I_Q, which can be written by :

$$g_m = \frac{I_Q}{2V_T} \qquad (2)$$

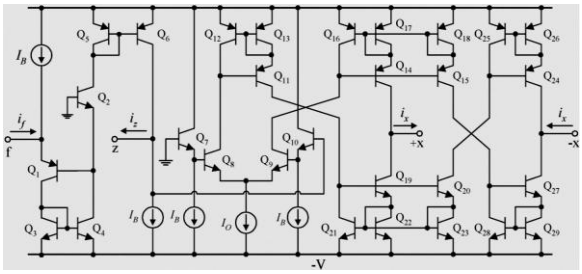

Figure 2.Possible bipolar implementation of the CFTA.

III. PROPOSED CURRENT MULTIPLIER/DIVIDER

Illustrated in Fig.3 is the proposed analog currentmultiplier/divider circuit, which consists of only two CFTAs.Since the circuit does not require any external passivecomponents, it is very suitable for the monolithic implementation. Routine circuit analysis using the CFT A properties described in equation (1) yields the output current tobe as follows.

$$i_{out} = \frac{i_1(t)i_2(t)}{i_3(t)} \qquad (3)$$

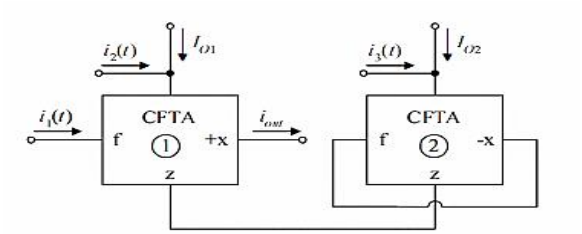

Figure 3.Proposed current multiplier/divider circuit.

Equation (3) clearly shows that, by properly selecting the applied input currents, the proposed circuit can perform bothfour-quadrant multiplication and division of two currentsignals. To function a signal multiplier, the input signalcurrents are Mt) and i2(t), while i3(t) = O. In case of a signaldivider, the input signals are i\(t) (or i2(t)) and i3(t). In addition,if i\(t) is chosen as an input signal current (iin) and i2(t) = i3(t) =0, then the proposed circuit can work as a current-controlledcurrent amplifier that its gain can be controlled electronicallyby the ratio of (/01/102)' It should also be noted from equation(3) that the proposed circuit is temperature insensitive, sincethere is no temperature-dependent term.

IV. NON-IDEALITY EFFECTS

Considering the parasitic elements and transfer errors, the simplified equivalent circuit represented the behavior of the non-ideal CFTA can be illustrated in Fig.4. These result fromthe series input resistance R_f at terminal f, and the shunt outputimpedances ($R_z||C_z$ and $R_x||C_x$) at terminals z and x,respectively. More specifically, a and /3 are the parasiticcurrent gain between the f to z, n to z, and transconductanceinaccuracy factor between the z to x terminals of the CFTA,respectively. Therefore, by taking into account the non-idealCFTA characteristics, the modified current transfer function forthe proposed circuit of Fig.3 can be rewritten as:

$$i_{out} = \left(\frac{\alpha_1\beta_1}{\alpha_2\beta_2}\right)\frac{\frac{i_1 i_2}{i_3}}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)} \qquad (4)$$

Where $\omega_1 = \left[\frac{\alpha_2\beta_2 i_3}{2V_T(C_{z1}+C_{z2})}\right]$ (5)

$$\omega_2 = \left[\frac{1}{R_L C_{x1}}\right] \qquad (6)$$

and R_L is the load resistor. It is apparent from equation (4) thatundesirable factors are yielded by the non-idealities of theCFTA. The tracking errors do affect the current transfer gainwith the factor $\left(\frac{\alpha_1\beta_1}{\alpha_2\beta_2}\right)$. However, to eliminate theseeffects, a careful circuit realization of the CFT A that provides$\alpha_i = \beta_i \cong 1$ should be strictly considered. Note also fromequations (5) and (6) that the useful frequency range (ω) of theproposed circuit is limited by the poles $\omega_1$andω_2. Therefore,the proper operation will be valid for frequencies lower thanapproximately $\frac{\omega_1}{10}$and $\omega_2/10$, or we can say that [12] :

$$\omega \ll 0.1\{\omega_1, \omega_2\} \qquad (7)$$

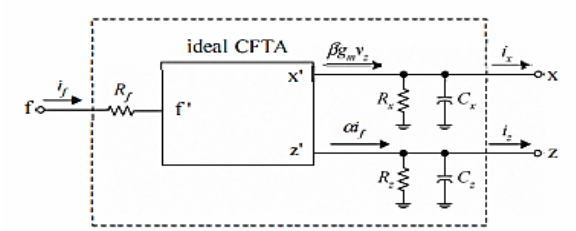

Figure 4.Simplified equivalent circuit of the non-ideal eFTA.

V. SIMULATION RESULTS

To confirm the theoretical analysis, the proposed current multiplier/divider circuit of Fig.3 is simulated in PSPICE program. To perform the CFT A active element in simulations,it was achieved by the schematic bipolar configuration given inFig.2 with the transistor model parameters of PRIOON (PNP)and NPIOON (NPN) of the bipolar arrays ALA400 from AT&T[13,14]. The supply voltage are ±V = ±3V, and the bias currentsare I_B = 50 uA.

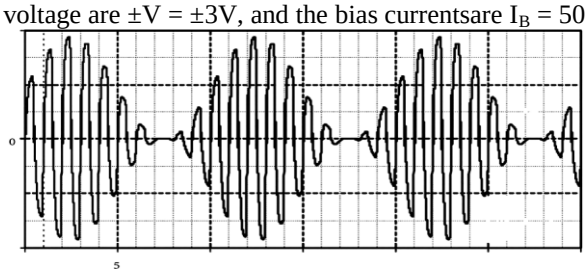

Figure 5, Output current waveform obtained from the multiplier of Fig.3 for 100 kHz modulating sinusoid and 1 MHz carrier inputs.

proposed circuit when operating as a multiplier. In this case,two sinusoidal signals were set to be : $i_1(t)$ = 100 sin2pi(l0e6)t uA, $i_z(t)$ = 100 sin 2pi(10e5)t uA, and $i_3(t)$ =0 uA, whereas the bias currents were chosen as: and $I_{O1} = I_{O2}$ =100 uA. To verify the divider operation, the input signal currents $i_1(t)$ and $i_z(t)$ were kept constant at 50 uA, and $i_3(t)$ was a 100-kHz triangular periodic waveform with a peak valueof 50 uA.

The simulation results are shown in Fig.6. From thesimulations, an accuracy of less than 2% in output waveformswas observed.Fig.7 depicts output current waveforms obtained from theproposed circuit of Fig.3 when working as a current-controlledcurrent amplifier. The simulation result are obtained for threedifferent values of I_{O1}, while I_{O2} =100 uA, $i_1(t) = i_{in}(t)$ = 50 sin 2pi(10e5)t uA, and $i_z(t) = i_3(t) = 0$

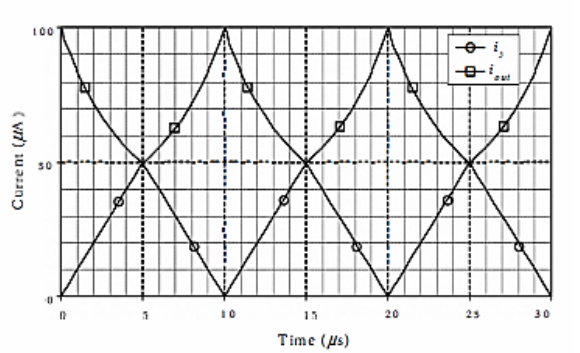

Figure 6. Output current waveform obtained from the divider of Fig.3 for 100 kHz triangular input.

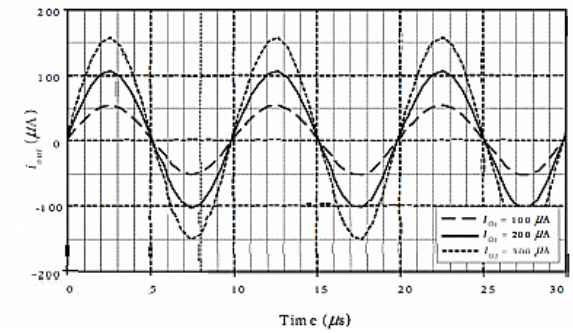

Figure 7, Output current waveforms obtained from Fig.3 for different values of IO1.

Under the conditions of $i_z(t) = i_3(t)$ = 50 uA and $I_{O1} = I_{O2}$ =100 uA, the change in the total harmonic distortion (THD)versus input current signal $i_1(t)$ at operating frequencies f =100 kHz is are given in Fig.8. The obtained results show thatthe THD of the circuit increases rapidly if an input currentsignal is increased beyond the 100 uA level. However, forinput signal amplitudes lower than 50 uA, the THD remains inacceptable limits of the order of THD = 4%. To display the temperature performance of the proposedcircuit, the simulation result is shown in Fig.8 where therelative sensitivity of iout with respect to temperature is approximately equal to 13*10e-9 A/C. It is clearly seen thatthe circuit exhibits excellent temperature insensitivity over awide range of temperatures.

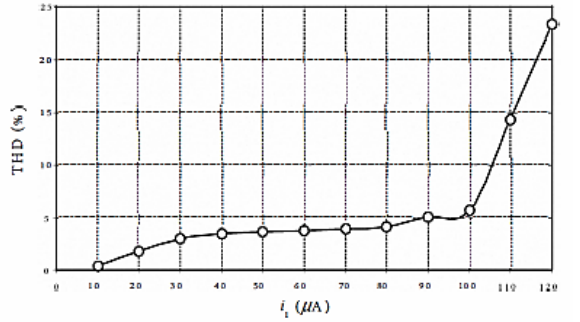

Figure 8. Variation of THD against input current amplitude.

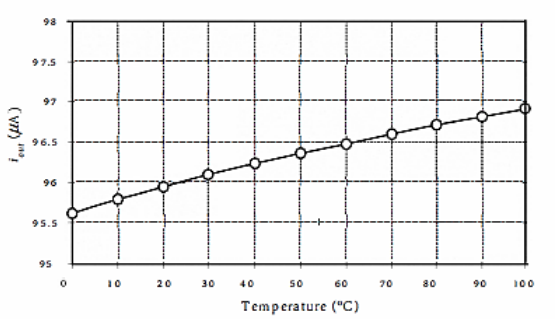

Figure 9.Variation of the output current iout against temperature.

VI. CONCLUSION

Simple topology for realizing current-mode analogmultiplier/divider circuit has been presented. The proposed circuit employs only two CFT As without needing external passive elements. The circuit can be used for performing themultiplication, division and amplification without changing itstopology. The proposed circuit is simple and canonical instructure, temperature-insensitive, and suitable for fullymonolithic integration. The effects of CFTA non-idealities arediscussed, and simulation results are provided.

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