Comparison of Power Consumption in Array Multiplier with and without SVL Circuit

K. Raja Kumari, S. Leela Lakshmi

Abstract -In this paper, we performed the comparative analysis of power consumption of array multiplier circuit implemented with two adder modules and Self Adjustable Voltage level circuit (SVL). The adder modules chosen were 10 transistor- Static Energy Recovery CMOS adder and 8 transistor CMOS (SERF) circuits. At first, the circuit was simulated with adder modules without applying the SVL circuit. And secondly, SVL circuit was incorporated in the adder modules for simulation. In the multiplier architecture chosen, less power consumption was observed being consumed by the SERF adder based multipliers applied with SVL circuit. .

Key Words: 10 Transistor SERF Adder, 8 transistor adder, SVL Circuit.

Nomenclature

Pleak	Leakage power dissipation
Ileak	Leakage current
Vdd	supply voltage
P dynamic	Dynamic power dissipation
VL	Voltage supply to the load circuit
Vn	Voltage drop of all weak NMOS transistor
Vdsn	Drain to source voltage of NMOS transistor
Vss	gnd
ΔT	propagation delay
Tand	Delay of AND gates
Tsum	Delay between Cin and sum bit of full Adder
Tcarry	Propagation delay of input and output carry
Tfinal	Delay of final stage carry look ahead adder

Abbreviations

SVL	Self Adjustable Voltage level circuit
CMOS	Complementary metal oxide semiconductor
SERF	Static Energy Recovery CMOS adder
MTCMOS	multi- Threshold Voltage CMOS
VTCMOS	Variable threshold- voltage CMOS
PTM	Predictive Technology Model
VL	low supply voltage
NMOS	N-channel MOS
GND	ground
PMOS	P-channel MOS
VLSI	Very Large Scale Integration

I. INTRODUCTION

Today's Semiconductor device industries have been challenged with producing low power high performing portable electronic devices due to the increasing demand of their own consumer market. It is believed that the next generation portable electronic devices have to be developed with ultra-low power computational units such as multipliers [4].

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In order to incorporate low Power design into such computational units, Leakage power has to be minimized because leakage power accounts for the significant portion of the total power consumption in such circuits in deep sub-micron regimes. Research has shown that greater than 50% of the total power consumption is due to leakage phenomenon within which stand-by leakage is another major component [6]. The stand-by leakage is the only source of power consumption in a static circuit [8]. This means that a fully charged device will be deficient of any charge even if it is not used for some long time. In Such case the efficiency of the device is compromised.

The CMOS technology, supply voltage and threshold voltage have been scaled down to achieve faster performing devices [12]. However, leakage current has increased considerably and has become a major component of the total power consumption [1]. The leakage power component further is comprised of stand-by and active leakage currents. Most microelectronic circuits remain for considerable amount of time in static state. Therefore, low power design approach should also include stand-by leakage power reduction in static CMOS circuits. Stand-by leakage power dissipation dominates the dynamic power dissipation in deep sub-micron circuits and also in circuits that remain in idle mode for long time such as mobile phones [1]. The Stand-by leakage power dissipation is the power dissipated by the Static or the "idle" circuit. i.e. when the circuit is not turned ON. In the same lines, the dynamic power dissipation occurs when the circuit is switching. The equations (1) and (2) denote leakage and dynamic power dissipation respectively.

$$Pleak = Ileak \times Vdd \quad (1)$$

$$Pdynamic = \alpha f C Vdd \quad (2)$$

Where α is the switching activity, f is the operating frequency, C is the load capacitance, Vdd is the supply voltage and I leak is the cumulative leakage current due to all leakage components [1], [14].The total power dissipation is the sum of (1) and (2). The leakage current consists of various components, such as Pn Junction Reverse-Bias current, subthreshold leakage, Gate leakage, Gate –induced drain leakage and punch through leakage [1], [3], [7], [8], [9], [10]. Among them the subthreshold leakage is considered to be a major contributing component of the leakage power. These leakage mechanisms are well described by literature [1].

Literature [13] includes the ideas of bulk driven voltage which generates a channel inversion and sufficiently low gate to source voltage supply. The multi- Threshold Voltage CMOS (MTCMOS) and Variable threshold- voltage CMOS (VTCMOS) are the two regularly used techniques for reducing stand- by leakage power [2].

The MTCMOS technique requires additional fabrication process for higher threshold voltage and the storage circuits are not able to retain data [2].

The VTCMOS technique has major drawbacks as well, such as large area penalty, slow substrate-bias Controlling operation and large power overhead [2]. Therefore, in order to skip the above mentioned drawbacks, a SVL circuit was chosen which minimizes stand-by leakage power whilst maintaining high- speed performance.

Figure 1 shows a self-adjustable voltage level circuit with Vdd as supply and VL as output voltages. The output voltage from this circuit is applied to the load circuit. The load circuits are the adder modules of conventional CMOS adder and SERF adder including their half adders which all are net-listed in the multiplier circuits. The SVL circuit hangs above these adder modules and drizzles only minimum voltages to them as such the sub threshold leakage current of idle MOSFETS decreases and the standby leakage power is minimized. For the stand-by mode that is when SL= 1 it supplies less voltage to the load circuit through "weakly on" NMOS transistors [6].The voltage supplied to the load circuit is

$$VL = Vdd - Vn \quad (3)$$

Where Vn is the voltage drop of all "weakly on" NMOS transistors. If Vdsn is the drain to source voltage of the NMOS transistors, then,

$$Vdsn = VL - Vss \quad (4)$$

Now, from equations (3) and (4), we have,

$$Vdsn = Vdd - Vn - Vss \quad (5)$$

Equation (5) shows that Vdsn can be decreased by increasing Vn [6]. In other words, by increasing the number of NMOS transistors. By decreasing Vdsn the Drain-Induced Barrier Lowering effect is decreased which increases the threshold voltage of NMOS transistors [6], [1]. The increased threshold voltage reduces the sub threshold leakage current of the NMOS transistors and thus, the Stand-by leakage power is reduced [6]. It will also decrease the dynamic power dissipation because of low supply voltage, VL.

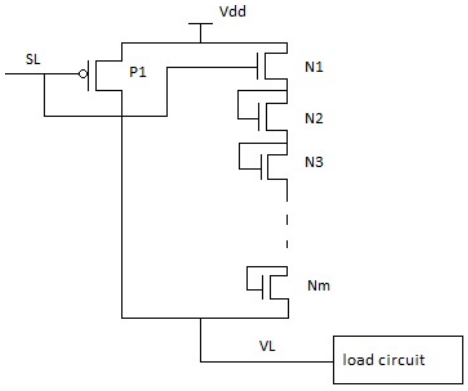

Figure1. Self-Adjustable Voltage Level Circuit.

Initially, each multiplier circuits were simulated using conventional 28 transistor adders and 10 transistor SERF adders one at a time. Their corresponding stand-by leakage power dissipation, delay and dynamic power were noted. And then, the two adder modules were constructed with SVL circuit and put into the multiplier architecture forming the complete circuit mesh one at a time. Again, their corresponding stand-by leakage power dissipation, delay and dynamic power were noted and a comparative analysis and evaluation was carried out. The SERF adder with SVL circuit based multipliers outperformed all other combinations which suggest that this combination (SERF adder with SVL circuit based multipliers) is suitable for ultra-low power design of multipliers. SVL circuits have been applied by literature [6] in CMOS sequential circuits, by Literature [2] in SRAM. This is the first time SVL circuits are being applied in CMOS multiplier circuits.

II. ADDER MODULES

2.1 10Transistor (10T) Adder

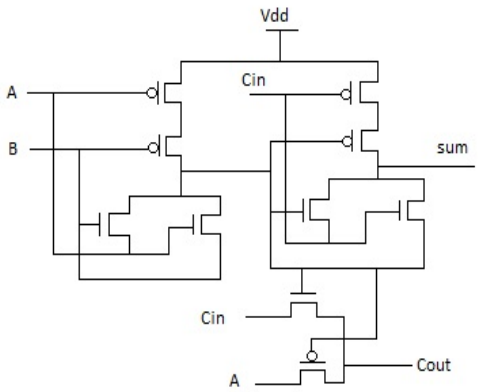

Figure 2.SERF full adder

The 10 transistor SERF adder is considered to be efficient in both low power consumption and less chip area [5]. In non-energy recovering circuits the charge from load capacitance during high is directly dumped to the ground (GND) during low logic level. In contrast, SERF adder reuses charge which the load capacitance during logic high to excite the gates rather than dumping the charge to the GND [5].

The circuit is shown in figure 3 which consists of two exclusive NORs realized by four transistors. The Carry Out is calculated by multiplexing inputs A and carry in (Cin). The sum is generated from the output of second stage exclusive NOR. If there is a capacitor charging at the output node of the first exclusive NOR and if initially, A=B=0, and A goes to high. When A and B both equal to low the capacitor is charged by VDD. In the next stage when B goes to high keeping A fixed at low, the capacitor discharges through A. Some charge is retained in A. Hence when A goes high it is not required to be charged fully. So the energy consumption is well managed and low here [5].

2.2 8Transistor adder (8T) Adder:

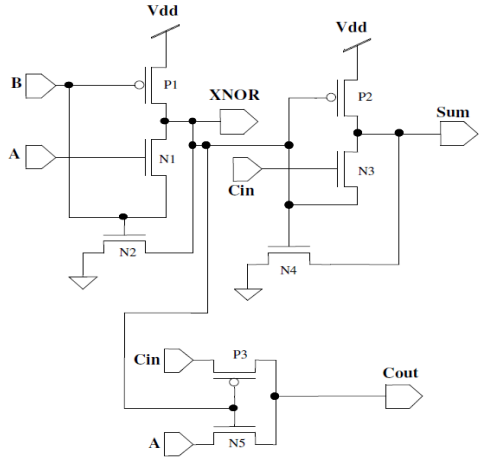

Figure 3.Conventional CMOS full adder with 8T

The proposed architecture for 8t full adder consists of 2 xnor gates. It provides less power consumption when compared to conventional 28t, 10t full adders. Static power dissipation in the proposed multiplier architectures can be overcomed by designing full adders in multipliers driven by svl circuit
The area, delay and power consumed by the various multipliers when the full adders are designed by 28t, 10t adders are compared with proposed 8t adder. The proposed 8t consumes less area, less power and consumes less time.

III. MULTIPLIER ARCHITECTURE

The multipliers are the well organized array of adder cells [4]. The performance and characteristics of the multipliers depend upon the algorithm in which they are based on [4]. Due to the emphasis of low power design, speed is not only the criterion for design objective. Therefore, designing multipliers with low power adder modules is essential keeping an eye on the consumer market of portable electronic devices. In this paper, we have designed and characterized three well-known multipliers viz. The 4Bits Array multiplier, the 4 bits carry Save Multiplier and 4 bits Baugh Wooley Multipliers.

3.1 Array Multiplier

Bit Array multiplier has a simple expandable structure which makes it easy to understand. In Bit Array Multiplier, the partial product is generated by multiplying multiplicand and multiplier bits [4]. The partial products are placed according to the correct shift in bit orders and then are added. If there are N partial products in the Bit – Array multiplier, (N-1) bit adders are required. Figure 4 shows the schematic of 4 bit- array multiplier. There is more than just one critical path in the Bit-Array multiplier.

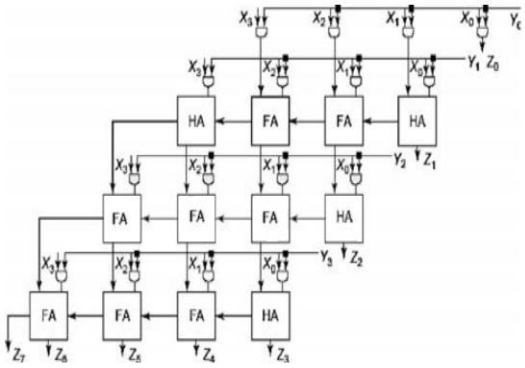

Figure 4. 4bits Array Multiplier

Theoretically, the approximate equation to calculate the propagation delay of these paths is shown below.

$$\Delta T = Tand + Tsum + [(Y-1)+(X-2)]Tcarry \quad (6)$$

Where, Tsum is the delay between Carry in (Cin) and the sum bit of full adder, Tand is the delay of the AND gates, Y is the width of multiplicand, X is the width of multiplier and Tcarry is the propagation delay of the input and output carry [4].

IV. SIMULATION SET UP AND RESULTS

The CMOS sub-circuit of the CMOS AND gate, CMOS full adders and half adders and SVL circuits were created in LTSPICE decks specifying the input and output nodes. The global variables such as supply voltage and ground were specified respectively as Vdd and Vss. These sub-circuit programs are called each time when they are required by the multiplier architecture. CMOS multiplier circuits' net lists are created with different combination of adders modules. The functionality of each circuit, CMOS AND, CMOS full adders and half adders were verified before creating the multiplier architecture net lists. The respective logic truth tables of half adder, full adder, CMOS AND gate and inverters were used during the verification. After extracting the multiplier architecture net lists, each multiplier circuits with different adder modules combination were simulated. These analyses are called the transient analysis and read on the Scope of the LTSPICE. Multipliers functionality verification can be done with number of different methods and approaches. In multiplier function verification, we chose a typical 4bits by 4 bits multiplying method where partial products generated are added to produce the final product in the form of [P7….to… P0] shown by equation (7) below

a3 a2 a1 a0
X b3 b2 b1 b0
p7 p6 p5 p4 p3 p2 p1 p0 (7)

We take the random two 4 bits numbers and find the final result of the multiplication in 8 bit number. Subsequently, we supply the same multiplier and multiplicand two 4 bits number through the inputs a3a2a1a0 and b3b2b1b0 in the multiplier net list and check the results in LTSPICE Scope readout. The corresponding 1s and 0s of [P7…P0] are compared to highs and lows of the output. If they match, the multiplier circuit is functioning correctly.
The net lists of the circuits were extracted and simulation was performed using LTSPICE. All the CMOS circuits were implemented with 90nm node technology in LTSPICE.
All the multipliers were compared and analyzed for power consumption.

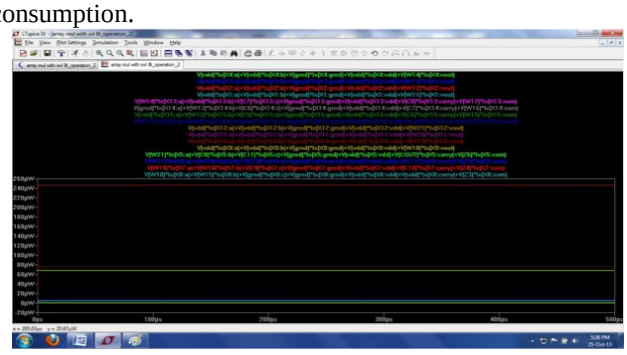

Figure 5.power results for 8T with SVL

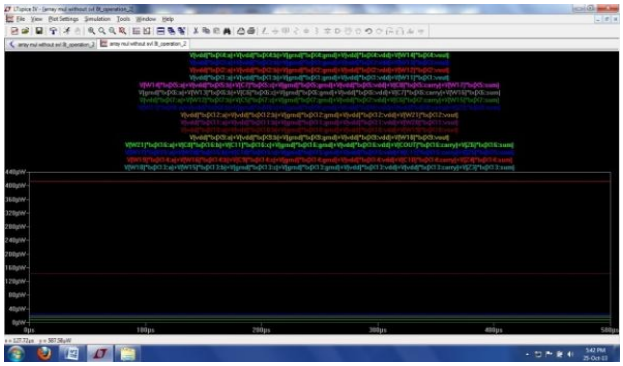

Figure 6.power results for 8T without SVL

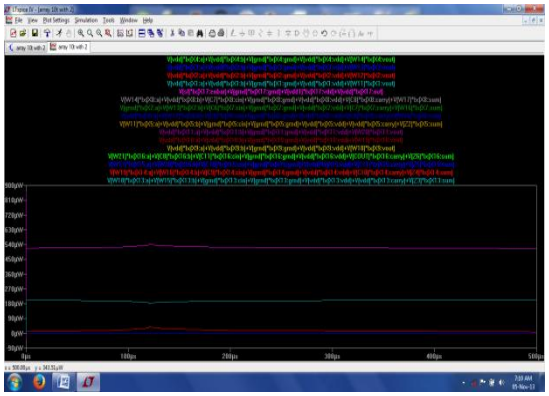

Figure 7.power results for 10T with SVL

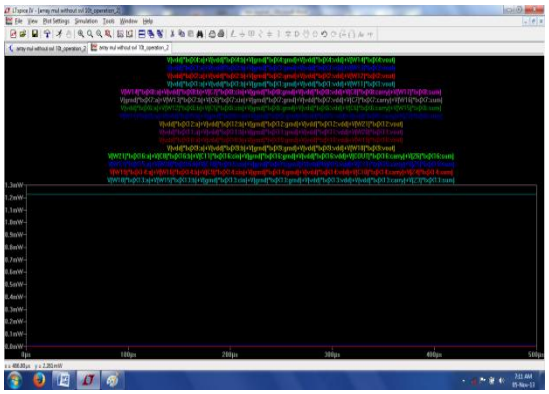

Figure 8.power results for 10T without SVL

V. FUTURE WORK

Dual threshold CMOS technique can be applied into the multiplier circuits. There are certain critical and non- critical paths in the multiplier circuits. A higher threshold voltage can be assigned to the transistors in the non- critical paths and lower threshold voltage can be assigned to the transistors in the critical paths as such the leakage current is minimized without compromising The performance [1]. Dual threshold CMOS can reduce leakage power in both stand-by and active mode of operation without a penalty on both area and delay [1].

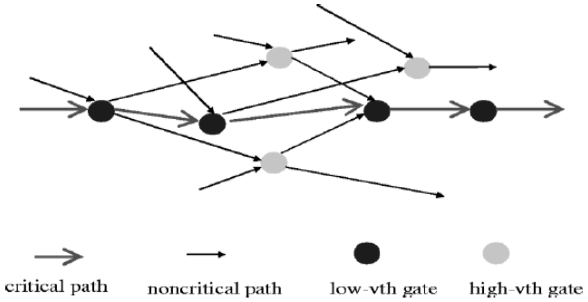

Figure 9. Dual threshold Voltage circuitry

VI. CONCLUSIONS

The power measurement with svl and without svl and area measured for the 10t and 8t adder. The proposed 8t adder consumes less power when used in the above multiplier. Therefore, the multiplier circuits with SERF Adder applied with SVL circuit outperform the multiplier circuits with CMOS 8T Adder applied with SVL circuit in terms of stand-by leakage power dissipation. In other words, the SERF adders applied with SVL circuit are suited for ultra-low power design of CMOS multipliers circuits.

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