

Design of Low Power SRAM Architecture with Isolated Read and Write Operations at Deep Submicron CMOS Technology

Naveen Kumar Sarva, U. Nageswara Rao, D. Ramesh, D. Harihara Santosh

Abstract - Low power VLSI design has become the major challenge of chip designs as leakage power has been rising with scaling of technologies. In deep submicron technologies, leakage power becomes a key for a low power design due to its ever increasing proportion in chip's total power consumption. Motivated by emerging battery-operated application on one hand and shrinking technology of deep sub micron on the other hand, leakage power dissipation is playing a significant role in the total power dissipation as threshold voltage becomes low. Here we proposed Novel SRAM architecture called IP-SRAM with separate write sub-cell and read sub-cell. In this paper we designed the total 8 bit SRAM architecture with newly proposed techniques and compare this one with conventional SRAM architecture and we observed that the total power consumption is reduced. Here the total architecture was designed with 180nm technology.

Keywords – IP-SRAM, Deep Submicron Technology, Sub Threshold Leakage Power.

I. INTRODUCTION

SRAMs strongly IMPACT the over- all power, performance, stability and area requirements. In order to manage constrained tradeoffs, they must be specially designed for target applications because The Static Random Access Memory (SRAM) is a critical component in the modern Digital Systems-on-Chip (SoCs) [1]. Rapid growth in semiconductor technology has led to shrinking of feature sizes of transistors using deep submicron (DSM) process. As MOS transistors enter deep submicron sizes, undesirable consequences regarding power consumption arise. Until recently, dynamic or switching power component dominated the total power dissipated by an IC. Voltage scaling is perhaps the most effective method to decrease dynamic power due to the square law dependency of digital circuit active power on the supply voltage.

As a result, this demands a reduction of threshold voltage to maintain performance. Low threshold voltage results in an exponential increase in the sub-threshold leakage current. On the other hand as technology scales down, shorter channel lengths result in increased sub-threshold leakage current through an off transistor. Therefore, in DSM process static or leakage power becomes a considerable proportion of the total power dissipation.

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For these reasons, static power consumption, i.e. leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies.

Here we present some VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power. In this paper we designed SRAM cell with low power techniques with 180nm technology and compare with conventional SRAM cell [2].

II. CONVENTIONAL 6-T SRAM CELL

Static Random Access Memory (SRAM) to be one of the most fundamental and vitally important memory technologies today. Because they are fast, robust, and easily manufactured in standard logic processes, they are nearly universally found on the same die with microcontrollers and microprocessors. Due to their higher speed SRAM based Cache memories and System-on-chips are commonly used. Due to device scaling there are several design challenges for nanometer SRAM design. Low power SRAM design is crucial since it takes a large fraction of total power and die area in high performance processors. A SRAM cell must meet the requirements for the operation in submicron/nano ranges. The scaling of CMOS technology [3] has significant impacts on SRAM cell random fluctuation of electrical characteristics and substantial leakage current.

The schematic of SRAM cell is shown in the Fig.1. It has 2 pull up PMOS and 2 NMOS pull down transistors as two cross coupled inverters and two 2 NMOS access transistors to access the SRAM cell during Read and Write operations [4]. Both the bit lines (BL and BLB) are used to transfer the data during the read and write operations in a differential manner. To have better noise margin, the data signal and its inverse is provided to BL and BLb respectively. The data is stored as two stable states, at storing points VR and VL, and denoted as 0 and 1.

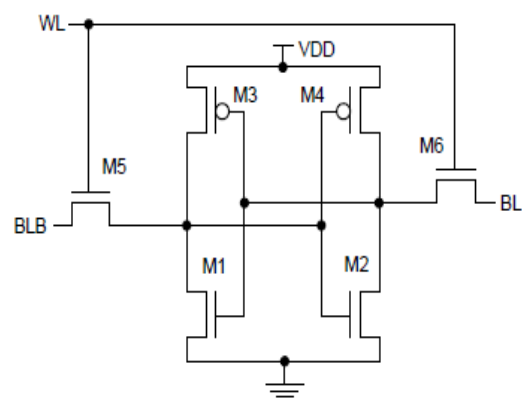


Fig 1. Conventional 6-T SRAM

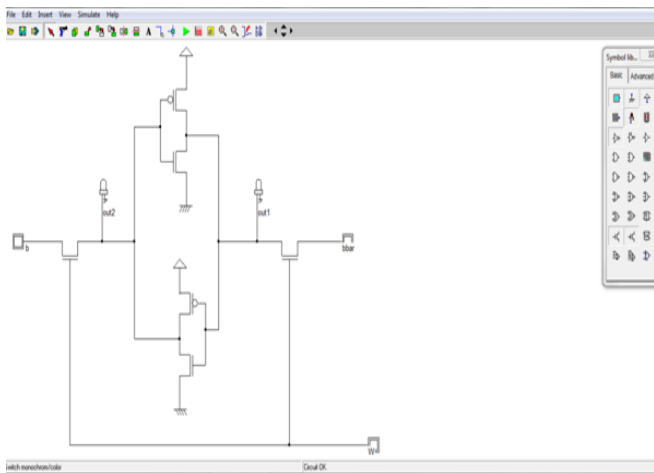


Fig 2. Schematic for conventional sram cell

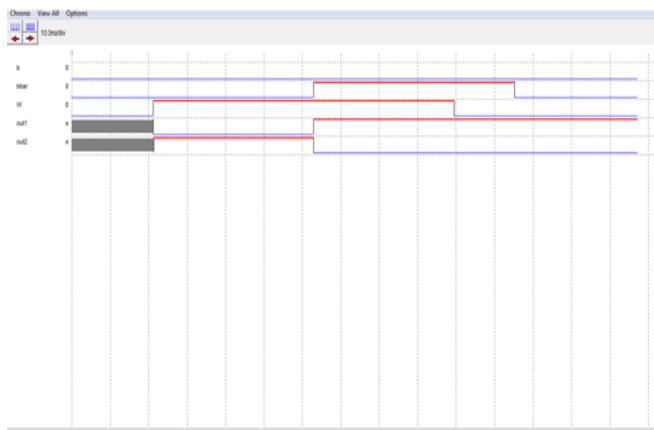


Fig 3. Simulation results for conventional sram cell

The dual inverter latch is heart of the SRAM cell [5]. Each end of the latch holds a value that is the complement of the other side.

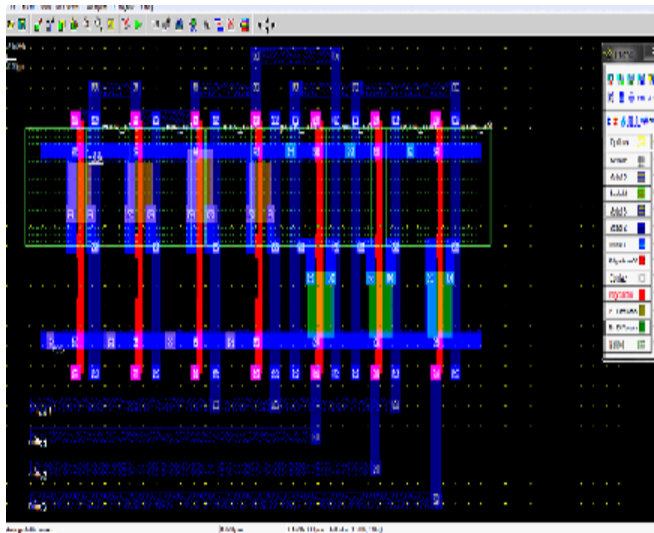


Fig 4. Layout for conventional sram cell

III. LFS – SRAM CELL

In power gated leakage feedback with stack, we are combining two techniques i.e. leakage feedback approach due to less transistor than sleepy-stack in which we replaces each transistor in base case into three transistors, and ultra low power technique i.e. Stack approach, here we are combining these two techniques.

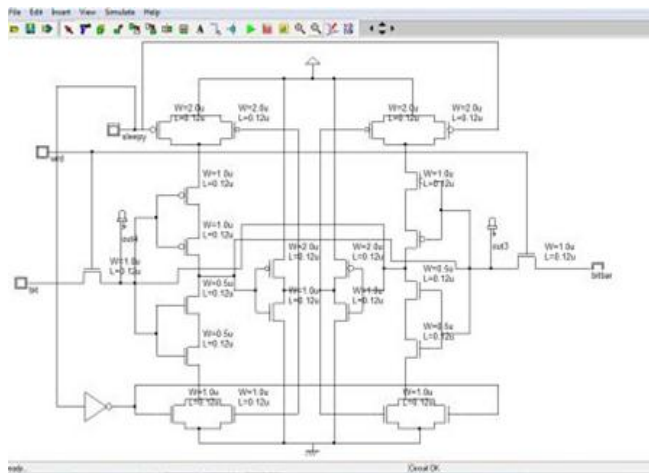


Fig 5. Schematic for LFS-SRAM cell

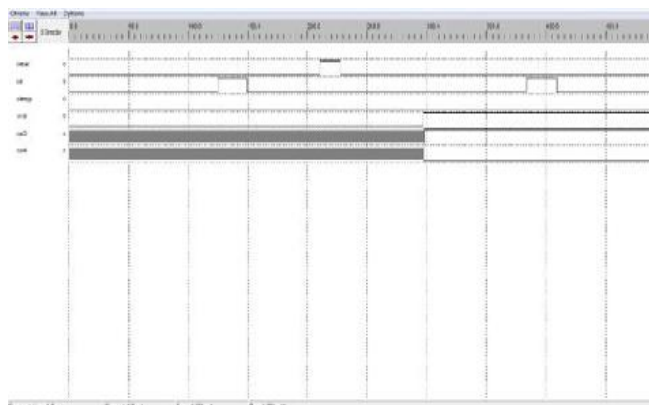


Fig 6. Simulation results for LFS-SRAM cell

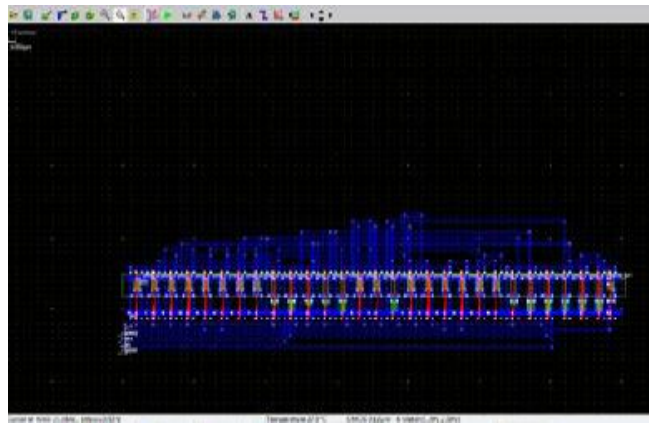


Fig 7. Layout for LFS-SRAM cell

IV. IP-SRAM CELL

In the novel power gated Improved P3 (IP) SRAM Cell, the combination of two separate sub-cells (write and read) structure is proposed with a pMOS gated ground and drowsy scheme to reduce the active and standby power without losing the cells' performance. The data write and memory storage is being done at upper sub-cell while lower sub-cell is used for data- read operation, only. In the active mode of operation, the cell is supplied with VDD [6]. In data write mode, the data read sub-cell is completely isolated from the data write sub- cell through BL's and vice-versa, which further improves the cell's stability.



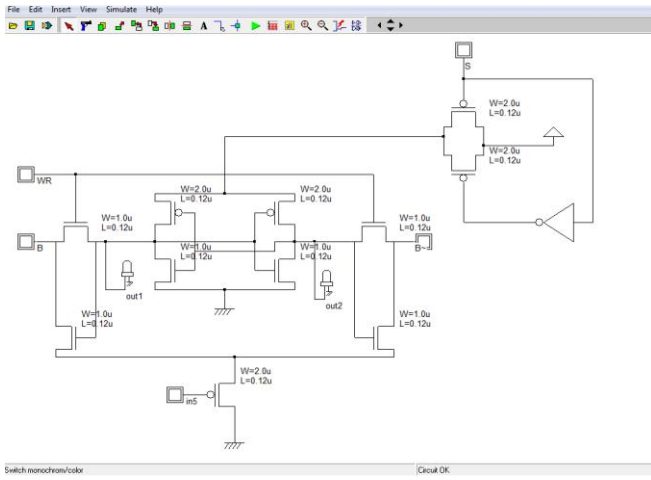


Fig 8. Schematic for IP-SRAM cell

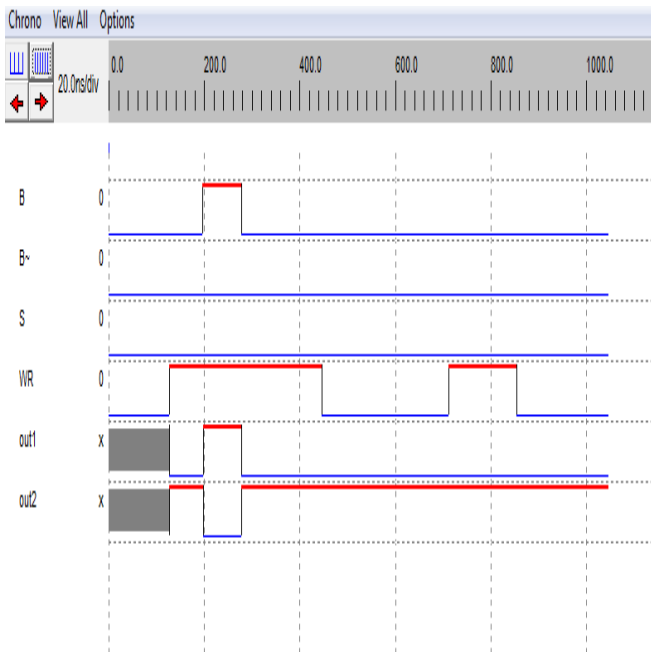


Fig 9. Simulation results for IP-SRAM cell

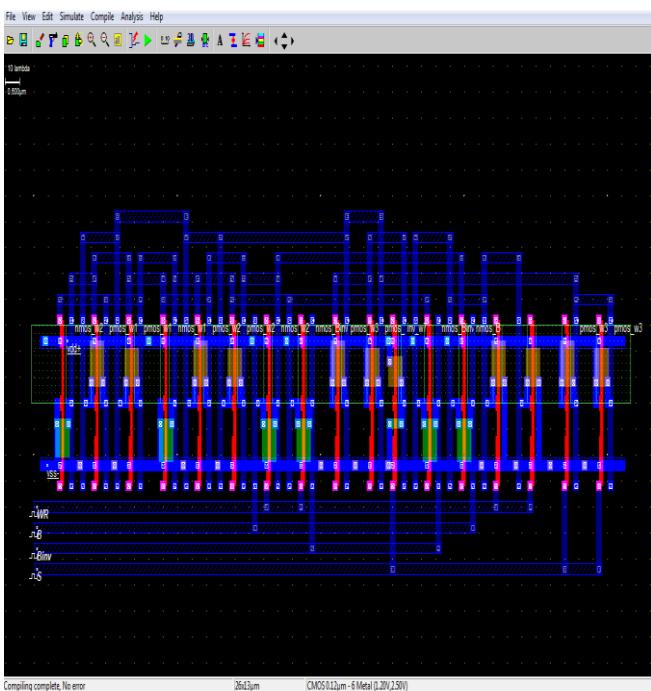


Fig 10. Layout for IP-SRAM cell

V. SRAM ARCHITECTURE

A general SRAM Architecture and its peripherals are shown in below. The SRAM array consists of rows and columns of bit cells. For small caches, it is possible to place a word of data in a row; however, in large memories because of space limitation, it is necessary to arrange several words of data in each row [7]. Cells of each column share the same bitlines. Before the read access, the bitlines are precharged to a known value by the precharge circuits. The row decoders are used to select a row in the array. Depending on the mode of operation, storage cells in the row are connected the common bitlines and either the stored data in the cell is read by sense amplifiers or overwritten by the write circuits. For larger memories, multiple blocks of the same array are used such that an extra address generator called block address decoder is required.

VI. ROW DECODER

A row decoder is used to decode the input address and select the word line. When performing a write or read operation only one of the row is selected and 8 bits of data is transmitted. The row decoder selects one of those rows, depending on the 3 bit address given to it. In order to design an 8x8 SRAM a 3x8 decoder [8] is used. Number of wordline equals to the number of rows in the SRAM cell array [9].

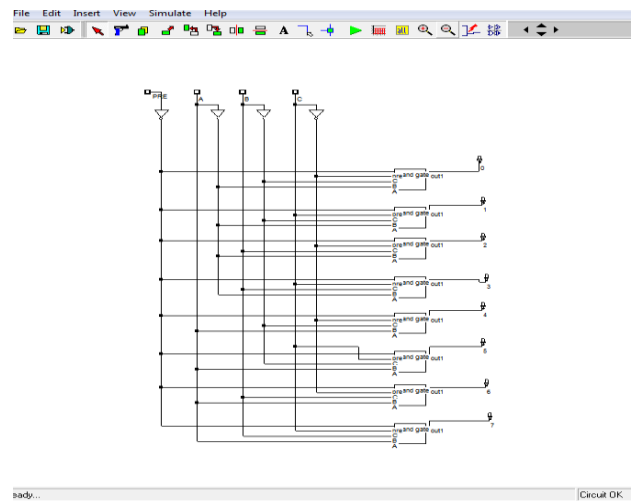


Fig 11. Schematic for 3to8 decoder

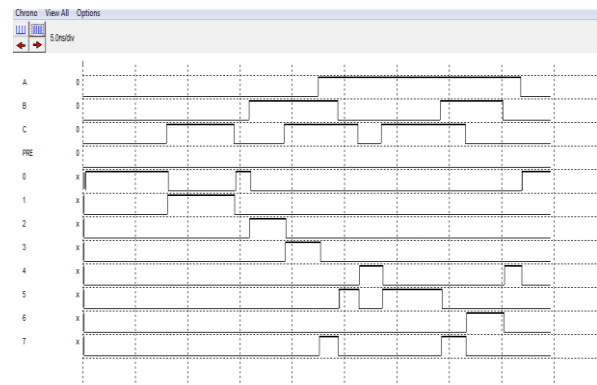


Fig 12. Simulation results for 3to8 decoder

VII. SRAM ARCHITECTURE

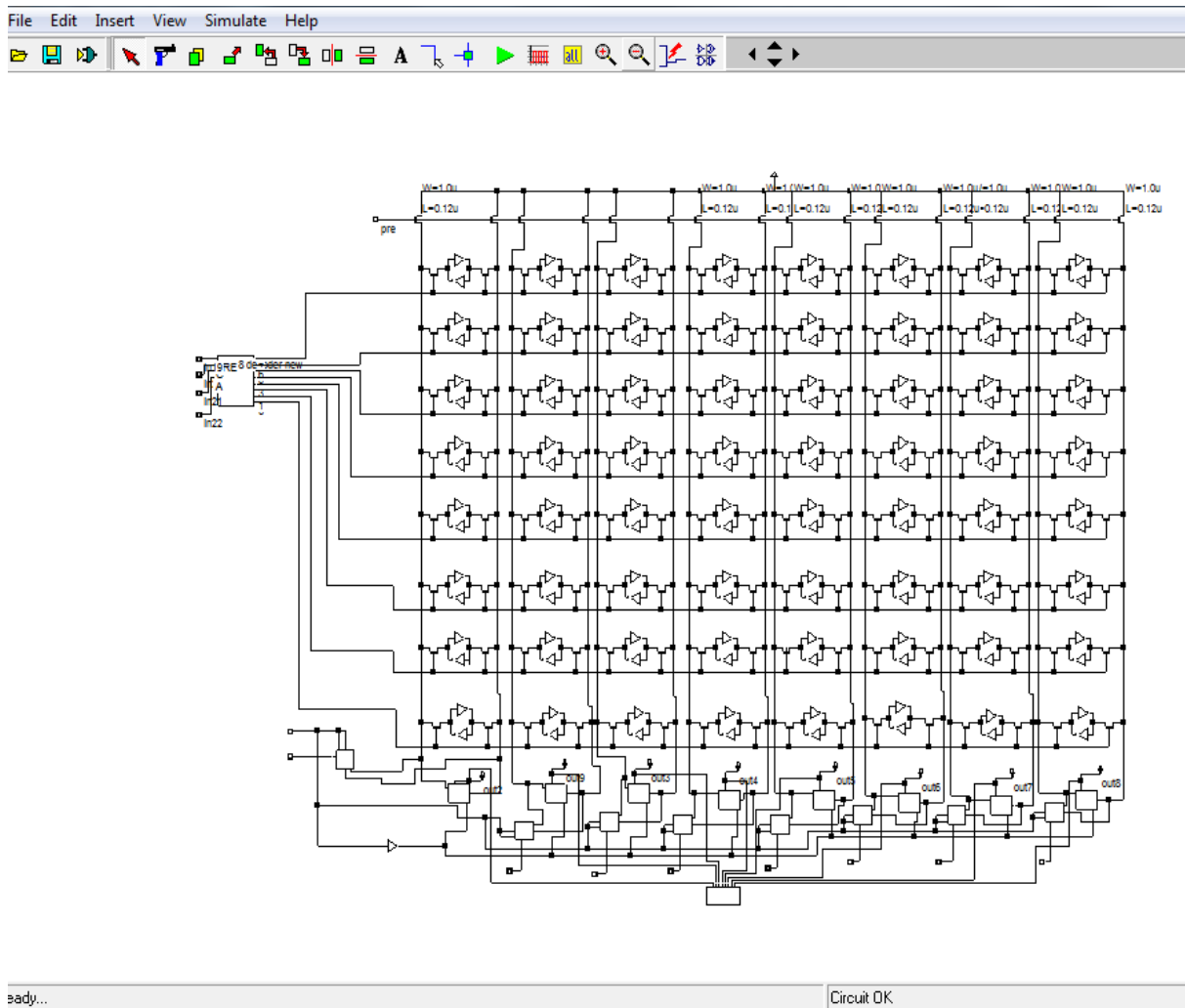


Fig 13. Schematic for SRAM Architecture

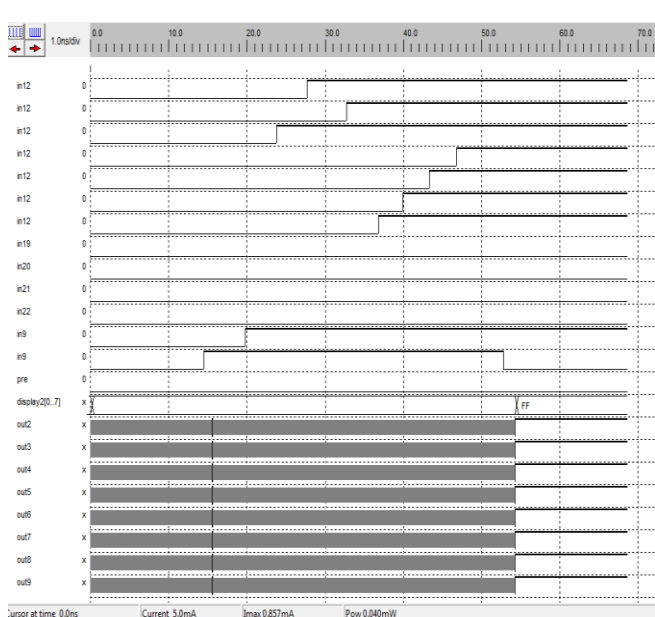


Fig 14. Simulation results for SRAM architecture

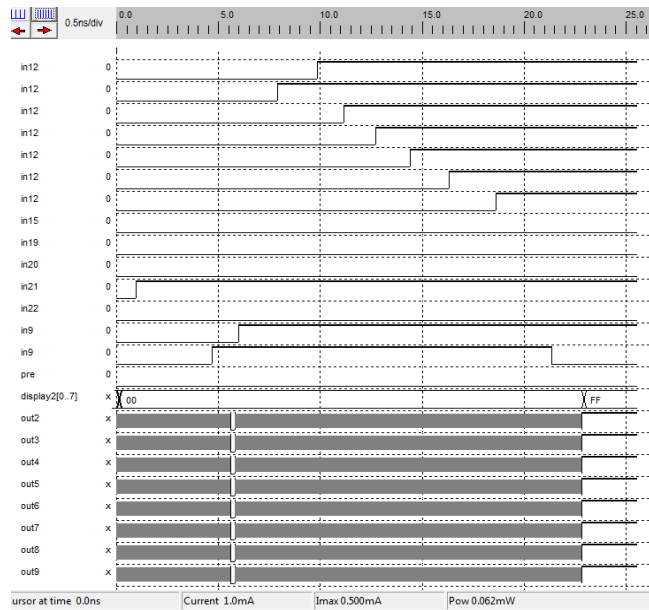


Fig 15. Simulation results for IP-SRAM Architecture



Zoom Out

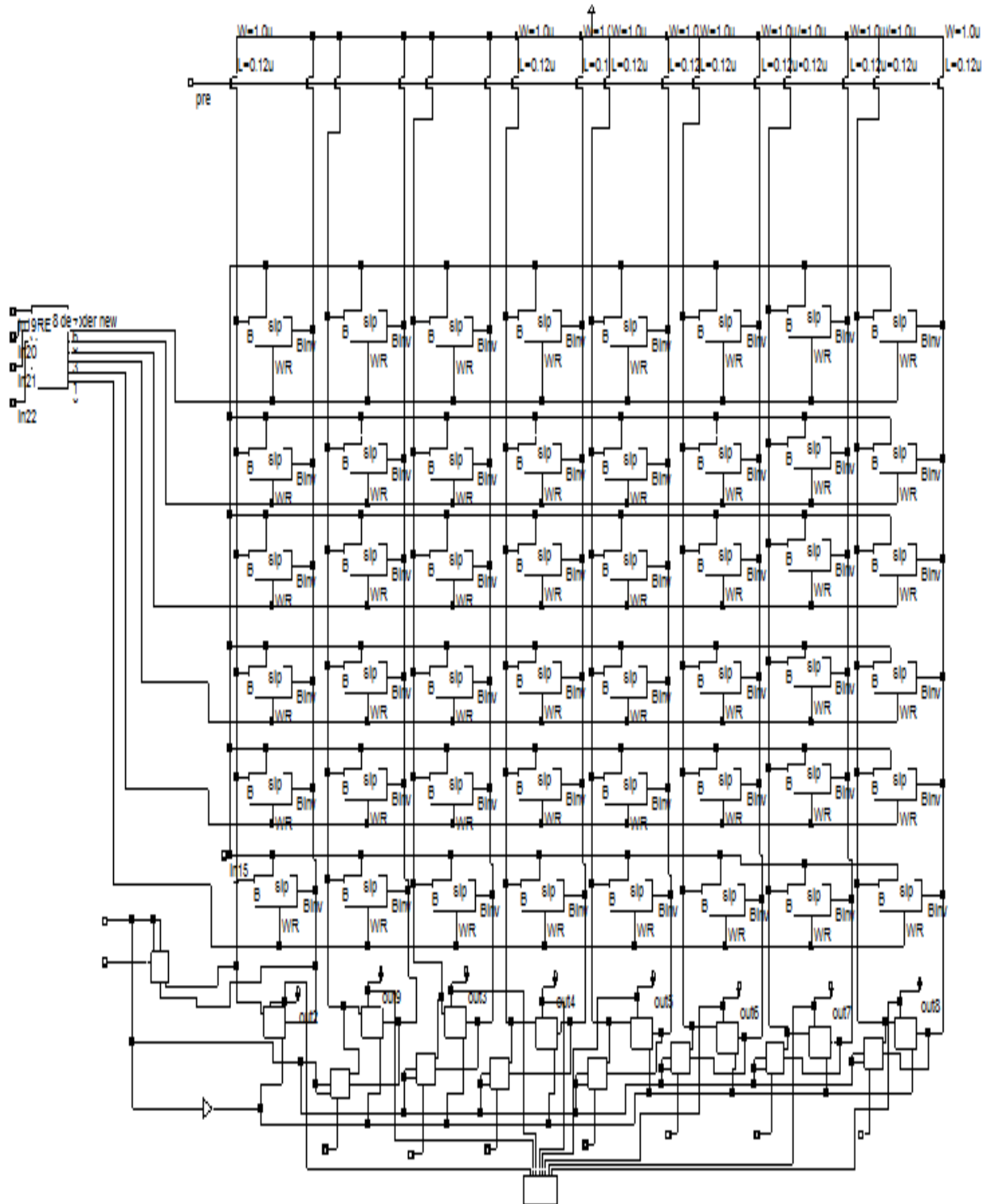


Fig 16. Schematic for IP-SRAM Architecture

VIII. RESULTS

Figure 16 is the Schematic of IP-SRAM Architecture and Figure 15 shows the simulation results of IP-SRAM. From these results it is clear that because of keeping the separate write sub cell and read sub cell the power consumption for IP-SRAM is substantially reduced.

IX. CONCLUSION

In this paper we designed SRAM architecture with IP-SRAM technique to reduce power consumption. In this IP-SRAM technique we have separate read and write operations and we are placing one PMOS device in between pull down network and ground to reduce power consumption. Here the total SRAM architecture was designed using 180nm technology. Hence it is concluded that the proposed SRAM Architecture is used for low power designs and these designed techniques are used for high performance and low power applications.

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