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Power Optimization of High Speed Pipelined 8B/10B Encoder

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Abstract- In this paper a modified 8B/10B Encoder is designed. Power consumption of 8B/10B encoder is reduced by deactivating unwanted switching of the clock. The clock signals are great source of power dissipation. Clock signal is not use to perform any digital computation. it is mainly used for synchronization of sequential circuits. Hence clock signal don't carry any information. So, clock-gating techniques can be used to save power by reducing unnecessary clock activities inside the gate module.

Index Terms- Clock gating, Pipelining, 8B/10B Encoder

I. INTRODUCTION

The demand of consumer is more functionality, energy efficient device and power optimization, power consumption of digital system has become as important as performance VLSI designers spend significant amount of time optimizing their design for minimal power consumption so in order to optimize power eliminating the unnecessary switching of parts of the clock network when there is no function required from that section for some duration. Clock Gating is a power reduction technique that can be used to control power dissipation by Clock net. In synchronous digital circuit the clock net is responsible for significant part of power dissipation up to 15-50%. Clock Gating reduces the unwanted switching on the part of clock net by disabling the clock. 8B/10B encoding technique was developed by A. X. Widmer and Peter A Franaszek in the year 1983. 8B/10B encoder have its application in PCI express, Serial ATA, USB 3.0, Fiber Channel, 33A and many more. The demand of the people is higher transmission speed and bigger capacity. But at high-speed fiber transmission there is a problem of base line offset and unbalance flow of the code. To overcome these problems, the 8b/10b encoder is designed. This is widely used because of its low transmission mistake percent and DC compensation function, also with checking mistake function during the transmission and special function [1]. In this paper, a clock gated design approach is designed for the high-speed 8B/10B encoder, which can lead to the power reduction without complicating the design of encoder. The reminder of the paper is organized as follow. Section II describes the conventional 8B/10B encoder and pipelined 8B/10B encoder. Section III describes the implementation of clock gated 8B/10B encoder. Section IV describes the result and conclusion of our study.

Due to the quick development of communication of technology, fiber communication is most popular now days. The demand of the people is higher transmission speed and bigger capacity. But at high-speed fiber transmission there is a problem of base line offset and unbalance flow of the code. So to overcome these problems, we design the 8b/10b encoder. This is widely used because of its low mistakes at transmission and DC compensation function, also with checking mistake function during the transmission and special function.

8B/10B transmission technique has several advantages First it has a guaranteed transmission of density, which ensures three to eight times transition between one and zero in every 10-bit encoded data sequence, and this is very important for the clock recovery from the transmitted encoded data sequence. Second advantage is 8B/10B is DC balanced code that mean the number of zero and one after encoding process is almost same and no more than five continuous 1's and 0's which avoid DC shifting over time.

Third advantage of 8B/10B is it have 1024 combination of code in the 10-bit sequence after encoding out of which 536 code is effective .so it can be determined where there is a wrong transmission of data by detecting if the received code is an effective or not.

There is a parameter named as Running Disparity, which shows the difference between number of 0's and 1's during the process of encoding. This RD is used to determine the encoded output. When RD=+1 means number of 0's is two more than 1's, and when RD=-1 means the number of 1's is two more than 0's, and if code is perfectly balanced RD is either +1 or -1. 8B/10B encoding codes are according to criterion that the number of 1's and 0's are almost same.[2]

In 8B/10B encoding technique the source 8-bit data sequence is fragmented into two parts, five bits and 3 bits. The higher 3 bits are encoded in to four bit using 3B/4B encoder and lower five bits are encoded in to six bit using 5B/6B encoded. We have 256 input data named as $D_{x.y}$ and 12 control signal named as $K_{x.y.}$ Input data is marked as from higher three bit to lower five bit is H, G, F, E , D, C, B and A . Output encoded 10 bit data is marked as from higher four bit data to lower six bit is j, h, g, f, i, e, d, c, b and a.

We consider initial RD of 8B/10B encoder is negative. If current RD is negative then we choose corresponding result from the RD= -1 column meanwhile it will be checked whether the 10-bit result is perfectly balanced. If it is RD stays the same, otherwise changing RD in to +1. [3]

The reminder of the paper is organized as follow. Section 2 describes the conventional 8B/10B encoder and pipelined 8B/10B encoder. Section 3 describes the implementation of clock gated 8B/10B encoder. Section 4 describes the simulation result and conclusion of our study.

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II. CONVENTIONAL 8B/10B ENCODER

In figure.1 The block diagram of the conventional 8B/10B encoder which have 5 block named as Disparity control, 3B4B/5B6B Coding, 3B4B/5B6B Encoding Switch unit, 3B/10B and 3B/10B coding units are with the functions of converting the 3 bit and 5 bit data in to the 4 bit and 6 bit using combinational logic separately. The result of encoding is under the control of bit K. The encoding switch is made of XOR gate which exclusive-or the output of 3B/10B and 5B/10B encoding unit with disparity control signal C6 & C4

Disparity control unit generates the disparity control signal dispout according to the current disparity of output code CurRD6, CurRD4 and the disparity output of last clock period C6, C4. The block diagram of Disparity control unit is shown in Fig: 2 in the encoder the signal dispk works as the testing signal. The disparity is determine by an outside signal dispin when dispk=1, otherwise it is determined by internal disparity when dispk=O. [4]

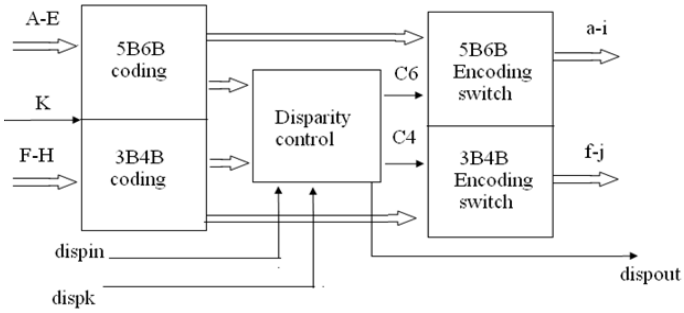

Figure.1: Block Diagram of Conventional 8B/10B Encoder

A. *Pipelined 8B/10B Encoder Design*

In conventional 8B/10B encoder, there is large number of combinational logic. These large numbers of combinational logics introduces a large amount of delay in the critical path, and to achieve high speed the critical path should be shortened. To boost up the speed of encoder, the pipelined 8B/10B architecture is proposed for high-speed serdes.

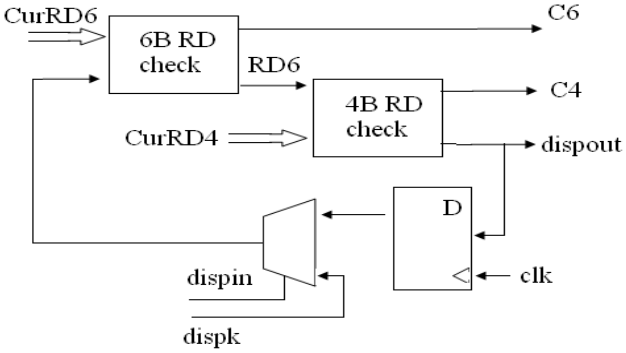

Figure.2: Block Diagram of Disparity Control

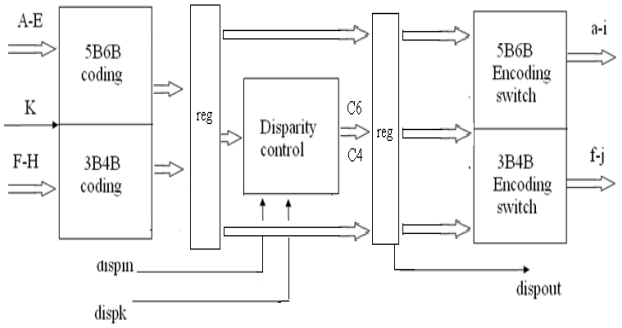

Figure.3: Block Diagram of pipelined 8B/10B Encoder Architecture

In the figure3 the original large combinational logic is broken into two sub logic block by adding two registers. On the one side the data generated from the 5B/10B and 3B/4B encoding block is sent to the registers and then forwarded to the next stage. On the other side C6 and C4 and dispout are generated. This is the result of Disparity Control and also buffered by the registered before they are sent to the next stage. This is because the delay of the disparity control to the output is quite long. Using this proposed pipelined 8B/10B encoder architecture. The combinational circuit is slimed and the critical path is shortened.

III. IMPLEMENTATION OF CLOCK GATED 8B/10B ENCODER

The system clock is connected to clock pin of every flip flop in circuit design, this result in three major components of power consumption. Power consumed by combinational logic whose values are changing on each clock edge. Power consumed by flip flop. Power consumed by the clock buffer tree in the design. [5]

RTL clock gating is the most common technique used for power optimization and improving efficiency and performance. There are three different techniques. RTL clock gating can be classified in three categories. Combinational RTL clock gating, system level RTL clock gating and sequential RTL clock gating. Combinational RTL clock gating technique reduces the power by disabling the clock on register level when output is not changing. The System level clock gating technique disables the clock for the entire the design block, effectively disabling all the function. On the other hand sequential and combinational selectively suspend the clocking while the design keeps producing the output.

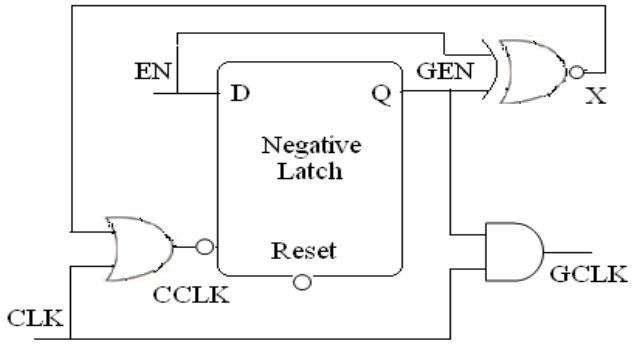

Figure.4: Generation of Gated Clock using Negative Latch

The sequential RTL clock gating without affecting the design functionality changes the RTL micro-architecture. Sequential clock gating is a multi-cycle optimization with multiple implementation tradeoffs and RTL modifications. Gated clock is easily accepted technique to optimize power and can be applied at system level, gate level, RTL. Clock gating can save more power by not clocking the register or memory element if there is no change in its state. Clock continuously consumes power because it toggles the register and their associated logic. So to reduce power consumption clock gating shuts off the clock while system maintaining its current state. One of best available technique is used for clock gating and observation is made during simulation.

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Clock gating technique using negative latch is shown in figure:4 This proposed technique save power in such a way when the target device is 'ON', clock controlling device is 'OFF', and also when the target device is 'OFF', clock controlling device is 'OFF'. In this way we can save more power by avoiding unnecessary switching of the clock net.
When the enable signal EN turn on and at that time the GEN is zero, the XNOR will produce 0 at its output i.e. X=0. This will go to the clock controlling circuit. At the input of Latch there is a OR gate which have global clock and output of XNOR as the input. This logic will generate clock pulse that will drive the Latch when X=0. In the next pulse of the clock GEN become 1 and output of XNOR turn to 1, OR gate give constant high CCLK until EN turn to '0'.

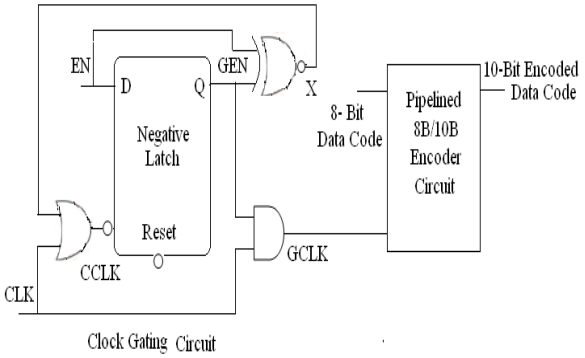

Figure.5: Pipelined 8B/10B Encoder Clock Gated

When GEN is '1', in our second clock generation circuit there is a AND gate, which have global clock and GEN as input, in this case a clock pulse will be generated for the target device when the CCLK is constant that mean latch will hold its state without switching, In figure 5 a clock gated pipelined 8B/10B encoder is shown, unwanted switching of clock is control by the negative latch clock control circuit. [6]

IV. SIMULATION AND RESULT

A. Pipelined Encoder without Clock Gating

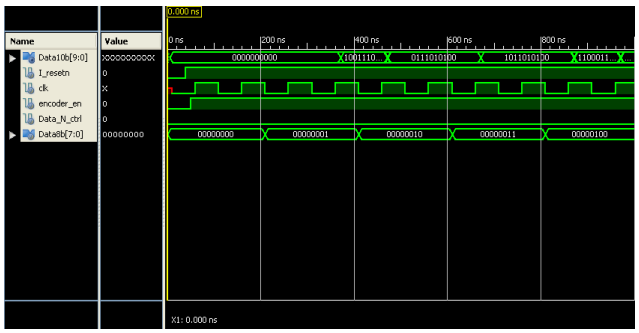

Figure.6: Waveform of Pipelined 8B/10B Encoder

B. Pipelined Encoder with Clock Gating

Figure.8: Waveform of Clock Gated Pipelined 8B/10B

C. Conclusion

In order to evaluate the power reduction obtained by applying clock gating in pipelined 8B/10B encoder, we have evaluated the power consumption in pipelined 8B/10B encoder and power consumption in pipelined 8B/10B encoder with clock gating.

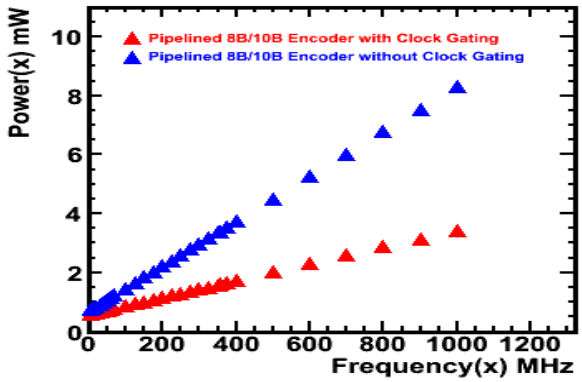

Figure: 9 Clock Power of Pipelined 8B/10B Encoder and Clock Gated Pipelined 8B/10B Encoder

Verilog code of Pipelined 8B/10B encoder was simulated in Xilinx 14.2 ISE Navigator and then Verilog code of Pipelined 8B/10B with gated clock was simulated and synthesized and the Xpower was obtained using Xilinx XPower Analyzer. The results obtained from the Xilinx 14.2 implementation with the device in which, we have generated NCD, PCF, SAIF files after the post simulation. The comparison of power reduction is shown in graph figure 9 between pipelined 8B/10B Encoder and clock gated Pipelined Encoder.

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