An Efficient Design of R-2R Digital to Analog Converter with Better Performance Parameter in (90nm) 0.09-µm CMOS Process

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Abstract— ***CMOS technology favors digital circuitry but imposes a challenge to the analog designer faced with limitations such as process gradients and random device variations. With increasing complexity comes an increase in the number of devices in a system, and hence, an increase in the die size required for that system. As the die space available becomes more and more critical, the need to optimize each function in the system for area consumption. The DAC is optimized for large integrated circuit systems where possibly dozens of such DAC would be employed for the purpose of digitally controlled analog circuit calibration. An R-2R Ladder is a simple and inexpensive way to perform digital – to – analog conversion by using repetitive arrangements of precision resistor networks in a ladder-like configuration. The application of Microwind 3.1 for realizing R2R DAC bridges the gap between theory and the real circuit. This paper provides a detailed view of a 4 bit R2R ladder with optimum accuracy by using Microwind 3.1.This paper describes the design of a DAC which is of contemporary nature with reasonable speed, resolution and linearity with lower power, low area. This paper provides a detailed view of a 4 bit DAC with optimum accuracy by using Microwind 3.1. For all about Pre Layout simulation has been realized using 90 nm (0.09um) CMOS process Technology.***

Index Terms— digital-to-analog converters (DAC),R-2R, DNL, INL, etc.

I. INTRODUCTION

Digital to analog conversion is one of the common functions in modern communications and other mixed-signal systems.Decoding a digitally processed signal into a form that can be played out of a loudspeaker or transmitted by an antenna requires a digital to analog converter (DAC). While DACs have been used since the invention of the digital computer, designers are continuously introducing new and more complex systems in which DACs are needed. [5,6] Data converters, i.e., analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), are interface circuits between the analog and digital domains. They are used in, e.g., digital audio applications, data communication applications and other types of applications where conversion between analog and digital signal representation is required [7]

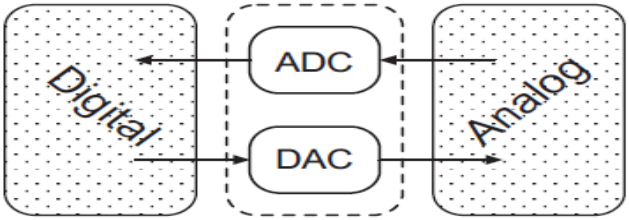

Figure 1.1: Data converters as interface between the analog and digital domain.

An analog-to-digital converter, or ADC, performs the former task while a digital-to-analog converter, or DAC, performs the latter. An ADC inputs an analog electrical signal such as voltage or current and outputs a binary number. The digital data are entered through the 4 lines (D0 to D3) which is to be converted to an equivalent analog voltage (Vout) by the mean of the R/2R resistor network. Commercial Digital to Analog converter ICs are based on the similar principles. [5] The R/2R network is build by a set of resistors of two values, with values of one sets being twice of the other. In all of the circuits sets of 1K and 2K resistors are used, which is near to the R/2R ratio. Accuracy or precision of DAC depends on the values of resistors chosen, higher precision can be obtained with an exact match of the R/2R ratio. [3]

Figure 1.2.Digital to Analog Converter

II. R-2R DIGITAL TO ANALOG CONVERTER

One of the most common DAC building-block structures is the R-2R resistor ladder network shown in Figure 2.1. It uses resistors of only two different values, and their ratio is 2:1. An N-bit DAC requires 2N resistors, and they are quite easily trimmed. There are also relatively few resistors to trim.

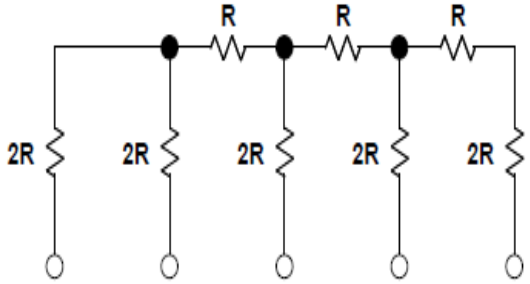

Figure 2.1: 4-Bit R-2R Ladder Network

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The R-2R ladder consists of two different resistors placed in a configuration as shown in fig 4.The inputs to the ladder are fed from a N bit inputs. The input voltages range from 1.2V to 2.5V. This configuration consists of a network of resistors alternating in value of R and 2R. Starting at the right end of the network, notice that the resistance looking to the right of any node to ground is 2R. Each node voltage is related to Vref, by a binary-weighted relationship caused by the voltage division of the ladder network. The total current flowing from Vref is constant, since the potential at the bottom of each switched resistor is always zero volts. Therefore, the node voltages will remain constant for any value of the digital input.

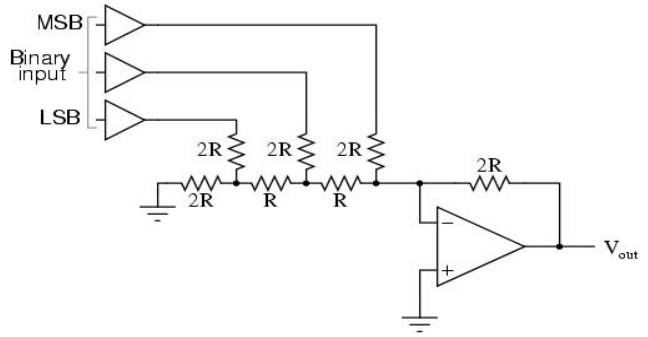

Figure 2.2: 4 bit 2-2R DAC

It is not easy to construct a resistor-based DAC with a high resolution, due to the resistance spread, and the needs for 2N serial resistors. A better choice is the R-2R ladder this configuration consists of a network of resistors alternating in value of R and 2R. For a N bits DAC, N cells based on 2 resistors R and 2R are connected in serial. At the right end of the network is the output voltage "Vout". We used 7 resistors for the 4-bit implementation of the R 2R DAC that is twice less than for the previous R-ladder. The difference is even more significant in the 8-bit circuit, with only 15 resistors, while the simple ladder would require 255 resistors in serial. The digital input (B3,B2 B1 B0) determines whether each cell is switched to ground tied to Vdac through the resistors Each cell's output voltage is a ratio of Vdac because of the voltage division of the ladder network. The final output voltage VOUT depends on the value of B, following the given formula equation (2.1).

$$V_{OUT} = V_{dac} \cdot \frac{(2^N - B)}{2^N} \qquad \text{…….(2.1)}$$

On this principle, table 1 will gives the value of VOUT versus the input code, with Vdac equal to 1.2V.

- Integral Non-Linearity

Due to the non-ideal behavior of switches, process fluctuations and various gradient effects, there exist a small difference between the ideal analog output "Vout_ideal" and the actual analog output "Vout". The deviation of "Vout"from the ideal value "Vout_ideal" is called the integral non-linearity(INL).The normalized integral non-linearity can be given by equation 2.2.

$$INL_i = \frac{Vout_i - Vout_{ideal}}{\Delta V} \qquad \text{…….....(2.2)}$$

where

INLi=the integral non-linearity for input i (Relative error between -1 and 1),Vout_i=the real DAC output for input i (V),Vout_ideal=the ideal DAC output for input i (V),ΔV=ideal voltage step (V)

- Differential Non-Linearity

The difference between two adjacent analog outputs may be significantly different from the theoretical voltage step.This deviation is called the differential non-linearity (DNL). The normalized differential non-linearity includes the voltage step ΔV to get the relative error. Figure 5 illustrates the difference between INL and DNL concepts.

$$DNL_i = \frac{Vout_{i+1} - Vout_i - \Delta V}{\Delta V} \qquad \text{……(2.3)}$$

where

DNLi=the differential non-linearity for input i (Relative error, usually between -1 and 1)

Vouti+1=the real DAC output for input i+1 (V),Vouti=the real DAC output for input i (V)

ΔV=ideal voltage step (V)

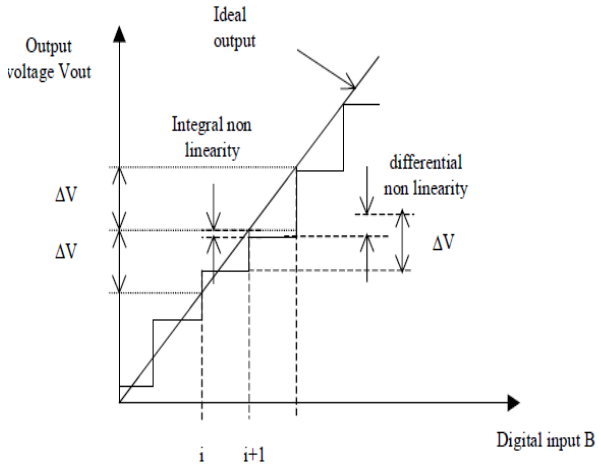

Fig2.3 : The illustration of integral and differential non-linearity

Table 2.1 :VOUT of 4 bit R-2R DAC verses input code B

B3	B2	B1	B0	Vout
0	0	0	0	1.2
0	0	0	1	1.125
0	0	1	0	1.05
0	0	1	1	0.975
0	1	0	0	0.9
0	1	0	1	0.825
0	1	1	0	0.75
0	1	1	1	0.675
1	0	0	0	0.6
1	0	0	1	0.525
1	0	1	0	0.45
1	0	1	1	0.375
1	1	0	0	0.3
1	1	0	1	0.225
1	1	1	0	0.15
1	1	1	1	0.075

III. LAYOUT CONSIDERATIONS

The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area, reduce the fabrication cost, increase operating speed and dissipate less power. Past few years have seen the introduction of nanoscale technologies for industrial production of high performance integrated circuits (IC). Thus we have used here Microwind 3.1 to design and simulate an integrated circuit at physical description level as it is open source software tool for all users which allows to design and simulate an integrated circuit at physical description level (IC). Also The DSCH3.5 program is a logic editor and simulator. DSCH3.5 is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH2 provides a userfriendly environment for hierarchical logic design, and simulation with delay analysis, which allows the design and validation of complex logic structures. Schematic layout of 4 bit R-2R ladder DAC is as shown in Figure 3.1.

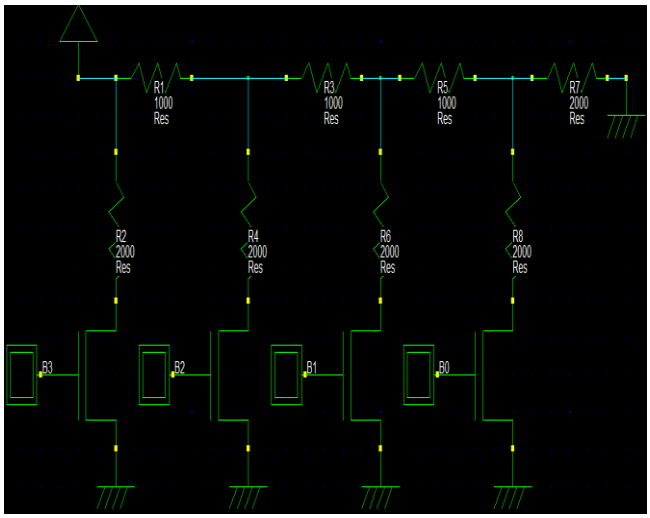

Fig 3.1: The Schematic layout of 4 bit R-2R ladder DAC

The resolution of the R-2R DAC is linked with the accuracy of the resistors and the resistance of the switches which must be negligible to avoid a voltage drop and then some non-linearity. It is important to implement a low Ron switch (Large width, minimum length), together with large R resistors. In order to compensate the Ron resistance of the nMOS device, a dummy switch, whom pass resistance is half Ron, may be inserted inside each cell in serial with R. In figure 6, the design of a four-bit R-2R digital-to-analog converter is reported. The elementary resistor pattern has a value of 500 ohm.The physical layout of R-2R ladder DAC is as shown in figure 3.2.

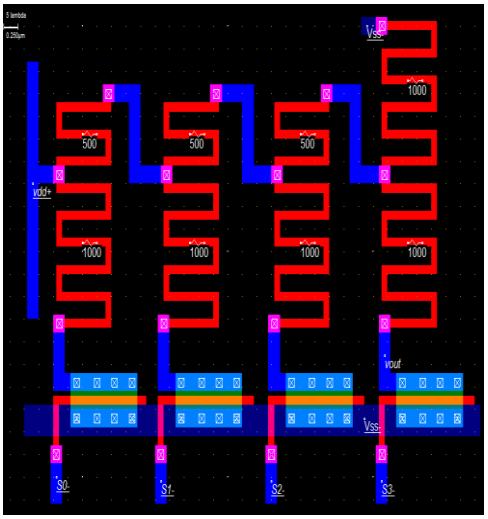

Fig 3.2 : The Physical layout of R-2R ladder DAC

IV. SIMULATION RESULTS

After attempting to design the perfect Physical layout of 3 bit R-2R ladder DAC, with 90 nm (0.09µm) technology and the input given to this converter is from 000 to 111. We have achieve the following simulation result as there are total 16 combinations of input for this DAC ,here below in figure 4.1and figure 4.2 we have shown the behavior of DAC for the any two possible inputs combinations out of 16 i.e. for 0100(B3,B2,B1,B0) and 1000(B3,B2,B1,B0).And after performing simulations using Microwind software tool the various performance parameters get vary according to the type of DAC that we are using. These performance parameters includes power consumption , area, integral non-linearity (INL), differential non-linearity (DNL).

Here we have designed the 3 bit resistor string DAC with 90 nm (0.09µm) technology and the input given to this converter is from 000 to 111. After giving all these inputs one by one we have observed the performance, the following table 4.1 shows the behavior of 4 bit R-2R DAC.

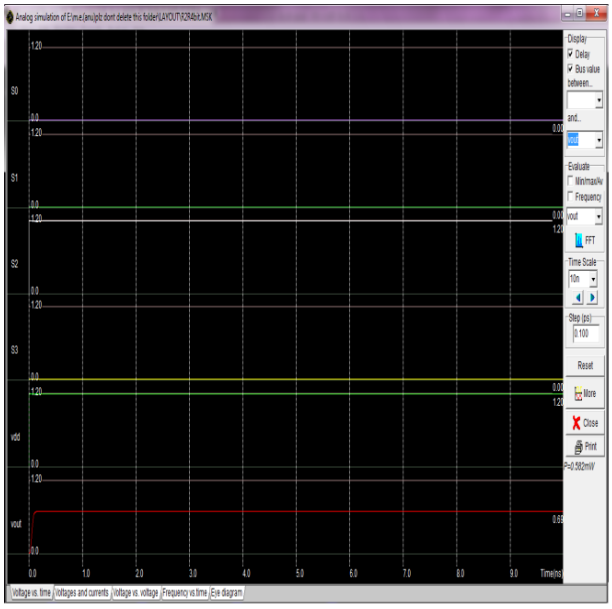

Fig 4.1 : The simulation result of of R-2R ladder DAC for input 0100(B3,B2,B1,B0)

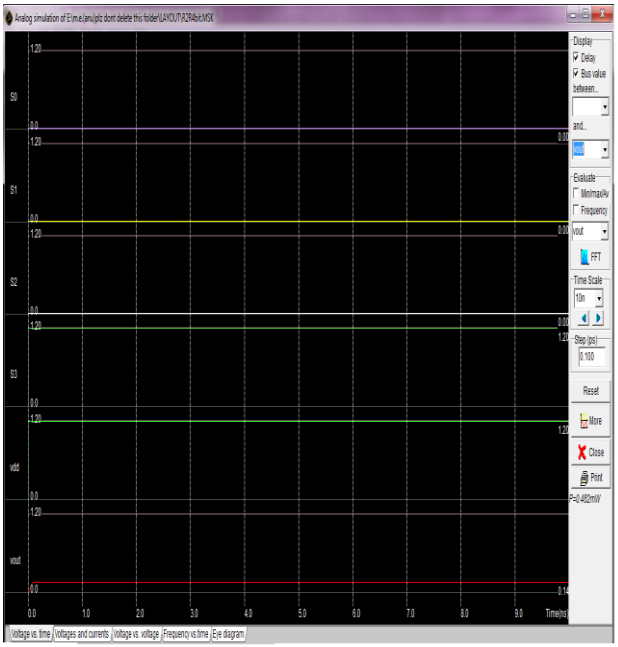

Fig 4.2 : The simulation result of of R-2R ladder DAC for input 1000(B3,B2,B1,B0)

Table 4.1 : Readings of R-2R DAC circuit for all possible inputs

DECIMAL	4 Bit R2R DAC circuit Table of Readings						INL	DNL
	Digital Inputs				Analog o/p Value			
	B3	B2	B1	B0	Theoretical ue V0	Experiment /alue V0		
0	0	0	0	0	1.2	1.2	0	-0.075
1	0	0	0	1	1.125	1.2	0.075	-0.405
2	0	0	1	0	1.05	0.87	-0.18	-0.075
3	0	0	1	1	0.975	0.87	-0.105	-0.255
4	0	1	0	0	0.9	0.69	-0.21	-0.075
5	0	1	0	1	0.825	0.69	-0.132	-0.135
6	0	1	1	0	0.75	0.53	-0.22	-0.075
7	0	1	1	1	0.675	0.53	-0.145	-0.465
8	1	0	0	0	0.6	0.14	-0.46	-0.075
9	1	0	0	1	0.525	0.14	-0.385	-0.115
10	1	0	1	0	0.45	0.1	-0.35	-0.075
11	1	0	1	1	0.375	0.1	-0.275	-0.115
12	1	1	0	0	0.3	0.09	-0.21	-0.075
13	1	1	0	1	0.225	0.09	-0.135	-0.09
14	1	1	1	0	0.15	0.7	-0.080	-0.075
15	1	1	1	1	0.075	0.07	-0.005	

V. CONCLUSION

With an increasing trend to a system-on-chip, DAC has to be implemented in a low-voltage submicron CMOS technology in order to achieve low manufacturing cost while being able to integrate with other circuits. Experiments were performed on 4 bit R2R DAC, the accuracy of theoretical and Microwind 3.1 experimented scenarios are expressed in previous chapter. In this paper 4-bit R-2R DAC simulated in submicron technology, the average power is found to be 1.25 mw with very low area of 41.73 μm^2 with excellent INL and DNL and . From this results could conclude that conversion is performed for all combination successfully and a low-power 4-bit R-2R DAC in a 0.09µm CMOS process with a 1.2 V supply voltage is designed.

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