International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-3 Issue-7, December 2013

Leakage Reduction and Stability Improvement Techniques of 10t Sram Cell: A Survey

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Abstract--Reduction of leakage power is very important for low power applications. Because these high leakage currents are the major contributor of total power consumption of the circuit. This paper explains about various leakage reduction techniques as well as stability improvement techniques of the different SRAM cells. Some of the leakage reduction techniques discussed in this paper are dynamic V_{DD}, multiple V_{th}, SVL (Self- Controllable Voltage Level) and AVL(Adaptive Voltage Level). The stability improvement techniques are word-line adjustment, dual voltage supply, NBL (Negative Bit line) and bit interleaving technique. These techniques are applied on different SRAM cells (6T, 7T, 8T and 10T) and the results are compared. For simulation, MICROWIND 3.1 tool is used.

Keywords—Leakage reduction, write ability, SRAM, leakage power.

I. INTRODUCTION

High leakage currents on SRAM cell are the major contributor of total power consumption as the threshold voltage, channel length and gate oxide thickness. As technology scales down, the supply voltage, gate oxide thickness and channel length must be reduced. In future, the gate oxide thickness may be as low as 0.5nm for CMOS technologies [1]. As a result, the reduction in gate oxide thickness increases gate leakage current. The gate tunnelling current is also predicted to increase at a rate of 500 times per technology whereas the sub-threshold current increases by only 5 times [1].

As a result of high drain voltage and negative gate voltage, field crowding occurs at drain edge causing gate induced drain leakage (GIDL). And also this high drain voltage application to a short channel device results in lowering of barrier height and shifting of point of maximum barrier to the left causing drain induced barrier lowering (DIBL).

If the supply voltage is below the threshold voltage, the process parameters and the variability of the SRAM increase severely [2]. Some of the SRAM stability issues are process-induced device variation, decreasing I_{ON} / I_{OFF} and threshold voltage random variation [3].

Due to increase in V_t fluctuations and process variations, SRAM cell cannot be operated at further scaled supply voltages without functional failures causing yield loss. A low-power 6T SRAM cell [4] shown in fig.1 could reduce access delay and write power but could not improve read stability. A single-ended 6T SRAM cell [5] suffers from write delay.

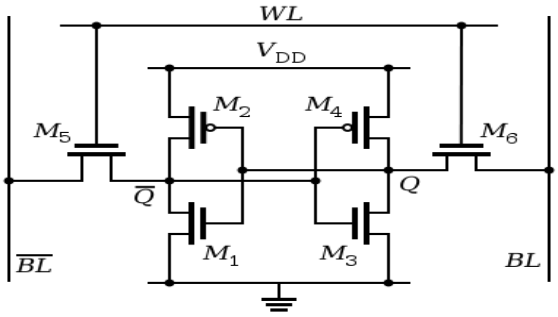

Fig.1. Basic SRAM cell structure

The paper is organized as follows:
Section II explains about various leakage currents occurring in the transistor of SRAM cell. Section III presents various leakage current reduction techniques. Section IV discusses about various techniques used for write ability improvement. Section V presents the simulation results of the proposed techniques. Finally, conclusion is given in Section VI.

II. LEAKAGE CURRENTS ON SRAM

The leakage currents occurring on the SRAM cell are sub-threshold leakage current and gate leakage current, minor amount of DIBL and GIDL.

A) SUB-THRESHOLD LEAKAGE CURRENT:

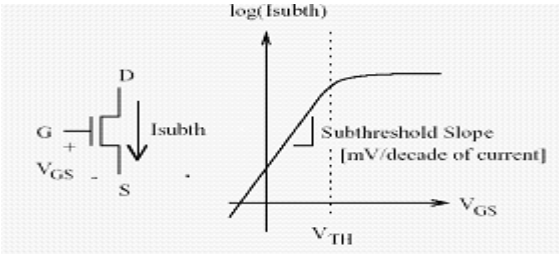

Fig.2. Sub-threshold leakage current of transistor

Manuscript published on 30 December 2013.
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The sub-threshold leakage current occurs between the drain and the source of the transistor. These leakage current occurs when the gate voltage (V_g) is less than the threshold voltage (V_{th}). The curve between gate source voltage (V_{GS}) and the sub-threshold current (I_{SUB}) is shown in fig. 2.

B) GATE LEAKAGE CURRENT:

The sub-threshold leakage occurs only on the standby condition. But, the gate leakage current shown in fig. 3 occurs both on the ON and OFF state.

The technology scaling results in the reduction of gate oxide thickness. This causes a high electric field and tunnelling of electrons between the substrate and gate. And this results in the gate oxide tunnelling current.

If positive bias is applied to gate, tunnelling occurs from substrate to gate. If negative bias is applied, tunnelling occurs from gate to substrate.

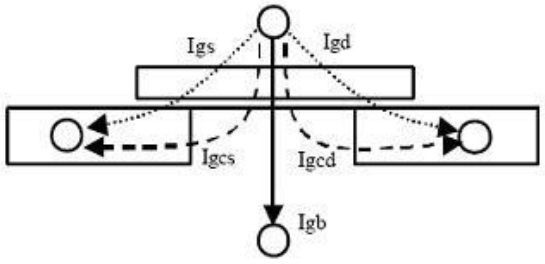

Fig.3. Gate leakage current

C) DIBL:

The source and drain separation is large for long channel devices. In these devices, the V_{th} is independent of the channel length and the drain voltage. But, in the short channel devices, the source and drain separation width is small. And also the V_{th} is dependent on drain voltage i.e, V_{th} varies with the drain voltage. This is referred as Drain induced Barrier Lowering (DIBL).

D) GIDL:

Gate Induced Drain Leakage (GIDL) occurs due to the high electric field occurring in the drain junction of the transistor. It mainly occurs in the OFF state.

The high drain voltage and the negative gate voltage causes field crowding at the drain edge. This process results in gate induced drain leakage known as I_{GIDL}.

III. LEAKAGE CURRENT REDUCTION TECHNIQUES

The various techniques for reducing the leakage current are a) Dynamic V_{DD} b) Multiple V_{th} c) SVL d) AVL.

A) Dynamic V_{DD} Technique:

In the dynamic V_{DD} scheme, normal supply voltage is given to the circuit during the active mode. During standby condition, reduced supply voltage is given. For this process, an extra peripheral circuitry known as the efficiency voltage converter is needed [6]. These reduced supply voltage decreases the leakage current. But the supply voltage reduction, results in low SNM (Static Noise Margin) and data flipping failures.

B) Multiple V_{th} Scheme:

The multiple V_{th} scheme offers both high and low threshold transistors in the same chip which can be used for dealing the leakage problem. The high threshold transistors are used for suppressing the sub-threshold leakage and the low threshold transistor is used for achieving high performance.

The following methods are used for achieving multiple threshold voltages: i) Multiple channel doping ii) Multiple oxide CMOS iii) Multiple channel length iv) Multiple body bias.

C) SVL Scheme:

The SVL (Self controllable Voltage Level) circuit is shown in the fig. 4. The load circuit shown in the fig. 4 can be a SRAM cell.

The basic idea is that when the SRAM cell is in active mode means, the CL is low. And there is no degradation in noise margin. During standby mode, CL is high and reduced supply voltage is given to SRAM cell. This reduces the leakage current and also reduces noise margin.

The drawback of this technique is that it cannot able to reduce the gate leakage current.

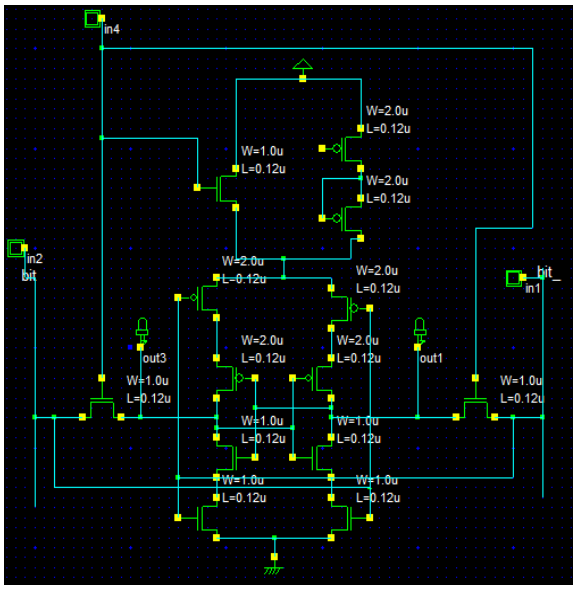

Fig.4. 10T SRAM cell with SVL circuit

D) AVL Scheme:

The AVL (Adaptive Voltage level) scheme reduces the sub-threshold leakage as well as gate leakage current.

In this technique, an AVL circuit is added to the SRAM cell for controlling the effective voltage across it. The AVL switch can be added either at the ground node (AVLG) or supply node (AVLS).

The AVLG circuit will provide 0V at ground node during the active mode and increased voltage during the standby mode [7]. This scheme is similar to that of the diode footed cache design scheme for controlling the leakages in SRAM. In that, a diode is designed with high threshold transistor for raising the ground level in standby mode [8]. The 10T SRAM cell with AVLG circuit is shown in the fig. 5. And the 10T SRAM cell with AVLS circuit is shown in fig. 6.

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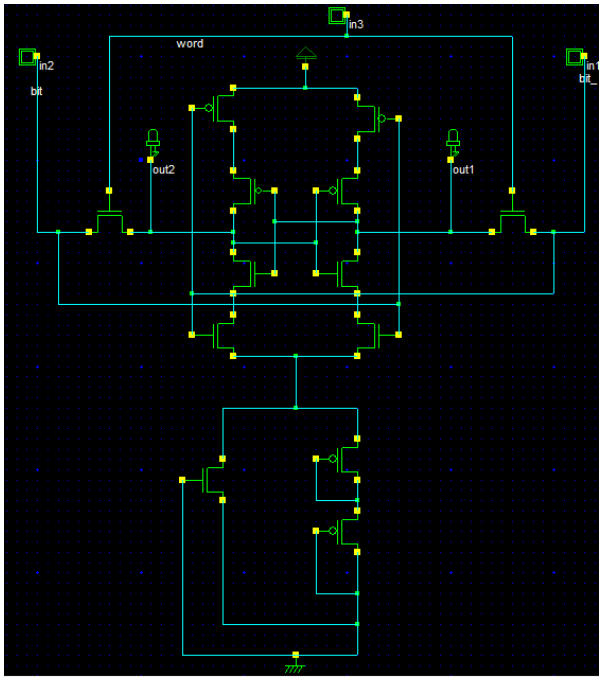

Fig.5 10T SRAM cell with AVLG circuit

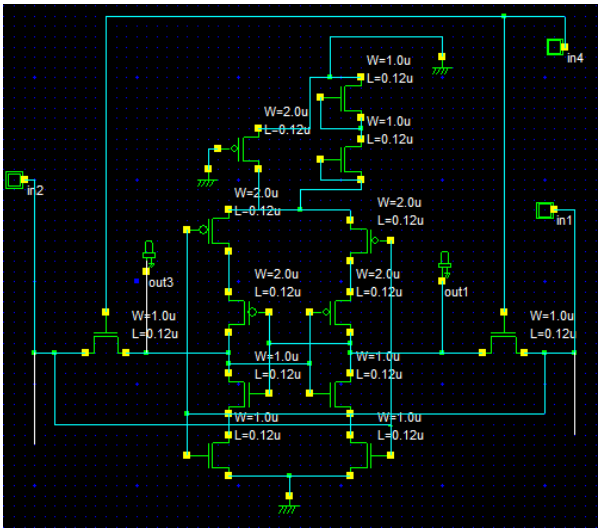

Fig.6. 10T SRAM cell with AVLS circuit

IV. STABILITY IMPROVEMENT TECHNIQUES

The techniques used for improving the write ability of SRAM are a) Word line adjustment b) Dual power supply scheme c) NBL d) Bit interleaving technique.

A) Word line Adjustment:

In the word line adjustment scheme, the voltage level of the WL is lowered than the power line of the flip-flop in SRAM cell. These results in the improvement of SRAM read margin. The circuit for WL voltage adjustment is shown in the fig. 7.

Some of the schemes used for the word line adjustments are i) Replica Access Transistor (RAT) scheme which self-calibrates the WL voltage suppression [9][10], ii) Adaptive voltage level control scheme which is generated from the dual power supplies in the WL driver [11].

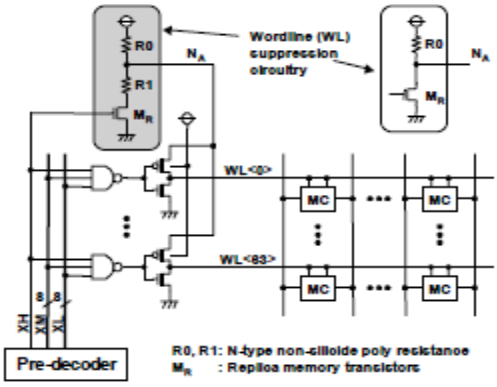

Fig.7. Circuit for WL voltage adjustment

B) Dual Power Supply Scheme:

The technology scaling requires the supply voltage to be reduced in order to reduce the power consumption. But, the lowering of supply voltage results in worsened SRAM stability. In order to overcome this problem, extra power supply was used in many designs [12][13].

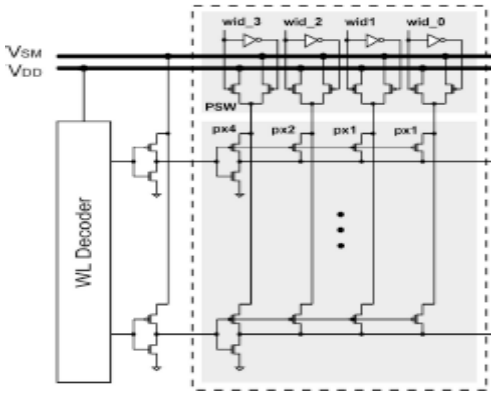

Fig.8 Circuit for dual power supply scheme

In 6T SRAM cell, the cell with higher V_{DD} have better read stability but worsened write stability. In order to improve the write ability, word line compensation technique is combined with dual power supply scheme [11]. Two global power supplies namely V_{SM} and V_{DD} are used in the fig.8.

C) NBL Scheme:

In Negative Bit Line (NBL) scheme, negative voltage is applied to the bit line during write operation for improving the write ability. This negative voltage is generated by capacitive coupling without using any on-chip or off-chip negative voltage source [13]. The main drawback of this scheme is that there is no improvement on the read access and read disturb failures. And it also leads to increase in NBTI (Negative Bias Temperature Insensitivity) variations.

D) Bit Interleaving Technique:

In this technique, the write ability is improved by cutting off the positive feedback loop of the SRAM cross-coupled inverter. In the read mode, an access buffer is used for isolating the storage node from read path for better read robustness and leakage reduction [14].

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The bit-interleaving technique is done by incorporating the SRAM cell with additional word lines namely WWL/WWLb for tolerating the soft errors. The 9T SRAM cell with two word lines WWL/WWLb is shown in fig. 9.

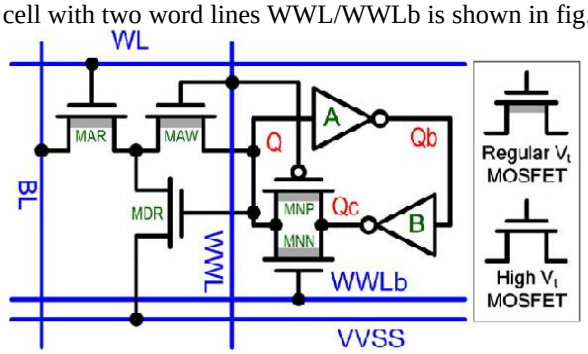

Fig.9. 9T SRAM cell with two wordlines WWL/WWLb

V. SIMULATION RESULTS

The power consumption of the conventional (6T, 7T, 8T and 10T) SRAM cells are shown in the table 1. Simulation results are simulated on MICROWIND under different supply voltages.

Table.1. Power consumption of various SRAM cells

CELL TYPE	VOLTAGE (V)	POWER (W)	CURRENT (A)
6T SRAM	1.2	0.195 m	0.162 m
	0.5	1.452 µ	0.003 m
	0.25	0.030 µ	0
7T SRAM	1.2	0.191 m	0.159 m
	0.5	0.646 µ	0.001 m
	0.25	0.019 µ	0
8T SRAM	1.2	0.426 m	0.385 m
	0.5	1.965 µ	0.004 m
	0.25	0.040 µ	0
10T SRAM	1.2	0.210 m	0.175 m
	0.5	0.926 µ	0.002 m
	0.25	0.023 µ	0

The power consumption of the AVL (AVLG & AVLS) and SVL (SVL lower & upper) techniques is shown in the table 2.

Table.2. Power consumption of 10T SRAM using various techniques

TECHNIQUE	VOLTAGE (V)	POWER (W)	CURRENT (A)
10T with AVLG	1.2	0.141 m	0.118 m
	0.5	0.911 µ	0.002 m
	0.25	0.023 µ	0
10T with AVLS	1.2	0.504 µ	0.005 m
	0.5	0.057 µ	0.001 m
	0.25	0.012 µ	0
10T with SVL upper	1.2	4.699 µ	0.006 m
	0.5	0.144 µ	0.001 m
	0,25	0.030 µ	0
10T with SVL lower	1.2	0.142 m	0.119 m
	0.5	0.835 µ	0.002 m
	0.25	0.024 µ	0

The output waveform of the 10T SRAM cell is shown in fig. 10. In the waveform, three control lines are used namely bit (in1), bit_ (in2) and word (in3) as shown in fig.5. If the in3 is 0, both Q and nQ (out1 and out2) will be zero.

When in3 is 1, in1 is 0 and in2 is 1, out2 will be high and **write operation** is performed. When in3 is 1, in2 is 0 and in1 is 1, out1 is high and **read operation** is performed.

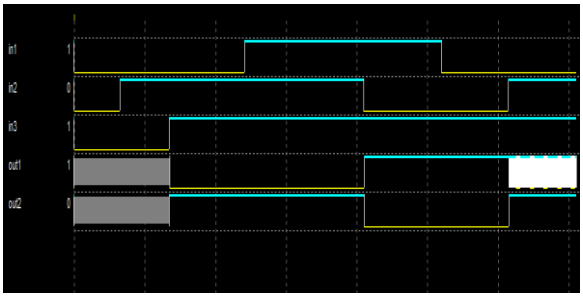

Fig.10. Output waveform of 10T SRAM cell

The layout of 10T SRAM cell is shown in the fig. 11.

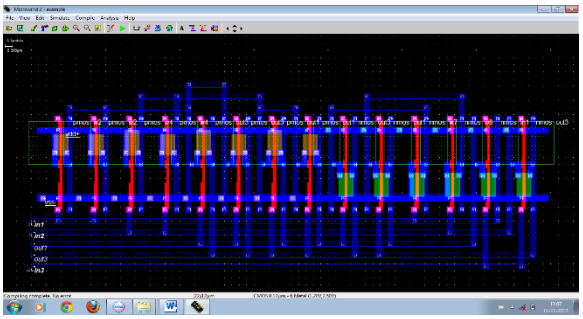

Fig.11. Layout of 10T SRAM cell

The voltage and current waveforms of 10T SRAM cell is shown in the fig.12. The power consumption is about **0.210mW** and average drain current (I_{dd}) is 0.175mA.

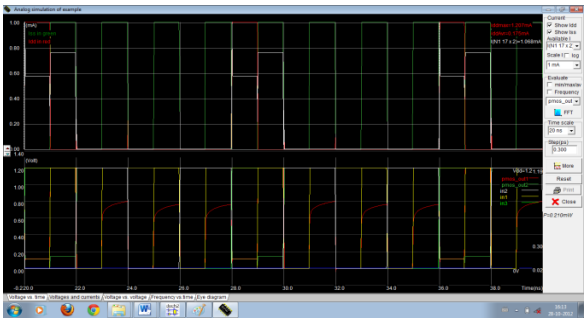

Fig.12. Voltage and current waveforms of 10T SRAM cell

The layout of 10T SRAM cell with AVLG is shown in the fig.13.

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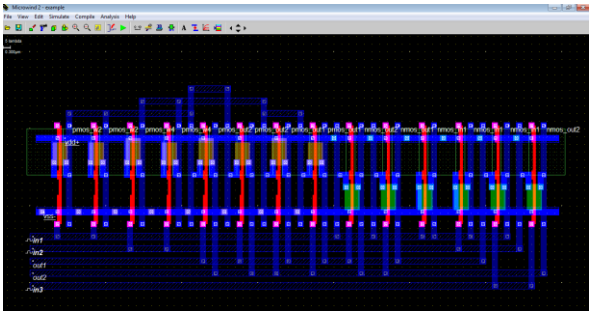

Fig.13. Layout of 10T SRAM cell with AVLG

The voltage and current waveforms of 10T SRAM cell with AVLG is shown in fig.14. The power consumption is about **0.141mW** and the average drain current (I_{dd}) is 0.118mA.

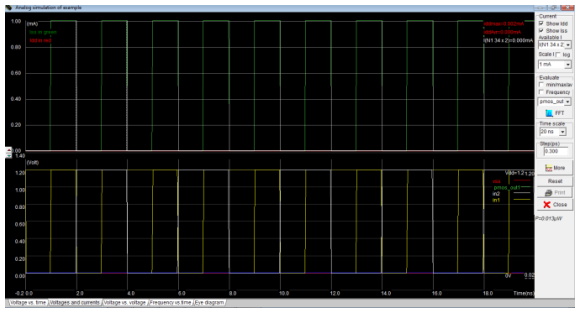

Fig.14. Voltage and current waveform of 10T SRAM cell with AVLG circuit

The layout of 10T SRAM cell with AVLS is shown in fig.15 and its voltage and current waveforms are shown in fig.16. The power consumption is about **0.504µw**. These results show that the power consumption of the 10T SRAM cell reduces much with the AVLS technique compared to AVLG technique. The average drain current (I_{dd}) is also reduced to 0.005mA compared to the conventional SRAM cells.

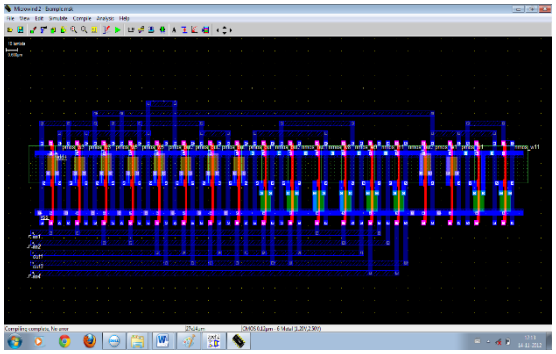

Fig.15. Layout of 10T SRAM cell with AVLS

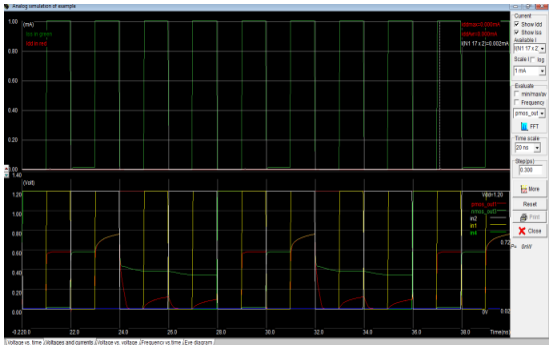

Fig.16. Voltage and current waveform of 10T SRAM cell with AVLS circuit

The voltage vs time waveforms of 10T SRAM cell with SVL lower and upper is shown in fig.17 and 18. The power consumption is about **0.142mW** and **4.699µW** and the average drain current (I_{dd}) is 0.119mA and 0.006mA.

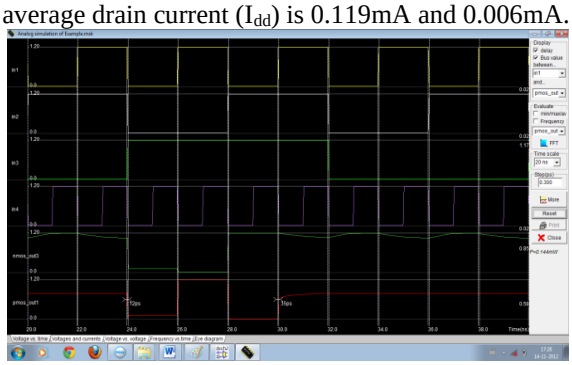

Fig.17. Voltage vs time waveform of 10T SRAM cell with SVL lower circuit

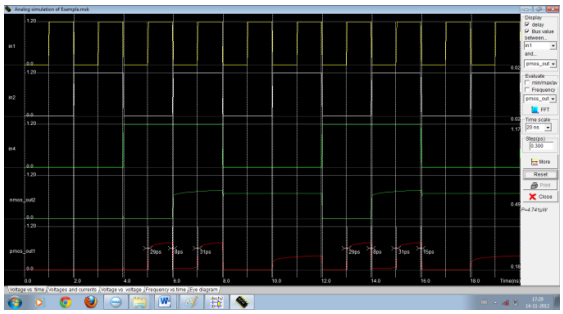

Fig.18. Voltage vs time waveform of 10T SRAM cell with SVL upper circuit

The layout of 10T SRAM cell with SVL lower and upper is shown in fig.19 and 20.

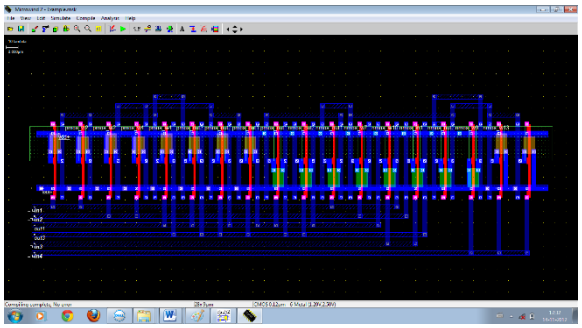

Fig.19. Layout of 10T SRAM cell with SVL lower

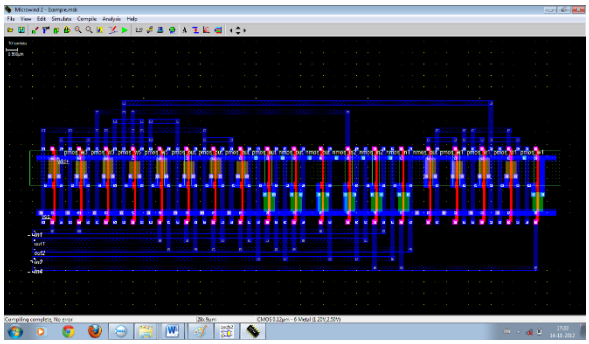

Fig.20. Layout of 10T SRAM cell with SVL upper

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VI. CONCLUSION

Many researches have been conducted on SRAM leakage current reduction and stability improvement. Some techniques focus only on one part of the problem and introduce another problem. The drawbacks of the various techniques are also mentioned in this paper. Of the several leakage reduction techniques discussed in this paper, SVL and AVL techniques show greater leakage suppressing capability. For the stability improvement of SRAM, bit interleaving technique improves both write and read ability of the SRAM in a better way compared to other techniques.

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