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Design and Analysis of Low Offset High Speed Low Power 1Kb SRAM Memory

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Abstract— This paper we present the design and analysis of 1Kb Static Random Access Memory (SRAM) at 180nm technology and main focusing on optimizing power consumption and delay factors are improved by varying the size of transistor used in Sense Amplifier. The present 1kb SRAM can be divided into main three block sense amplifier, basic cell and precharged circuit. Present 1kb SRAM design input decoupled sense amplifier. Presented Sense amplifier CMOS schematic is design tanner EDA S-edit, Simulate T-spice and 0.18µm technology.

Index Terms—Sense amplifier, Driver transistor, Access transistor, load transistor.

I. INTRODUCTION

Memory is an important part of computer and microprocessor based system design. It is used to store data or information in terms of binary number (0 or 1). Also data that is used in program as well as for executing the program are stored in the memory.[19] Since memory is an array type of structure, so cost per bit of the memory decreases with the cell area. For smaller memory cells, we can achieve larger storage capacity in the given silicon area.[19] One of the major issues in the design of SRAMs is the memory access time (or speed of read operation). For having high performance SRAMs, it is essential to take care of the read speed both in the cell-level design and in the design of a clever sense amplifier. Sense amplifiers are one of the most critical circuits in the organization of CMOS memories. Their performance strongly influences both memory access time and overall memory power consumption. High density memories commonly come with increased bit line parasitic capacitances. These large capacitances slow down voltage sensing and makes bit line voltage swings energy-consuming, which result in slower more power hungry memories [5]. Memory is the main and important field of design. Today the size of memory is decreasing and the storing capacity is increasing. As the storing capability is increasing, the response for the data writing and reading from the memory should be very fast. For this purpose different types of sense amplifiers are used. [3]. Sense amplifier the main circuits used in the memory design. There are mainly two types of sense amplifiers and they can be categorized in current mode and voltage mode sense amplifier.

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Current mode sense amplifier detects the current difference between the bit lines and voltage mode sense amplifier detects the voltage difference between the bit lines to determine whether a “0” or a “1” is stored in the memory cell .It amplifies the voltage signal and transfers it on the output circuits. Applications of sense amplifier automotive current monitoring, battery chargers, photovoltaic systems [18].Importance of Sense Amplifier in SRAM memory design is an important circuit to regenerate the bit line signals in a memory design. The sense amplifier can be also applied to the receiving of long interconnection signal with large RC delay and large capacitive load signal. Moreover, the complexity of the differential logic circuit can be enhanced by combining the sense amplifier with differential logic networks to reduce the delay time. However, designing high-speed sense-amplifier circuit is a challenge, particularly for large SRAMs realized in CMOS technology. This is because large memories usually use long bit-lines which present a large capacitive load to the memory cells, thus causing extra signal delay. Sensing and amplifying the data signal which transmits through memory cell to bit lines are the most important capability for a sense amplifier [18].

II. ARCHITECTURE OF MEMORY

Block diagram shown in figure 1 has been designed in Tanner S-edit and some parameters has been observed. For an analog designer, W/L ratio of a transistor is the main factor to achieve the desired objectives. I simulated the design for offset voltage of the bitlines. Offset voltage is the differential voltage developed between the bitlines of a cell. Offset voltage should be low for lower power consumption and higher speed. Another parameter is power consumption during read operation. By optimizing the value of W/L ratio of SRAM cell transistor and sense amplifier, power consumption is improved.

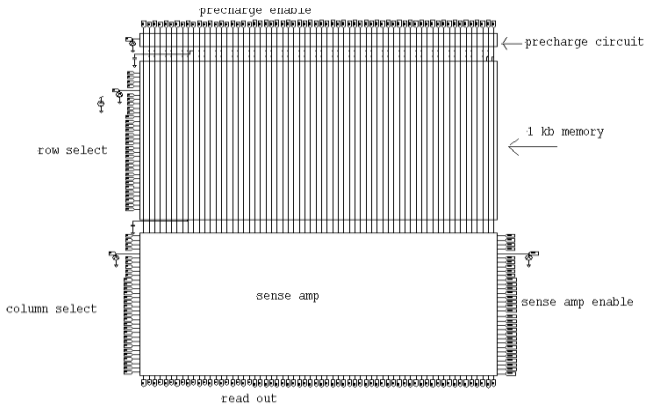

Figure 1 Designed Block Diagram in Tanner S-Edit Tool

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A. *Sense Amplifier*

Transistors MP0, MP1**,** MN0 and MN1 form a cross-coupled complementary structure. The speed and loading characteristics of any cross-coupled sense amplifier depend on the conductivity of the discharging chain and the capacitances of cross-coupled nodes. The higher the conductivity and the lower the capacity can speed an amplifier. Discharge chain of sense amplifier consists of only two n channel transistors MN0 (MN1) and MN2, connected in series and thus satisfies the condition on fast discharging the cross coupled nodes. Moreover, this sense amplifier has two decouple transistors isolate the loading of output nodes because the bit line loading is decoupled from the output nodes and a lot of improvement has been made in the sensing delay. However there still exists a current flow, which is caused by the voltage difference between bit lines and output nodes.

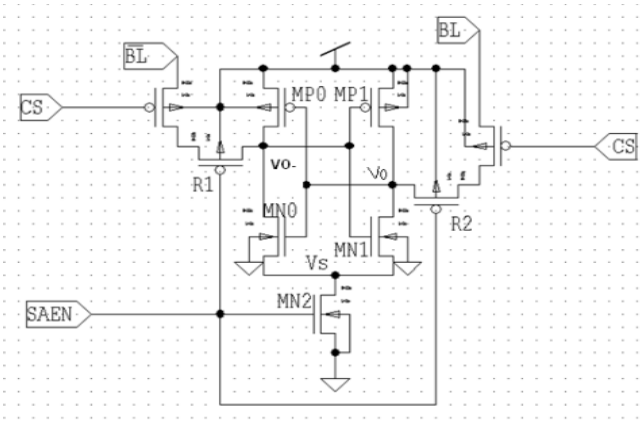

Figure 2: Circuit Diagram of Sense Amplifier

This is one of the commonly used sense amplifier in high speed memory applications. Without loss of generality we assume that BL_ goes down and BL remains high, when the memory cell is accessed. The offset voltage of the latch is characterized as the minimum input differential voltage between BL_ and BL that is required for the correct output of the latch. Ideally the two cross coupled NMOS transistors (MN0 and MN1) and the two PMOS pass transistors (R1 and R2) are perfectly matched. For this ideal case, BL_ can be infinitesimally less than VDD for SAO_ to go down. But due to process variations, perfect matching is not possible, and hence, BL_ needs to be less than VDD by a finite amount for correct reading. This finite value is the offset voltage of the sense amplifier. For the latch output nodes precharged to VDD, mismatch in pull-down NMOS (MN0 and MN1) and input PMOS pass transistors (R1 and R2) contributes to the latch offset. In this thesis, offset contribution from MN0 and MN1 is named as the intrinsic latch offset and that of R1 and R2 as the extrinsic latch offset. The total latch offset is sum of these two offsets. The variations in column pass transistors do not influence the latch offset because column pass transistors remain ON during sensing operation. The pull-up PMOS transistors (MP0 and MP1) do not contribute to the latch offset because they are in subthreshold region during sensing period. It appears that the tail transistor MN2 does not influence the offset, as it is a common mode transistor. But as will be shown in the following discussion, the size of the tail transistor has a significant impact on the latch offset. Also, the rise time of sense enable signal (SAEN), has a very profound influence on both the intrinsic and the extrinsic offset.

B. *Schematic and Working of Basic Cell*

SRAM cell contains two cross-coupled inverters forming latch and the two access transistor connecting these invertors to the complimentary bitlines to communicate with outside the cell. Figure 3shows the schematic of basic cell structure it consists of six transistors. In schematic three types transistor first is access transistor second is driver transistor and third is load transistor. In given below schematic transistors MN5 and MN6 is called the access transistor, the access transistor is the NMOS transistors, As long as the access-transistors are turned off, the cell keeps one of its two possible steady states In both read and write operation common word line signal controls the accessibility to the cell nodes Na and Nb through two NMOS access transistors. Transistor MN3 and MN4 are called the driver transistor and MP3 and MP4 called the load transistor. Vdd supply is 3.3 volt word line is applied to the gates of both the access transistors. Substrate of P channel transistor is connected to the Vdd supply and substrate of N channel is connected to the ground terminal.

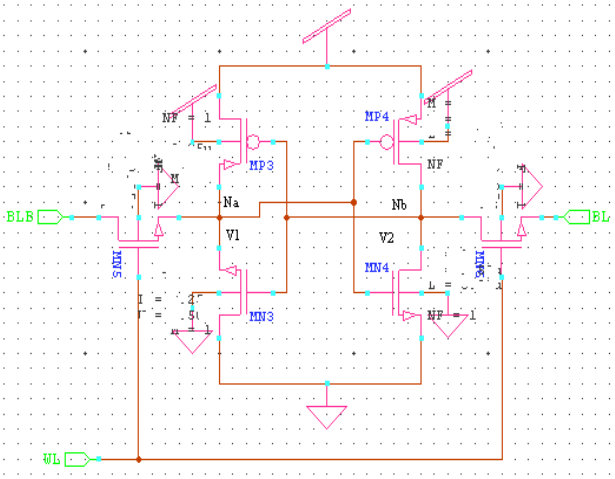

Figure 3 Basic Cell When "0" is Stored (V_2 = 0 v and V_1 =V_{dd})

Working of basic cell we have to assume the previous state of cell. Suppose cell has already store the high data that will result out the node Na has high status and node Nb has the low status, that results out the transistor MP4 & MN3 gets on and MP3 & MN4 gets off. When the data comes to the bit lines of the cell, suppose zero is being placed on the bit line and one is placed on the bit complement line. As soon as the word line goes to high then node Na will discharge through the bit lines and will goes to low status which forces the transistor MN4 to become off and when node Nb goes high it will force MN3 Transistor to gets on. In this way the cell will flip the state from MN3 and MP4 off to MN4 and MP3 gets on. In this way the write operation get performed and after the write operation word lines goes to low status when the word line goes to low the pass transistor gets off and data which is get stored in the cell remains as such as long as the power supply is apply.

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C. Calculation W/L Ratio

First design basic cell schematic than we have to set the W/L ratio of the access, driver and load transistor basic cell design in any CMOS circuit design W/L ratio is important parameter. Basic cell W/L ratio set the two basic criteria consideration which we have taken is given below

i. The data read operation should not be destructive.
ii. Static noise margin should be in the acceptable range.

We take the static noise margin (SNM) consideration to calculate the W/L ratio. SNM is defined as maximum value of noise that can be tolerated by cross coupled inverters before altering the state SNM is very important parameter to design any of the memory cell because it indicate the stability of the cell .

i. Calculation of W/L Ratio of Driver and Access Transistor:

When the data read operation first we assume that the logic"0" is stored in the cell. The voltage levels in the CMOS SRAM cell the beginning of the read operation is shown in the figure 3.In figure the transistor MP3 and MN4 are off and transistor MP4 and MN3 are on. Internal node voltage are V2 = 0 v and V1 =Vdd before the cell access (pass) transistors are turned on After the pass transistor gets turn on by the word selection circuitry the voltage level of the bit complement will not shows any significant variation since no current will flow through MN6. On the other half of the cell MN4 and MN5 will conduct the non zero current and voltage level of the bit complement will begin to drop slightly. because the column capacitance is large so that is why decrease in the column voltage in the bit lines is very small during the read phase in this process voltage V1 will increase slightly from its initial value "0" so if the W/L ratio of the access transistor MN5 is large as compared to the driver transistor MN3 than the voltage V1 may exceed the threshold voltage of the MN4 which will force an unintended change of the stored value. So this is the key design issue, that during data read operation voltage V1 should not be exceed the threshold voltage of the MN3 so that transistor MN3 remains turned off during the read phase so by keeping these thing in mind we calculate the W/L ratio of the transistors which is given below. When the data come than word lines goes high then access transistor will work in saturation region and driver will work in linear region. So to calculate the W/L ratio of driver and access transistor we have to compare the drain currents of both (driver and access) transistor. In the following equation, 5 represents MN5 and 3 representsMN3.The corresponding equation is given below.

Drain current of the access transistor

$I_{d5} = ß_5[(V_{dd} – V_1 – V_{tn})^2]/2$ (1)

Drain current of driver transistor

$I_{d3} = ß_3[2 (V_{dd} – V_{tn}) V_1 – V_1^2]/2$ (2)

As from the circuit $V_1 = V_{tn}$

By putting this value in the above value in equation 1 and 2 We get the given equation

$(W/L)_5/(W/L)_3 = [2(V_{dd} –V_{tn}) V_{tn}]/ (V_{dd} - 2V_{tn})^2$ (3)

Put the following value in equation (3)

$V_{dd} = 3.3$ V

$V_{tn} = 0.6$ V

we get the following value

$(W/L)_5 = 0.7 *(W/L)_2$

Generally from the literature survey we find that the W/L ratio of the driver transistor is generally taken as 3 so W/L ratio of the access transistor is given as

$(W/L)_5 = 0.7 * 3 = 2.1$ (4)

Approximately W/L ratio of the access transistor is = 2

ii. Calculation of W/L Ratio of Load Transistor:

Figure show the schematic SRAM basic cell stored 1.when the Write "1" operation, First method is as usual we have to compare drain current of both the transistor, we assume that logic zero is initially stored in the cell as shown in the figure 3.6 . The voltage level of the CMOS SRAM cell at the beginning of the data write operation is shown in the figure 4.From figure 4, it is clear that transistor MP4 and MN3 will turn on and MP3 and MN4 gets off so it shows that MN5 is operating in the linear region and the MP3 is operated in the saturation region so to calculate the W/L ratio of both the transistor we have to compare the drain current of both the transistor the corresponding mathematical calculation is given below. Here 5 represents MN5 and 3 represents MP3.

Drain current of the access transistor

$I_{d5} = ß_5 [2 (V_{dd} – V_{tn})V_{tn} - V_{tn}^2]/2$ (5)

Drain current of the load transistor

$I_{dp3} = ß_{p3} (0 - V_{dd} – V_{tp})^2 /2$ (6)

We have to put the parameter in the above equation which is given below

$V_{dd} = 3.3$ V

$V_{tn} = 0.6$ V

$V_{tp} = 0.56$ V

Mobility of electron as per the model file $u_n = 446$

Mobility of electron as per the model file $u_p = 155$

By putting the above parameter in the equation we get the following value

$(W/L)p_3/(W/L)n_5 = 1.05$

As we know that $(W/L)n_5$ is 2 so

$(W/L)p_3 = 1.05×2 = 2.1$

Approximately $(W/L)p_3 = 2$

From then above method it is clear the W/L ratio of the load transistor should be 2

So from above calculation we get the parameter of the basic memory cell as

W/L ratio of the load transistor = 2

W/L ratio of the access transistor = 2

W/L ratio of the driver transistor = 3

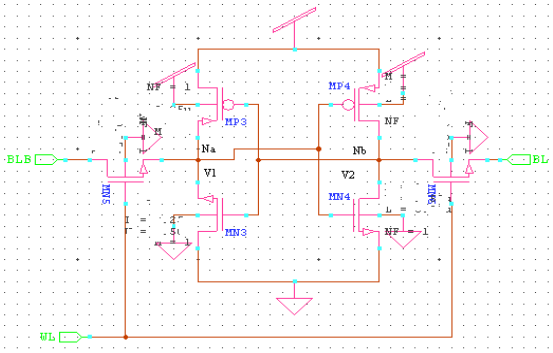

Figure 4: Basic Cell When "1" is Stored ($V_1 = 0$ v and $V_2 = V_{dd}$)

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D. Schematic of Precharge Circuit:

Figure show the precharge schematic circuit Where MN7 and MN8 are the load transistor and MN9 is used to equalize the voltage equally to the bit lines when the equalizing voltage is applied to the MN9 transistor then it precharge the bit lines to half of Vdd.In a read operation, the bitlines start precharged to some reference voltage usually half of the positive supply. When word line turns high, the access transistor connected to the cell node storing a 0 starts discharging the bitline, while the complementary bitline remains in its precharged state, thus resulting in a differential voltage being developed across the bitline pair. SRAM cells are optimized to minimize the cell area, and hence their cell currents are very small, resulting in a slow bitline discharge rate. To speed up the RAM access, sense amplifiers are used to amplify the small bitline signal and eventually drive it to the external world.

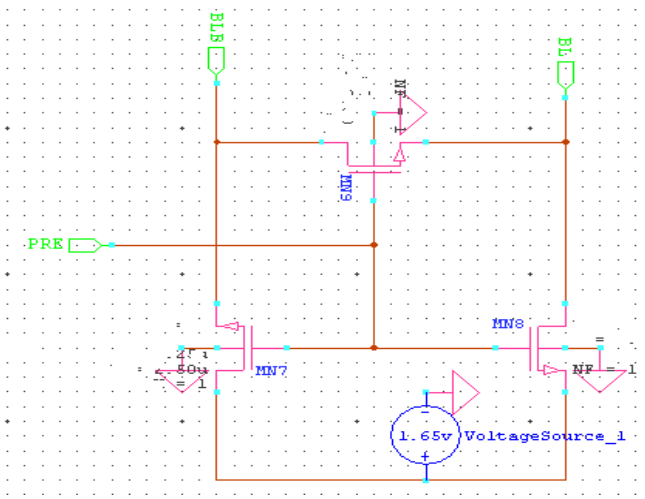

Figure 5: Precharge Circuit

III. SIMULATION RESULT

The waveform shown in Figure 6 output Voltage of Sense Amplifier is simulated using 0.18µm IBM MOS model parameters technology. The figure 6 shows the output voltage of Sense Amplifier. It is to read 1 from memory cell. Output voltage shows the logical 1 i.e. Vdd .Access time of memory is shown in figure below and it is 3 ns. Precharge signal and sense amplifier enable signal also shown in figure.

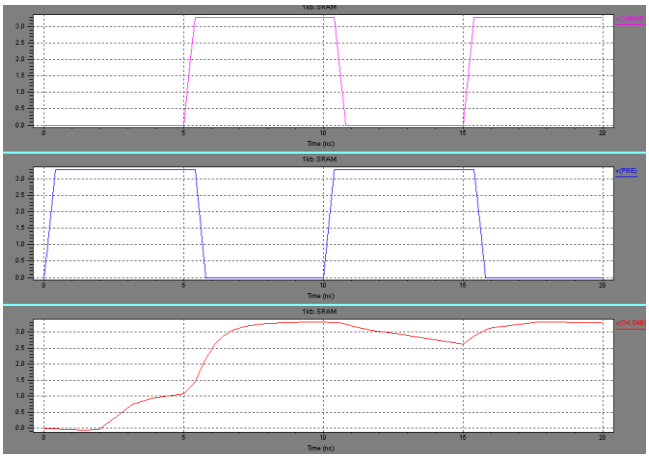

Figure 5: Output Voltage of Sense Amplifier

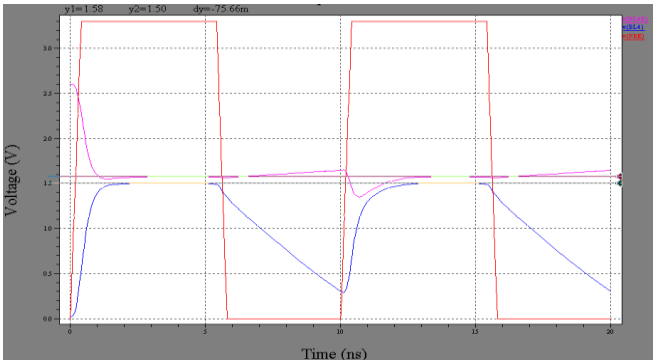

Figure 6: Memory Cell Bit Lines Voltage

The figure 7 shows power consumption during reading operation of the cell.

Power Results

v3 from time 1e-009 to 2e-008

Average power consumed -> 4.167555e-002 watts

Max power 6.213727e-002 at time 5.8e-009

Min power 2.028986e-002 at time 1.97413e-009

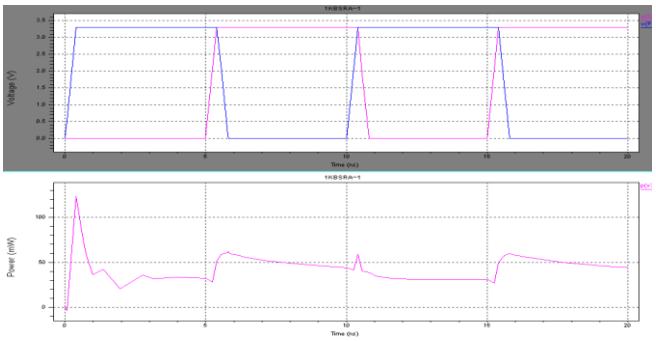

Figure 7: Simulation Waveform Showing Power consumption

The figure 8 shows a read cycle when cell is storing 1.This shows the output voltage and bitline variation during read operation. It also showing the row select WL4 and sense amplifier enable signal SAEN4

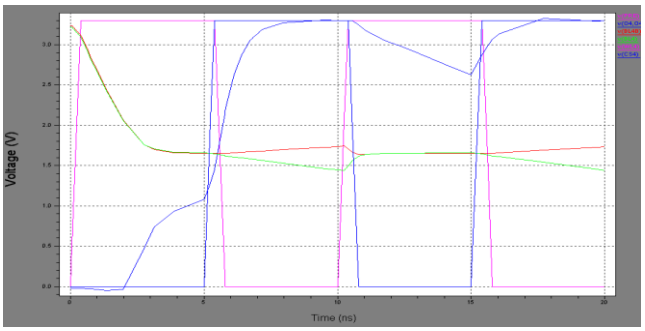

Figure 8: Read Cycle Showing Row Select Signal WL4

By decreasing the size of MN2 in the sense amplifier and increasing the rise time of SAEN signal, the second factor increases but first factor decreases. For large CBL's the decrease in first delay factor can overweigh the increase in second delay factor, resulting in lower total delay.

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The power dissipation in bit lines is (ΔVBL .CBL . VDD) which decrease with decrease in ΔVBL .Thus low offset or low ΔVBL results in low power.

Figure 9 Reduction in Overall Delay and Power Dissipation by Increasing Rise Time of SAEN Signal:

IV. CONCLUSION

In this paper we present a low power high speed Sense Amplifier design for SRAM memory is presented. The power consumption and delay factors are improved by varying the size of transistor used in Sense Amplifier. A 1K SRAM is designed and simulated at 0.18µm technology. The design is implemented in CMOS technology. Power consumption, offset voltage and access time of memory have been observed from simulation result. All results met specifications of the design.

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