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High Performance VLSI Architecture for Braun Multiplier

S.Karunakaran, B.Poonguzharselvi

Abstract: ***The requirement for portable devices with high fidelity should consume less power . Adding two binary numbers is the basic thing in ALU Unit. Adder is an important part of the processor. The complexity of designing the multiplier and ALU changes due to the transistor count. Full adder plays a vital role in signal processing applications, Embedded systems. In the design of fundamental computation units such as multiplier should be included in future applications. Designing VLSI multipliers helps in deriving high end performance architecture which minimizes the consumed power consumption in the architecture. Generally, parallel multipliers are adopted for area optimization and processing speed. 28 T and 20 T full adders are designed which is further utilized for the implementation of Braun multiplier in virtuso schematic of Cadence software 180nm transistor size design.***

Index Terms: Braun multiplier, 3 bit adder, low power

I. INTRODUCTION

In design of future systems low power components are needed. In multipliers and adders, the necessary parameter to be considered is the power consumption or dissipation. In the development of high performance and speed, the design of low power multipliers are essential. Adders plays a crucial role in the synthesis of multipliers. Both multipliers and signal processing units plays an important role in VLSI systems. For generation of partial products Braun multiplier consist ofn-1 carry save adders and a ripple carry adder. Binary digits are added by means of adder which has the capability to save the carry.By adopting the carry save adders and ripple carry adders,products are added parallely, it is essential for speed multipliers.

II. LITERATURE SURVEY

Improvement in power, delay, area has been done in the implementation of Full adder cells by reducing the transistor count. Description about the 28 T and 20 T is given by comparing the simulation results of full adder cells in 180nm technology.

The basic logical equations of full adder Carry(1) and Sum(2) are using to implement the carry save and ripple carry adders.

Carry = A.B +B.Cin+A.Ci (1)

Sum = A.B.Cin+ Carry (A+B+**C**in) (2)

A. Full Adder Using 28 number of transistors:

The circuit and waveform of adder using 28 numbers of transistors is shown in diagram 1 & diagram 2 respectively. It includes 2 inverters, 14 NMOS and 14 PMOS transistors. The NMOS width: PMOS width which is beta ratio is 1:3. According to the ratio, the NMOS width is one-third of the PMOS width.

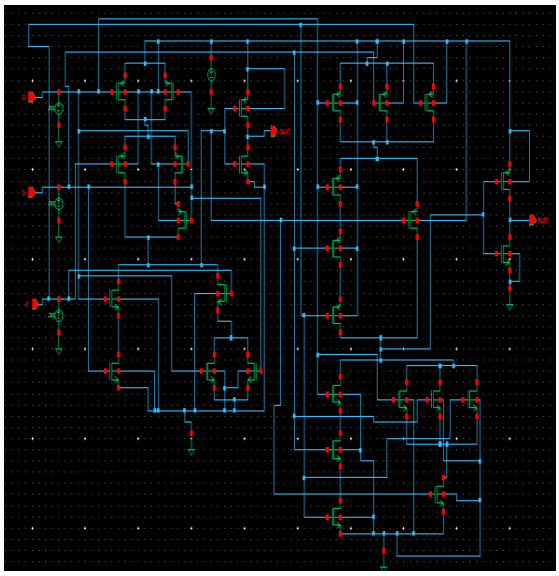

Fig I: Circuit of Full adder utilizing 28 number of transistors

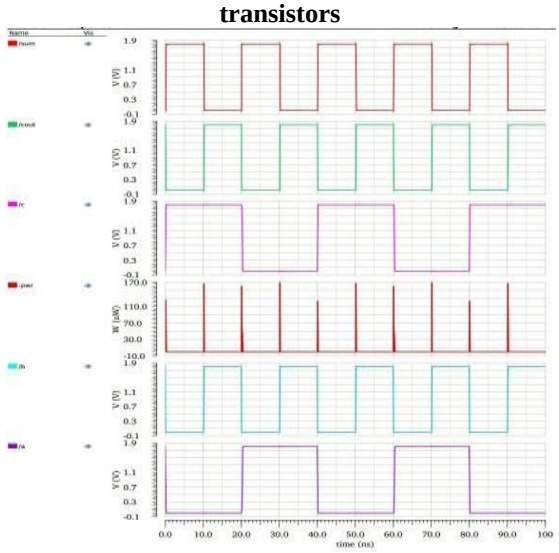

Diagram 2: Output of Adder using 28 number of transistors

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***Correspondence Author(s)**
S.Karunakaran, Department of ECE, Vardhaman College of Engineering, Shamshabad, Hyderabad-501 218,India.
B.Poonguzharselvi, Department of CSE, Chaitanya Bharathi Institute of Technology, Gandipet, Hyderabad-500 075, India

B.Adder Using 20 Number of transistor:

The functionality of Full adder is performed with 20 transistors. It consists of 10 number of transistors of PMOS and NMOS respectively. For this architecture, transmission gates are also utilised. Circuit 3 and Fig 4 shows the circuit and waveforms of Full adder utilizing 20 number of transistors respectively. For the above architecture ,VDD is given as 1.8V.

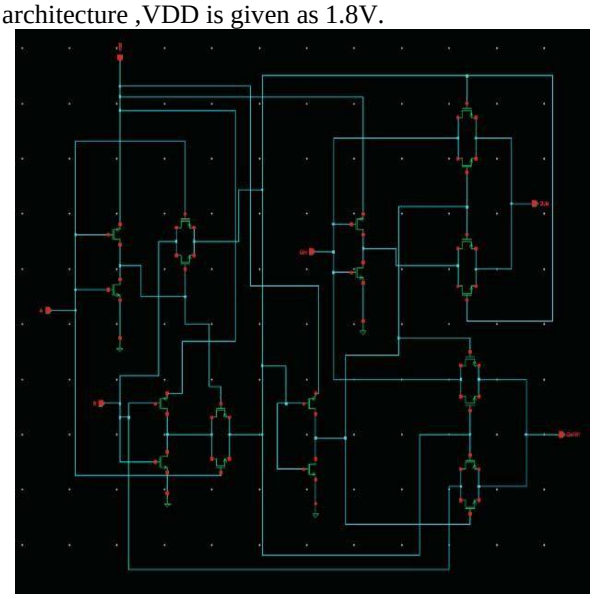

Fig 3 : Circuit of full adder utilizing 20 number of transistor

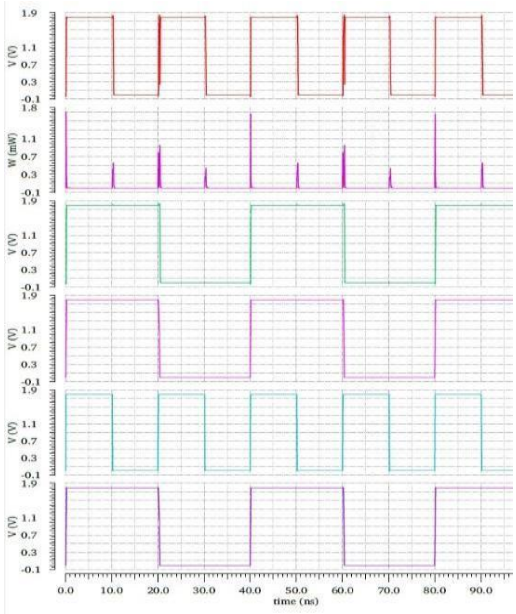

Fig 4 : Output of full adder utilsing 20 number of transistors

C. Comparison of Full adders:

The comparison between Full adders utilizing 20 number of transistors and 28 number of transistors regarding Power dissipation is depicted in the table given below.

Table 1 : Full Adder Power Consumption Details

Full Adders	Power dissipation (in mW)
28-T full adder	0.1204
20-T full adder	0.0454

The schematic shown in Fig 3 consists of transmission gates which gives the thresholding problem. Full adder utilizing 20 number of transistors has little distortions in the output whereas full adder utilizing 28 number of transistors provides distortion free output.

III. PROPOSED BRAUN MULTIPLIER

Braun multiplier has inputs such as multiplicand and multiplier which can be designated as A3 to A0 and B3 to B0. The output of the Braun multiplier has 8 bits which can be designated as P7 to P0.The proposed architecture and the output of the proposed Braun multiplier is provided in Fig 5 and 6 respectively

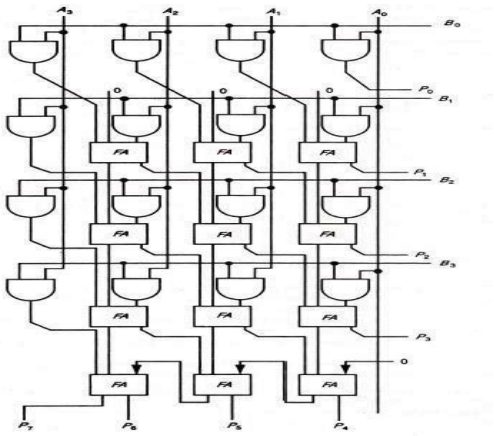

Diagram 5 : Proposed Braun Multiplier of 4 input bits

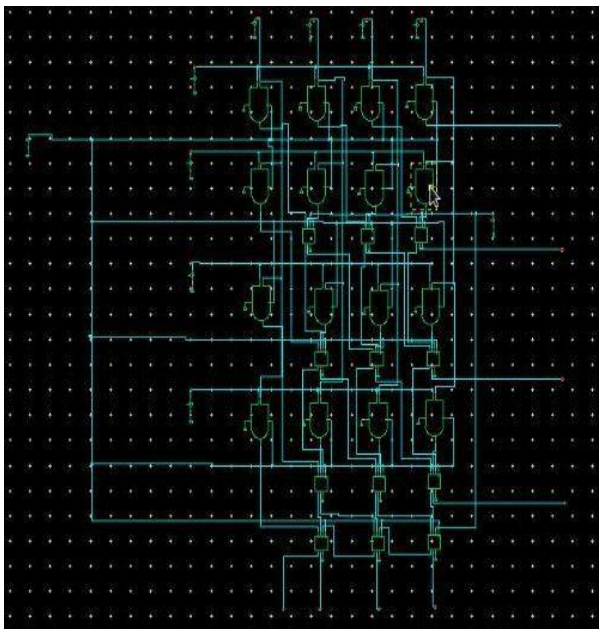

Diagram 6: Architecture of Braun multiplier of 4 input bits

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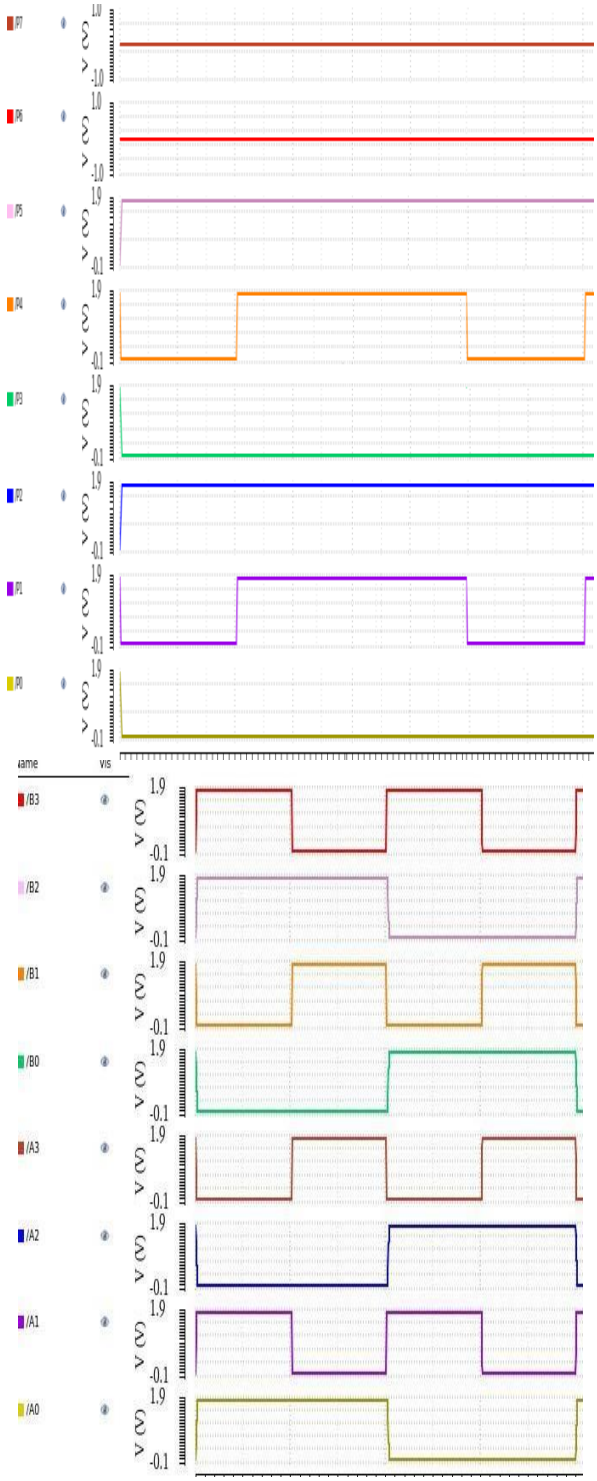

Fig 7: Output of Proposed Multiplier using 4 input bits

B. 8 Bit Braun Multiplier :

8-bit proposed multiplier architecture is having two 8-bit inputs. The proposed multiplier produces 16 digit output. The proposed 8 bit input Braun multiplier architecture and output is depicted in diagram 7 and Fig 8.

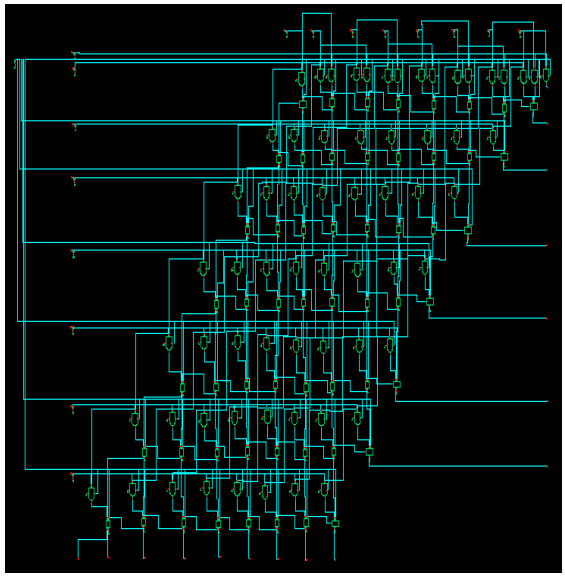

Diagram 7 : Architecture of Proposed multiplier using 8 bit input

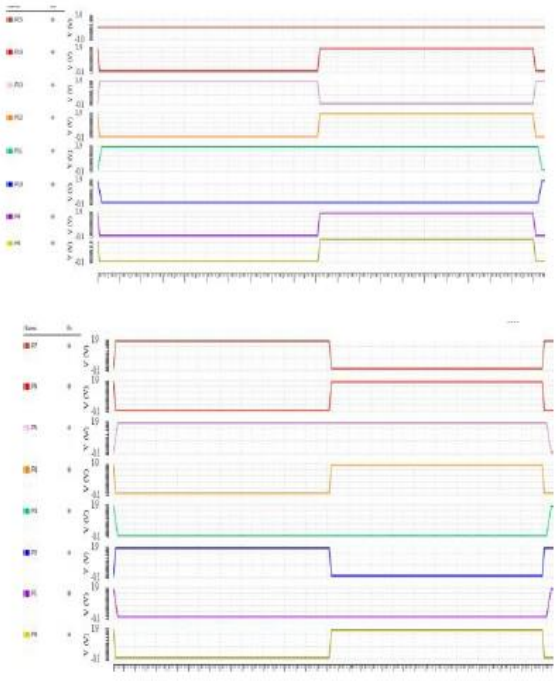

Diagram 8: Output of Braun Multiplication using 8 bit input

Table 2 shows the Comparison of various Braun multipliers in terms of power.The power consumed by the Braun multiplier 28-T Full adders) is more than the power consumed by the 28-T full adders. Individually, the 28-T Full adder consumes more power than 20-T Full adder.

Table 2 Comparison of various Braun multipliers in terms of power

Braun Multipliers	28T power in mW)	20- T (Power in mW)	Amount of Power saved(in mW)
4-bit braun Multiplier	1.24	1.09	0.1552
8-bit Braun Multiplier	0.5124	0.002468	0.5095

IV. CONCLUSION

28 T and 20 T Full adders has been analyzed and comparison of those full adders had been done based on their parameters. From the simulation results, full adder using 28 number of transistors is distortion free .So the proposed multiplier using four input bit and eight input bit is developed using 28 T full adder. These designs could be incorporated in basic computational units for high efficient systems.

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AUTHORS PROFILE

Dr.S.Karunakaran was born in Erode,Tamilnadu,INDIA,in the year1980. He received the Bachelorof Engineering degree in Electrical and Electronics Engineeringfrom the Periyar University, Salemin 2002 and the Masterof Engineering degree in VLSI designfrom the Anna University,Chennai, in the year 2002 . He obtained his Ph.D.degree with the Department of Electronics and Communication Engineering, Anna University Chennai in the year 2015. Presently, he isworking as a Professor in the department of ECE in Vardhaman College of Engineering, Hyderabad.His research interests includeVLSI design, ASIC design, Low power VLSIdesignetc.

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S**mt. B. Poonguzharselvi** was born in Erode, Tamilnadu, INDIA in the year 1989.She received the Bachelor of Engineering degree in Computer Science and Engineering from Anna University, Chennai in 2010and the Master of Engineering in Computer Science and Engineering from the Anna University,Chennai ,in the year 2012.Presently,she is working as a Assistant Professor in the Department of CSE in Chaitanya Bharathi Institute of Technology, Hyderabad.Her research interests includedata structures, DBMS, C programming, Java Programming etc.in Chaitanya Bharathi Institute of Technology, Hyderabad.Her research interests includedata structures, DBMS, C programming, Java Programming etc.

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