# Electrical Characteristics Assessment on Heterojunction Tunnel FET (HTFET) by Optimizing Various High-κ Materials: $HfO_2/ZrO_2$

**Ritam Dutta, Nitai Paitya**

***Abstract*: In this paper, DC performance of double gate tunnel field effect transistor with heterojunction has been assessed by various III-V compound semiconductor materials using 2-D Technology Computer Aided Design (TCAD) simulations. Different hetero high-κ dielectric materials like $HfO_2$, $ZrO_2$ have been incorporated to achieve better electrical characteristics, viz. high ON-state current drivability, improved switching ratio and high tunneling probability. In this work, lower band gap materials have been used as hetero gate dielectric to enhance mobility using band to band tunneling (BTBT), transconductance and steeper subthreshold-slope. The heterojunction TFET (HTFET) then incorporated with various hetero dielectrics (high-κ and low-κ combination), where the $ZrO_2$ – $SiO_2$ combination of dielectric having thickness of 2 nm both in front and back gate, attains maximum value of $I_{ON}$ as 1.522 × $10^{-5}$ A/μm. The subthreshold swing (ss) has also been recorded best as 23.93 mV/dec in comparison with conventional homo dielectric i.e. $SiO_2$-$SiO_2$ oxide throughout the 50 nm channel of HTFET as 34.22 mV/dec, can serve as better alternative tunnel FETs in low power logic applications.***

***Index Terms*: DC Performance, Heterojunction Tunnel FET (HTFET), High - κ dielectric, Subthreshold swing, 2-D TCAD, Band-to-band tunneling (BTBT).***

## I. INTRODUCTION

The conventional metal oxide field effect transistors (MOSFETs) face a real threat in power dissipation due to continuous scaling from micrometer to nanometer regime. Since reducing the sub-threshold swing (*SS*) is one way to reduce the power dissipation i.e. reducing the device leakage current for the same threshold voltage. As conventional MOSFETs have theoretically limited sub-threshold swing of 60mV/dec at room temperature, therefore an additional current controlling mechanism like band to band tunneling (BTBT) is introduced. Due to steep subthreshold slope and less leakage current the tunnel field effect transistors (TFET) with BTBT mechanism consume less power [1-3].

Low drain (ON-state) current and the ambipolarity have been the major limitations in tunnel FET. To improve these limitations, the drain current equation can be written as:

$$I_D \propto \exp\left[-\frac{4\sqrt{2m^*}E_g^{*3/2}}{3|e|\hbar\left(E_g^*+\Delta\Phi\right)}\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}t_{si}}\right]\Delta\Phi \quad (1)$$

Where $m^*$ is the effective mass, $E_g$ is the material bandgap, ΔΦ is range of energy over which the tunneling can occur, $e$ is an electron charge, $t_{ox}$ and $t_{si}$ are oxide and silicon film thickness, $\varepsilon_{ox}$ and $\varepsilon_{si}$ are the dielectric constants. $\hbar$ is the plank's constant [4-6]. Equation (1) shows that the tunneling current in a TFET can be raised by introducing a low band gap material. However, generally after employing a low band gap material throughout the tunnel FET body, the ON-state drain current increases as well as the off-state leakage current. To reduce this leakage current further source side doping concentrations, need to be raised compared to the intrinsic and drain region of the device for n-type TFET [7-9].

It has also been observed that the effective bandgap in a heterojunction can be significantly lower than the bandgap of the fundamental materials [10]. Therefore, the ON-state current ($I_{ON}$) in a heterojunction TFET (HTFET) can be higher than the ON-state current in homojunction TFET structures.

To address the issues of very less $I_{ON}$ and ambipolarity, various high-κ dielectric constants are used in dual gate TFET structures [11-12]. To boost the device mobility, high energy bandgap material like *Si* is replaced by lower energy bandgap materials, e.g., *Ge* [13-16]. Heterojunction tunnel FET with double gate uses the work-function engineering to upgrade the device performance up-to larger scale [17-19]. Several techniques to control the ambipolarity [20-21] have been studied. A non local BTBT tunneling model is used for device simulation process.

In this paper, a thorough investigation on electrical characteristics, viz. high ON-state current drivability, improved switching ratio, transconductance and subthreshold swing are performed on *Si*/*Ge* heterojunction tunnel FET (HTFET) by optimizing various high-κ dielectric materials. The simulations are carried out by using 2-D TCAD.

## II. DEVICE STRUCTURE & SIMULATION

### A. Device Specification

The proposed heterojunction tunnel FET (HTEFT) with *Si*/*Ge* material is designed, where in low bandgap material *Ge* is used in the intrinsic channel sandwiched between the source and drain region made of *Si*. The gate length of our proposed double gate tunnel FET structure is 50 nm, the body thickness ($t_{si}$) is 10 nm and the device oxide thickness ($t_{ox}$) for both front and back is of 2 nm each.

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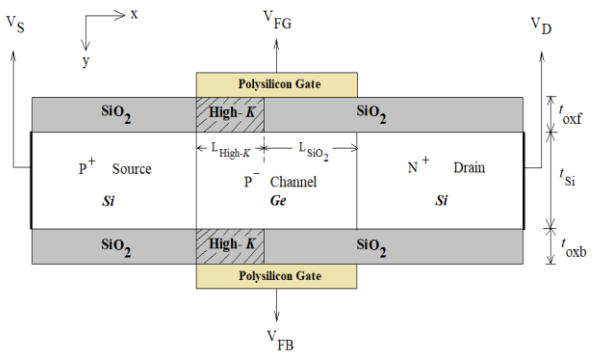


**Fig. 1. The 2-D Structure of Double Gate Heterojunction TFET with High- κ materials.**

Figure.1 shows the proposed Tunnel FET with heterojunctions and hetero gate-dielectric materials. The low bandgap *Ge* channel boost the carrier transportation compared to homojunction structures.

The high-κ materials like $HfO_2$, $ZrO_2$ has been employed in the gate oxide of the source region. Whereas, the gate oxide on the drain region is composed of a low-κ material such as $SiO_2$ [11]. This asymmetric gate dielectric design encourages local minima at conduction band edge of tunneling junction. This further improves the ON-state current ($I_{ON}$) and also improves subthreshold swing in this proposed double gate HTFET compared to conventional Tunnel FET that has same oxide material all over the gate region.

Our proposed heterojunction TFETs (HTFET) are designed by varying the typical device and electrical parameters shown in Table 1 validated by recent literature [22].

**Table.1.** Typical Parameters of Heterojunction Tunnel FET (HTFET) Structures.

| Parameters | Double Gate TFET with *Ge* channel [22] | Our Work |
|---|---|---|
| Gate length /Intrinsic channel length ($L_{ch}$) | 50 nm | 50 nm |
| Length of $SiO_2$ ($L_{SiO2}$) | 30 nm | 30 nm |
| Length of High-κ ($L_{high-\kappa}$) | 20 nm | 20 nm |
| Front gate oxide thickness ($t_{oxf}$) | 2 nm | 2 nm |
| Back gate oxide thickness ($t_{oxb}$) | 2 nm | 2 nm |
| Silicon film thickness ($t_{si}$) | 10 nm | 10 nm |
| $P^+$ source doping concentration | $1 \times 10^{20}$ $cm^{-3}$ | $1 \times 10^{20}$ $cm^{-3}$ |
| $N^+$ drain doping concentration | $1 \times 10^{17}$ $cm^{-3}$ | $1 \times 10^{17}$ $cm^{-3}$ |
| Intrinsic doping concentration | $1 \times 10^{15}$ $cm^{-3}$ | $1 \times 10^{15}$ $cm^{-3}$ |
| Gate work-function ($\phi$) | 4.8 eV | 4.8 eV |
| Gate voltage ($V_{GS}$) | 1 V | 1V |
| Supply voltage ($V_D$) | 1 V | 0.5 V |

## B. Simulation Framework

The proposed HTFET with various high-κ materials are designed with Synopsys TCAD device simulator. The results have been thoroughly compared and analyzed. In this work, for taking the recombination effects into the account, the Shockley Read Hall (SRH) model is used [23]. High electric field velocity saturation is modeled using field-dependent mobility model (FLDMOB). For higher doping concentration structures the Band Gap Narrowing (BGN) model has been used. The non local band to band tunneling (BTBT) model is applied for tunneling in lateral direction.

# III. RESULTS AND DISCUSSIONS

## A. Band Diagram Analysis

The comparative analysis of energy band diagram depicts the ballistic approach of carriers tunneling through the thin barrier width for the double gate heterojunction tunnel FET. The BTBT tunneling can be observed in the figure 2 and figure 3 shown below.

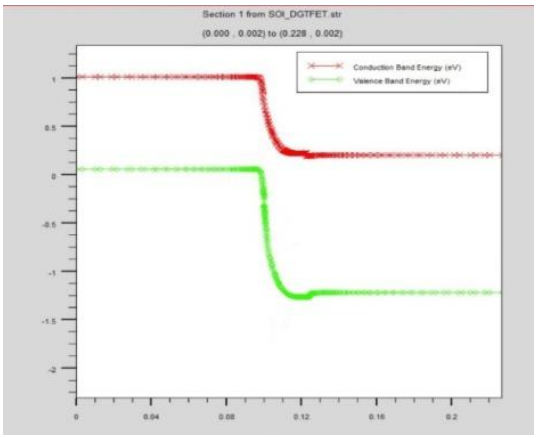


**Fig. 2. Energy band diagram of Double Gate Heterojunction TFET in OFF-state when $V_{GS} \leq 0V$**

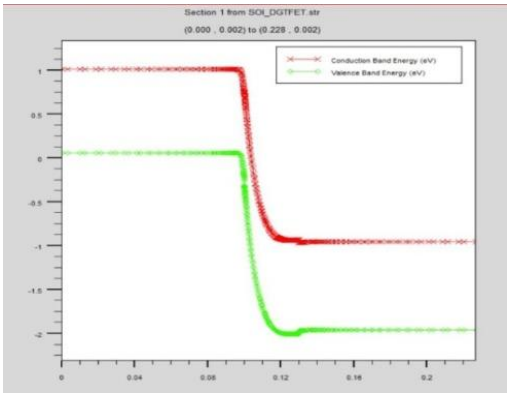


**Fig. 3. Energy band diagram of Double Gate Heterojunction TFET in ON-state when VGS> 0V**

Initially, the barrier preventing the flow of carriers from source to drain region at zero bias of gate voltage. Using the BTBT tunneling mechanism, on gradually biasing the gate voltage pulls down the barrier, creating an overlapping region between the valence band maxima of source side and conduction band minima of the channel. Due to the lesser energy bandgap of *Ge* (0.6 eV) compared to *Si* (1.1 eV), the tunneling process becomes much faster. This results a considerable raise in carrier mobility of the heterojunction tunnel FET.

### B. Transfer Characteristics

Figure 4 depicts the transfer characteristics of double gate heterojunction tunnel FET (HTFET) for supply voltage ($V_{DD}$) = 0.5V. The $I_{ON}$ / $I_{OFF}$ characteristics for our double gate heterojunction TFET structure with various low- κ and high-κ dielectric constants are performed with gate voltage ($V_G$) variation from 0V to 1.5V. The drain current obtained in log scale where the HTFET with high-κ $ZrO_2$ attains maximum value of $I_{ON}$ as $1.522 \times 10^{-5}$ A/μm, whereas, the conventional double gate homojunction TFET with low-κ $SiO_2$ provides $(I_D)_{max}$ as $1.018 \times 10^{-6}$ A/μm as shown in figure 4.

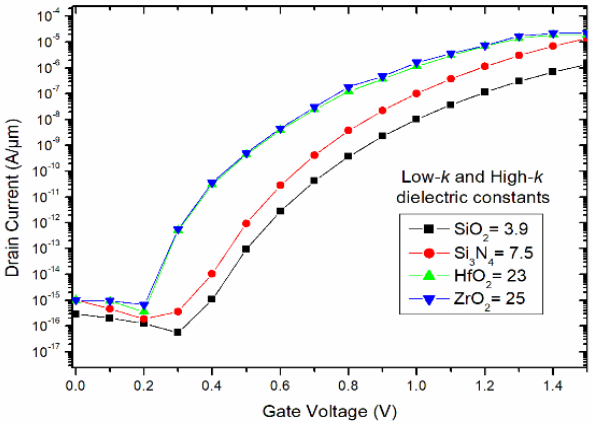


**Fig. 4. Transfer characteristics of Double Gate Heterojunction TFET for various low- κ and high- κ dielectric constants**

Now, the $I_{OFF}$ characteristics of HTFET for different hetero dielectric materials can also be investigated. The drain current obtained in log scale where the HTFET with low-κ $SiO_2$ attains minimum value of $I_{OFF}$ as $1.824 \times 10^{-16}$ A/μm, whereas, the high-κ $ZrO_2$ based HTEFT provides $(I_D)_{min}$ as $1.147 \times 10^{-15}$ A/μm.

### C. High-κ Dielectric Analysis

Larger drive current and reduced subthreshold swing (*SS*) can be attained by minutely selecting proper gate dielectric materials. As shown in figure 5, current boosts as the gate dielectric constant increases. Here, two low-κ dielectrics, $Si_3N_4$ and $Al_2O_3$ and two high-κ dielectrics viz. $HfO_2$ and $ZrO_2$, are compared to $SiO_2$, all with physical thickness of 2 nm. The high-κ materials $HfO_2$ and $ZrO_2$ have dielectric constants of 23 and 25, respectively.

In our proposed double gate HTFET structure, the device comprises with asymmetric gate dielectrics viz. high-κ $HfO_2$, $ZrO_2$ with conventional low-κ $SiO_2$. From the output characteristics of HTFET shown in figure 5, it is clearly observed that $ZrO_2$ – $SiO_2$ combination of dielectric having thickness of 2 nm both in front and back gate, attains maximum value of $I_{ON}$ as $1.522 \times 10^{-5}$ A/μm.

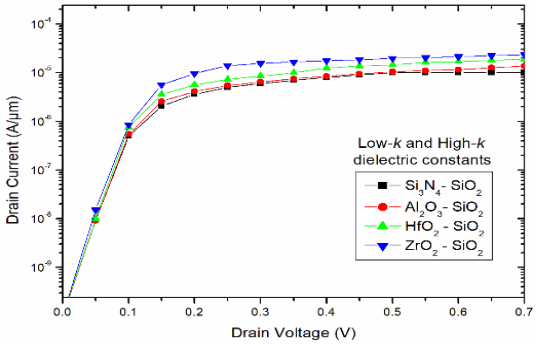


**Fig. 5. Output characteristics of Double Gate Heterojunction TFET for various gate dielectrics**

Various hetero dielectric based heterojunction tunnel FET (HTFET) on transconductance is analysed in figure 6. Since, development in $g_m$ results better charge control of the device, therefore the transconductance – gate voltage characteristics provides solution to identify the correct combination. From figure 6, it is clearly observed that $ZrO_2$ – $SiO_2$ combination of dielectric having thickness of 2 nm both in front and back gate, attains maximum value drive current compared to other dielectric materials.

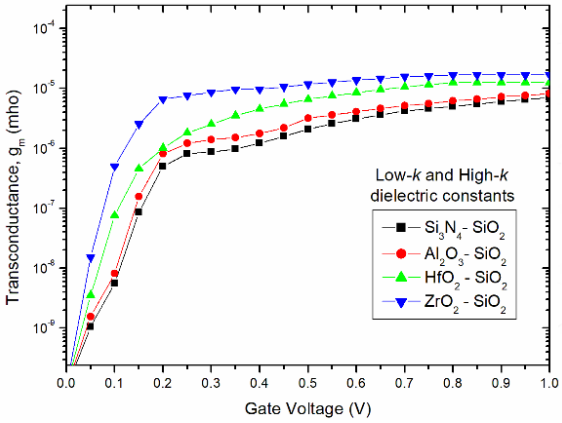


**Fig. 6.Transconductance of Double Gate Heterojunction TFET for various low- κ and high- κ dielectric materials**

### D. Subthreshold Swing

Keeping the overall gate length same as 50 nm for all double gate hetero dielectric tunnel FET structures, the sub-threshold swing (*SS*) is also measured and compared at $V_{DD}$ = 0.5V, $t_{si}$ = 10 nm, $t_{ox}$ = 2 nm. Since in all the transfer characteristics curves the drain current ($I_D$) is taken in log scale, therefore using the equation 2 for finding *SS* swing the comparison report is thoroughly investigated.

$$Subthreshold\_Swing(SS) = \frac{dv_g}{d(\log_{10} I_d)} mv/dec \qquad (2)$$

The comparison reports have been collected from the $I_{ON}/I_{OFF}$ characteristics graphs mentioned above. The subthreshold swing (*SS*) provided by the hetero dielectric i.e. $ZrO_2$-$SiO_2$ double gate HTFET has been recorded best as 23.93 mV/dec in comparison with conventional homo dielectric i.e. $SiO_2$-$SiO_2$ oxide throughout the 50 nm channel of HTFET as 34.22 mV/dec.

In our proposed double gate heterojunction TFET the better subthreshold swing (*ss*) results steeper slope, can be used for fast switching devices.

## IV. CONCLUSION

In this paper, the double gate heterojunction TFET (HTFET) with various high-κ dielectric have been designed and simulated using 2-D TCAD simulator. To deploy our proposed model in low power VLSI applications, a thorough investigation on electrical characteristics have been performed. Since *Ge* having lesser energy band gap, therefore the intrinsic channel is designed using *Ge* material, resulting a heterojunction device model can attain better drive current with less leakage current.

The heterojunction TFET then incorporated with various hetero dielectrics (high-κ and low-κ combination), where the $ZrO_2 – SiO_2$ combination of dielectric having thickness of 2 nm both in front and back gate, attains maximum value of $I_{ON}$ as $1.522 \times 10^{-5}$ A/μm. In addition to this, the subthreshold swing has also been recorded best as 23.93 mV/dec in comparison with conventional homo dielectric i.e, $SiO_2$-$SiO_2$ oxide throughout the 50 nm channel of HTFET as 34.22 mV/dec.

## REFERENCES


1. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, Vol.98, No.12, pp.2095–2110, 2010.
2. W. Y. Choi, B.G. Park Lee and K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.* Vol.28, No.8, pp.743–745, 2007.
3. W. Y Choi and W Lee. "Hetero-gate-dielectric tunneling fieldeffect transistors," *IEEE Trans. Electron Devices*, Vol.57, No.9, pp.2317–2319, 2010.
4. M. Jagadesh Kumar and S. Ramaswamy, "Double Gate Symmetric Tunnel FET: Investigation and Analysis", *IET Circuits, Devices and Systems*, Vol.11, No.4, pp.365-370, 2017.
5. P. Wisniewski and B. Majkusiak, "Modeling the Tunnel Field-Effect Transistor Based on Different Tunneling Path Approaches". *IEEE Transactions on Electron Devices*, Vol.65, No.6, pp.2626–2631, 2018.
6. A. Pon, S. Carmel, A. Bhattacharyya and R. Ramesh; "Performance analysis of Asymmetric Dielectric Modulated Dual short Gate Tunnel field effect transistor", *Superlattices and Microstructures*, Elsevier, Vol.113, pp.608-615, Jan. 2018.
7. R. Jhaveri, V. Nagavarapu and J. Woo, "Effect of Pocket Doping and Annealing Schemes on the Source-Pocket Tunnel Field-Effect Transistor", *IEEE Transactions on Electron Devices*, Vol.58, No.1, pp.80–86, 2011.
8. C. Sandow, et. al., "Impact of electrostatics and doping concentrations on the performance ofsilicon tunnel field –effect transistors", *Solid state electronics*, pp.53, 2009.
9. N. D. Chien and C. H. Shih, "Oxide thickness dependent effects of source dopingprofile on the performance of single and double tunnel field-effect transistors", *Superlatticesand Microstuctures*, Vol.102, pp.284-299, 2017.
10. S. J. Koester, I. Lauer, A. Majumdar, J. Cai, J. Sleight, S. Bedell,P. Solomon, S. Laux, L. Chang, S. Koswatta, W. Haensch, P. Tomasini,and S. Thomas, "Are Si/SiGe tunneling field-effect transistors a goodidea?," *ECS Transactions*, Vol.33, No.6, pp.357–361, 2010.
11. K. Boucart and A.M Ionescu,"Double-gate tunnel FET with high-κ gatedielectric", *IEEETrans. Electron Devices*, Vol.54, No.7, pp.1725–1733, 2007.
12. J. C. Pravin, D. Nirmal, J. Prajoon and Ajayan , "Implementation of nanoscale circuits using dualmetal gate engineered Nanowire MOSFET with high- κ dielectrics for low power applications" *Physica E Low-dimensional Systems and Nanostructures*. No.83, pp.95-100, 2016.
13. K.H. Kao, A. S. Verhulst, W. G. Vandenberghe, et. al., "Direct and IndirectBand-to-Band Tunneling in Germanium-Based TFETs", *IEEE Transactions On ElectronDevices*, Vol. 59, No.2, February 2012.
14. T. Krishnamohan, D. Kim, S. Raghunathan, and K. C. Saraswat, "Doublegate strained-Geheterostructure tunneling FET (TFET) with record high drive currents and < 60 mV/decsubthreshold slope," in *IEDM Tech. Dig.*, pp.947–949, 2008.
15. O. M. Nayfeh, C. N. Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt, and D. A. Antoniadis,"Design of tunneling field-effect transistors using strained - silicon / strained - germanium type-II staggered heterojunctions," *IEEE Electron Device Lett.*, Vol.29, No.9, pp. 1074–1077, Sep. 2008.
16. S. H. Kim, H. Kam, C. Hu and T.-J. K. Liu, "Germanium-source tunnel field effect transistorswith record high $I_{ON}/I_{OFF}$," in *VLSI Symp. Tech. Dig.*, pp.178–179, 2009.
17. U. R. Narang, M. Saxena, and M. Gupta, "Modeling and TCAD Assessment for Gate Material and Gate Dielectric Engineered TFET Architectures: Circuit-Level Investigation for Digital Applications", *IEEE Transactions on Electron Devices*, Vol.62, No.10, pp.3348-3356, 2015.
18. J. Knoch and J.Appenzeller,"Modeling of high-performance p-type III–V heterojunctiontunnel FETs," *IEEE Electron Device Lett.*, Vol.3, No.4, pp.305–307, 2010.
19. S. Verhulst, W. G Vandenberghe, K .Maex., S. De Gendt, M.Heyns , and G. Groeseneken, "Complementary silicon-based heterostructuretunnel-FETs with high tunnelrates," *IEEE Electron Device Letters*,Vol.29, No.12, pp.1398–1401, 2008.
20. K. Nigam, P. kondekar and D. Sharma, "Approach for ambipolar behavioursuppression in tunnel FET by workfunction Engineering," *Micro & Nano Letters*, Vol.11, No.8, pp.460–464, 2016.
21. C. Anghel, Hraziia, A. Gupta, A. Amara and A. Vladimirescu, "30-nm TunnelFET With Improved Performance and Reduced Ambipolar Current," *IEEE Transactions On Electron Devices*, Vol.58, No.6, pp.1649-1654, 2011.
22. D. Gracia, D. Nirmal and A. N. Justeena, "Investigation of Germanium based Double Gate Dual Metal Tunnel FET Novel Architecture using Various Hetero dielectric Materials", *Superlattices and Microstructures*, Vol.109, pp.154-160, 2017.
23. R. Dutta and N. Paitya, "TCAD Performance Analysis of P-I-N Tunneling FETS Under Surrounded Gate Structure", *SSRN-Elsevier*, 2019.