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Design and Development of Microcontroller Based Multilevel Inverter

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Abstract*: Now a day mostly we produce power from non conventional energy sources and power hassle increases day by day. To diminish this power demand we need to emphasize power infusion methods. Multi-level inverter is accommodating to infuse power from distinct renewable sources like solar, wind-power. It generates the alternating output level of voltage from different DC level sources. This inverter uses 'm' H-bridges and several DC sources to obtain (2m+1) level of output voltage. This paper focuses on improvement of quality of desired output voltage waveforms with less number of switching devices.

Index Terms: Cascade H-bridge Multi-level Inverter (CHBMLI), Total harmonic Distortion (THD), Pulse Width Modulation (PWM)

I. INTRODUCTION

A Multi-level inverter is an electronic device which converts the DC voltage preferably low level to desired alternating voltage. Mostly, we use 2 level inverter while converting the alternating voltage from DC voltage source. The expected multi-layer output is acquired by blending multiple DC level voltage sources like batteries etc. These are the common sources used. A common multilevel inverter starts with 3 levels. As the levels increases the output waveform with low harmonics distortion is produced. As per the standard provided by IEEE std 519-1992, total harmonic distortion for the specific equipments should be 5% with the filter and 15-20% without the filter. When we increase the number of levels, the complexity of circuit also increases. Again when we are increasing inverter level, it increases number of proportional devices, with increased cost of inverter. When we increase the number of switches, switching losses are also increases. From the last decade, different topologies have been introduced with several advantages and disadvantage one upon other. These topologies are "diode clamped" (neutral clamped), "cascade H-bridge", "flying capacitor" (capacitor clamped), and "Modified cascade H-bridge". Some of these topologies have capacitor unbalancing and need additional power diode, which reduces the performance of multi-level inverter.

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II. SINGLE CELL CASCADED H-BRIDGE MULTILEVEL INVERTER

Basic multi-level inverter uses single cell which contains four switches connected to form a bridge as shown in figure 1. The switch M1 and M2 are connected to one arm and switch M3 and M4 are connected to other arm. In this the modulating wave (Sinusoidal wave) is compared with carrier triangular wave and resulting waveforms applies switching for Switch M1 and inverse of this wave given to M2. In similar way second modulating and carrier signal gives switching to M3 and M4

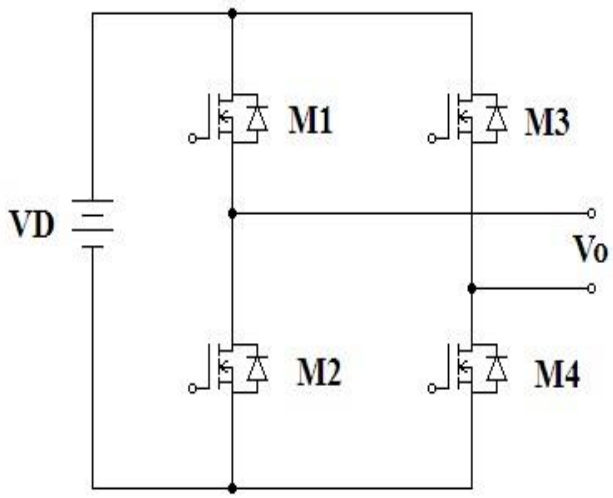

Fig: 1 Single Cell MLI

Fig-1 shows the single phase H-bridge cell. With the help of this cell we can obtain output voltage up to three levels and when cascading with other similar indistinguishable bridge gives five levels. Likewise when we cascade 'm' number of cell, number of levels 'n' in the output voltage turns to,

$n = 2m + 1$.

Fig-2 shows five level cascade H-bridge multi-level inverter. This five level inverter uses eight switches. These eight switches are organize in a such way to form two H-bridges, M1 and M2 forms one arm of first bridge with M3 and M4 forms other arm. Whereas switch M1' and M2' forms one arm of second H-bridge with switch M3, and M4'other arm.

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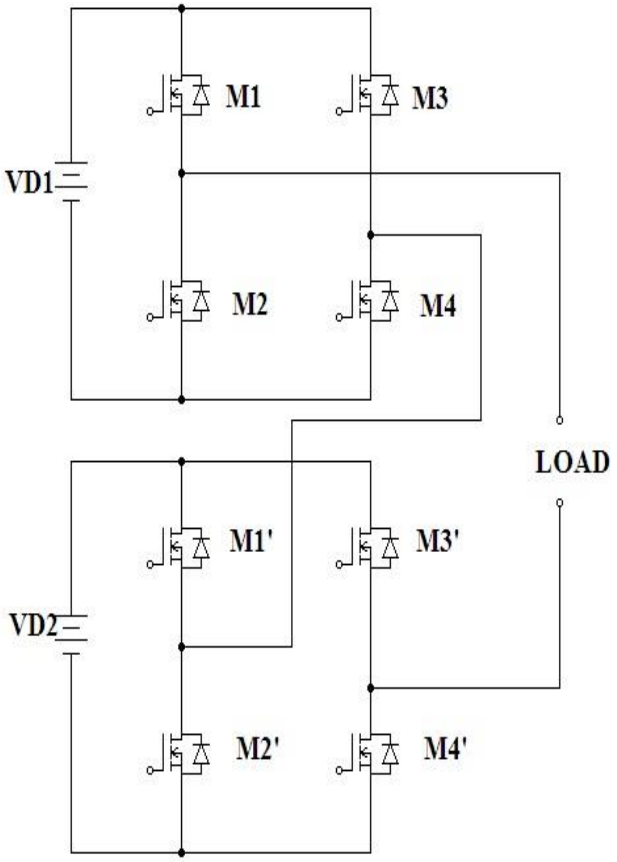

Fig.2: Two Cell MLI

III. BLOCK DIAGRAM AND CONTROLLING CIRCUIT

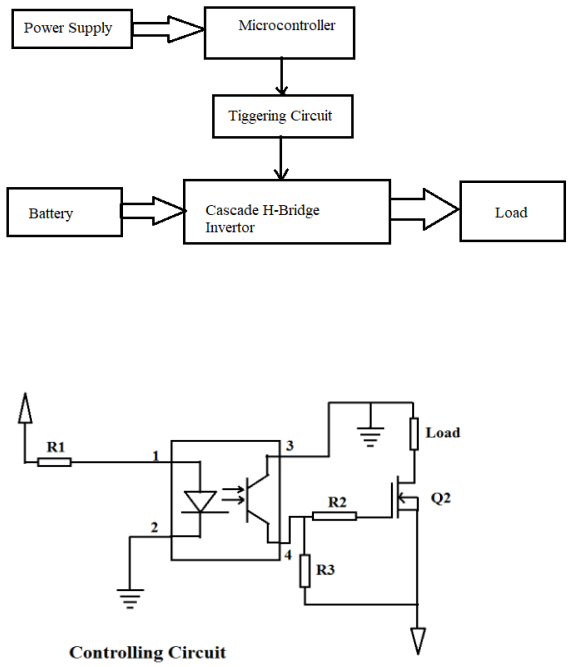

Fig.3 Block Diagram and controlling circuit

The fig.3 shows functional diagram of cascade H-Bridge multi-level inverter. Each cascaded circuit is powered by separate battery source. The output signal of cascade H-bridge circuit is given to single phase load. Total 12 powers MOSFET are used in each H-bridge circuit and switching of MOSFET is controlled by the microcontroller through an opto-isolator. A separate power supply is designed to control and trigger the circuit. Opto-isolator isolates power and control circuit. Synchronized switching strategy obtained by microcontroller to generate stepped power frequency output voltage.

IV. SEVEN LEVEL CASCADED H-BRIDGE INVERTER

Now a days there are many inverters available in the market but multilevel inverters has many advantages with great capabilities, out of this cascade H-bridge multi-level inverter focuses on improvement of output signal quality and damage of power devices with failure to achieve the desired current and voltage levels. Multilevel inverter designed in such way to overcome disadvantages of conventional inverters including some smart features which can be produce minimal distorted output current and voltage with minimal switching frequency.

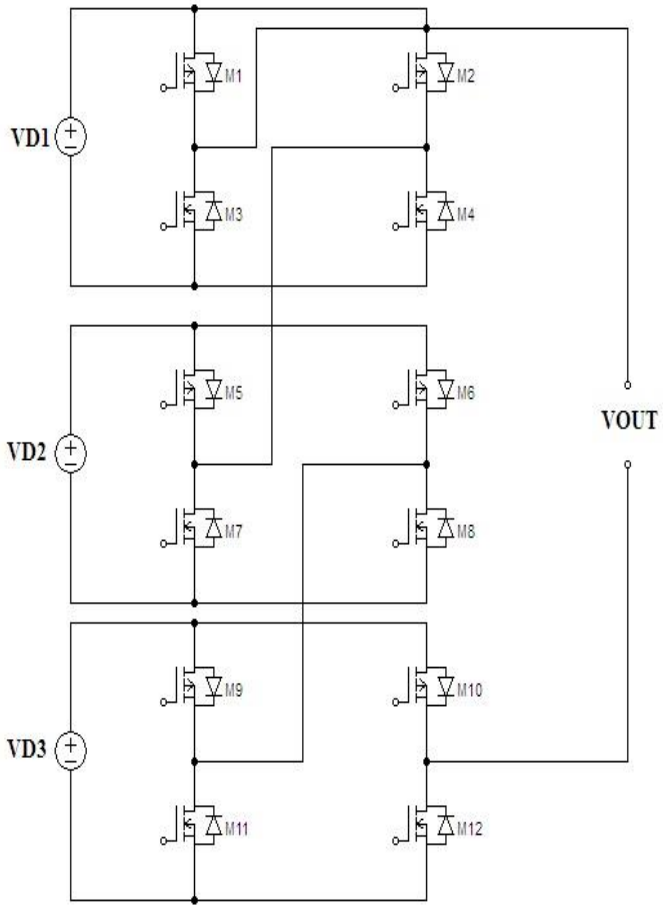

Fig.4 Seven level Cascaded H-Bridge MLI

Fig-4 shows seven levels cascade H-bridge multi-level inverter. It produces seven steps or levels of output in proportional to input source voltage. Input voltage source is suppose VD then expected steps are 3.VD, 2.VD,.VD, 0V,-VD,-2.VD,-3.VD. The output voltage oscillate between +3VD and -3VD. Switching state configuration determines output value of inverter. Switching states in seven levels cascade H-bridge multi-level inverter can be possible in seven different configurations. Each configuration gives output as follows,

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Mode: 1:
Here, This configuration makes MOSFET M1, MOSFET M2, MOSFET M5, MOSFET M6, MOSFET M9 and MOSFET M10 ON, So the level of output VOUT = 3VD.
Mode: 2:
Here, This configuration makes MOSFET M1, MOSFET M2, MOSFET M5, MOSFET M6, MOSFET M10 and MOSFET M12 ON, So the level of output VOUT = 2VD.
Mode: 3:
Here, This configuration makes MOSFET M1, MOSFET M2, MOSFET M6, MOSFET M8, MOSFET M10 and MOSFET M12 ON, So the level of output VOUT = VD
Mode: 4:
Here, this configuration makes MOSFET M2, MOSFET M4, MOSFET M6 MOSFET M8 MOSFET M10 and MOSFET M12 ON, So the level of output VOUT = 0V.
Mode: 5:
Here, This configuration makes MOSFET M2 MOSFET M4, MOSFET M6 MOSFET M8, MOSFET M9 and MOSFET M10 ON, So the level of output VOUT = -VD (-ve)
Mode: 6:
Here, This configuration makes MOSFET M2, MOSFET M4, MOSFET M7 MOSFET M8, MOSFET M11 and MOSFET M12 are ON, So the level of output VOUT = -2VD (-ve)
Mode: 7:
Here, This configuration makes MOSFET 3 MOSFET 4, MOSFET 7, MOSFET 8, MOSFET 11 and MOSFET 12 are ON, So the level of output VOUT = -3VD (-ve)

The summation of output of all bridges connected in series is load voltage. In this multi-level inverter output level is

$$N = 2X + 1$$

Where,
X = separately connected DC level Sources,
N = Number of output levels.

This multi-level inverter combines desired voltage from distinct DC level sources

V. RESULT

A prototype of cascade H-bridge multi-level inverter seven levels is developed and compared with three level inverter and result obtained are summarizes in table given below.

Sr.No	Inverter	Voltage THD
1	3 Level	58 %
2	7 Level	17 %

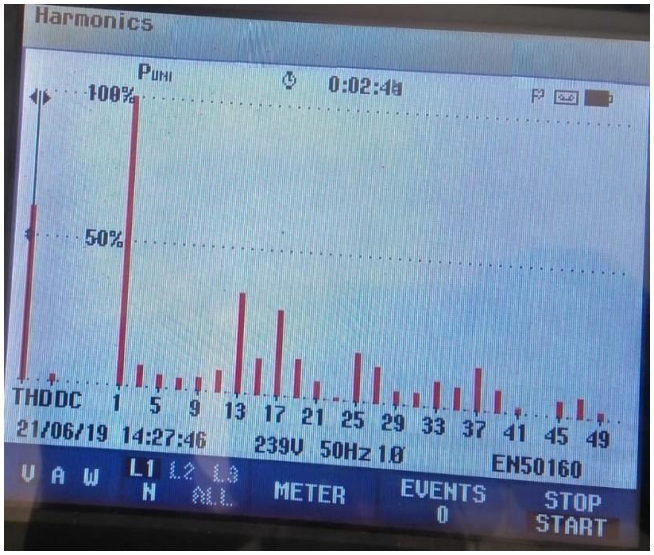

Fig. 4 Three level inverter THD content

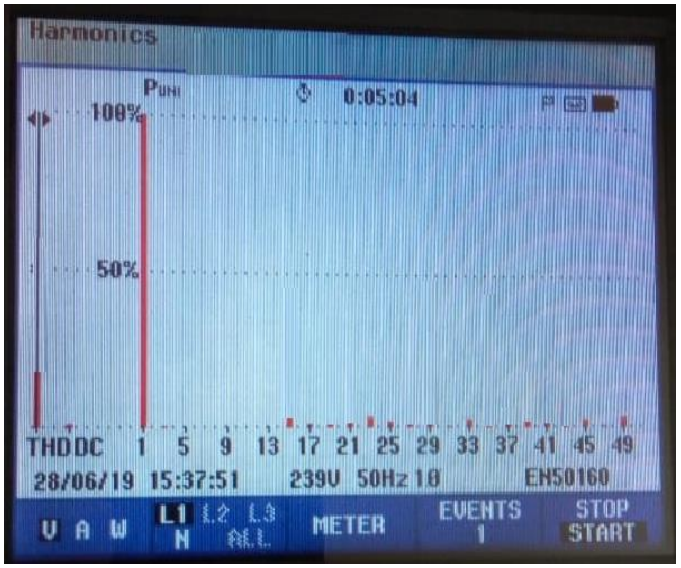

Fig. 5 CHML Seven level THD content

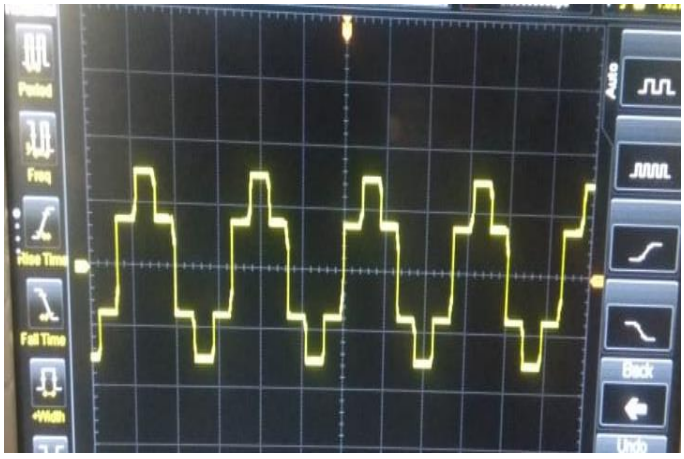

Fig. 6 CHML Seven Level waveforms

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Fig. 4 shows THD content measured by power quality analyzer of three levels inverter. Fig.5 shows THD content of cascade H-bridge multi-level inverter. The total harmonic distortion is a measurement of harmonics present in the output voltage waveform of cascade H-bridge multi-level inverter. Total harmonics distortion (THD) of output waveforms of inverter with respect to pure sine wave measured by power quality analyzer. Fig.6 shows the stepped waveform of cascaded H-bridge multilevel inverter, which becomes more sinusoidal if we increases the number of output voltage level. While comparing with three level inverter, content of THD is lesser in seven level CHML.

VI. CONCLUSION

In this way we have designed and developed Multi-level Inverter by using the single phase cascade H-bridge multi-level inverter. Analysis of different levels are compared and found total harmonics distortion (THD) content is approximately 40% less in seven levels than three level inverter. As levels are go increasing harmonics content decreases but up to particular point only.

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