Consequences of Body-Biasing Technique on SRAM Memory

Mukesh kumar, J.S. Ubhi

Abstract: ***The circuit changes the threshold voltage effectively with a definite delay and power by altering the body biasing of the transistors. The body bias is employed to govern the frequency and leakage of the memory device. The threshold voltage of individual transistor is decreases by applying the reverse body bias (RBB) and increases with forward body bias (FBB). This paper presents the viability of RBB to decrease the leakage power and increase in the speed of operations for SRAM circuit. The investigation of RBB dependencies on various performance parameters are analyzed. It is observed that the leakage power improves by 30.32% on applying RBB voltage compared to zero body bias while the transient power increases by 3.22% but decrease of delay by 84.56% dominates on it. Because of this the overall energy consumption reduces by 84.06%. Further the simulation work is carried out to see effect of supply voltage variation on leakage power at different RBB voltage and temperature. Therefore, the RBB scheme is beneficial for devices of low leakage, low energy and high speed of operation but this RBB voltage is limited by band-to-band tunneling current.***

Index terms: RBB, Frequency, leakage power, delay

I. INTRODUCTION

Through persistent scaling in CMOS technology, the feature size of the incorporated circuits encounters numerous physical confinements. The increasing leakage current, and the number of transistor per unit area leads to power dissipation in the device. Numerous applications like analog to digital converter, cache memory of computer, laptop, high speed registers, electronic toys, biomedical and wireless sensor networks, need very low-power circuits for long-time performance [1, 2]. The power dissipation, stability and operating frequency are the main concern in semiconductor industry. The device performance deterioration is because of bias temperature instability (BTI), hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), etc. that causes irregular functioning, unsuitable biasing and inappropriate environment condition during their working [3]. The substrate or body of MOS devices in a design is common, therefore body of all often kept at same voltage. The body biasing technique is utilized to alter the threshold voltage of transistors. As the source to body bias voltage increases, the depletion width of channel-body increases resulting in enhanced trapped charge density in depletion region and to maintain neutrality in channel charge must decrease. It impacts on the gate channel potential drop by adding of body bias to the channel-body junction voltage [4]. Various schemes have been implemented to apply body biasing on the transistors to decrease the delay (by reducing threshold voltage), the active power (on bringing down supply as well as threshold voltages although keeping up a similar speed when compared with a high threshold voltage circuit), leakage current or intra-die as well as inter-die threshold voltage disparity (by adaptive biasing) [5, 6]. The power and current requirement of body bias generator may get important, if the body bias voltage of transistors of a circuit is adjusted [7]. There may be two types of body biasing implemented: FBB is used to reduce threshold voltage and enhance device performance while RBB is utilized to enhance the threshold voltage and reduce the leakage current and hence power [8]. The use of the FBB is to boost threshold voltage roll-off conduct empowers the utilization of shorter gates can be clarified by a quasi 2-Dimensional model. RBB technique is often used to reduce the leakage of the circuit especially when it becomes idle. Reverse body biasing leads to increase in threshold voltage and hence decreasing the subthreshold leakage current. However, band to band tunneling current from source to substrate and drain to substrate p-n junction diode increases with increase of reverse bias voltage [9]. It is approaching to reduced leakage current at high value of reverse bias voltage. Consequently, an optimum RBB voltage is restricted by increased band-to-band tunneling currents that can be used in a transistor to decrease the total leakage current [10]. The efficacy of RBB is diminished as scaling of technology occurs because of increased effect of short channel and reduced impact of body effect [5], [9]. It is assumed that forward body biasing approach may be an alternate to the reverse biasing. It not only increases the body effect but also reduces the short channel effect. It is supposed that forward body biasing will be more productive in managing the threshold voltage of MOS device in near future technology as the ratio of supply voltage to threshold voltage reduces with scaling of technology [7]. The reverse body biasing voltage of a MOS transistor is limited by the voltage applied across the gate oxide. It can also be decreased by scaling down the gate oxide thickness in future generation of technology [11]. The remaining of the paper is structured as the following: In section II, the proposed SRAM cell structure is described. Section III shows the simulation results of the performance parameters by applying the body biasing of the SRAM cell. Finally, Section IV includes the conclusion and at last references are included.

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II. SCHEMATIC OF PROPOSED 10T SRAM MEMORY CELL

The transistor gating (TG) technique is utilized in design of a 10T SRAM cell from 6T SRAM cell and schematic is displayed in the Fig.1. It has transistor PM2 in the middle of PM0 & QB while PM3 is connected among PM1 & Q. NM2 transistor follows among NM1 & ground though NM3 is associated among NM0 & ground. Transistor PM3 is connected among PM1 & Q though NM2 in the middle of NM1 and ground. The transistors PM2 & PM3 are connected at draw up segment while NM2 & NM3 is associated to draw down part. Sleep transistors are "turned on" in active mode with the use of suitable gate voltage & stays "off" for hold condition on admissible gate supply voltage.

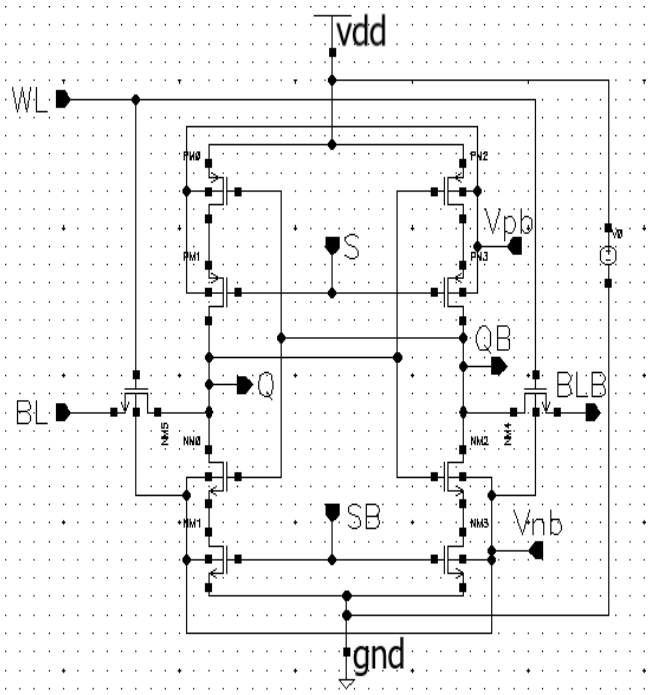

Fig.1 Schematic of 10T SRAM cell

III. RESULTS AND DISCUSSION

The threshold voltage of the transistor is demonstrated as a function of substrate bias co-efficient (Υ), fermi-level (ϕ_F) and source to body bias voltage (V_{SB}) as shown in equation given below [4]

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \quad (1)$$

$$\gamma = \sqrt{2q N_A \in_{Si}} \Big/ C_{OX} \quad (2)$$

$$C_{OX} = \in_{Si} / t_{ox} \quad (3)$$

$$\phi_F = \frac{KT}{q} \ln\left(\frac{n_i}{N_A}\right) \quad (4)$$

The variable V_{TO}, q, N_A, C_{Si}, t_{ox}, C_{ox}, K, T, n_i represent the threshold voltage when source to body is at zero potential, charge of carriers, acceptor concentration, permittivity of Si, oxide layer thickness, oxide capacitance, Boltzmann constant, temperature in kelvin and intrinsic Si concentration respectively.

Forward body biasing of NMOS

By keeping PMOS to maximum supply voltage and increasing NMOS body voltage above ground level is forward biasing condition. The simulation result is shown in the Table.1 as shown below

Table.1 Forward body biasing simulation results of NMOS 10T SRAM memory cell.

Forward Biasing voltage	Transient power (nW)	Static power (pW)	Delay(ps)
V_{PB} = 1V, V_{NB} = 0V	353.59	3.40	814.12
V_{PB} = 1V, V_{NB} = 0.2V	352.45	6.04	851.98
V_{PB} = 1V, V_{NB} = 0.4V	352.08	26.35	879.46
V_{PB} = 1V, V_{NB} = 0.6V	379.68	327.42 (n)	898.83
V_{PB} = 1V, V_{NB} = 0.8V	41.26 (µ)	42.03 (µ)	912.08
V_{PB} = 1V, V_{NB} = 1V	9.93 (m)	10.15 (m)	922.25

The forward body biasing simulation results shows that the transient power, leakage power and delay of SRAM memory cells increase with increase of forward body biased condition. The transient and leakage power increases by large amount as the biasing voltage increases after 0.6 V.

The threshold voltage variation of access transistors NM4 and NM5 of 10T SRAM as shown in Fig.1, with forward biasing and reverse biasing is illustrated in Fig.2. The threshold voltage decreases with forward biasing and increases with reverse biasing the body of NMOS transistor of SRAM memory. With FBB the threshold voltage of NM4

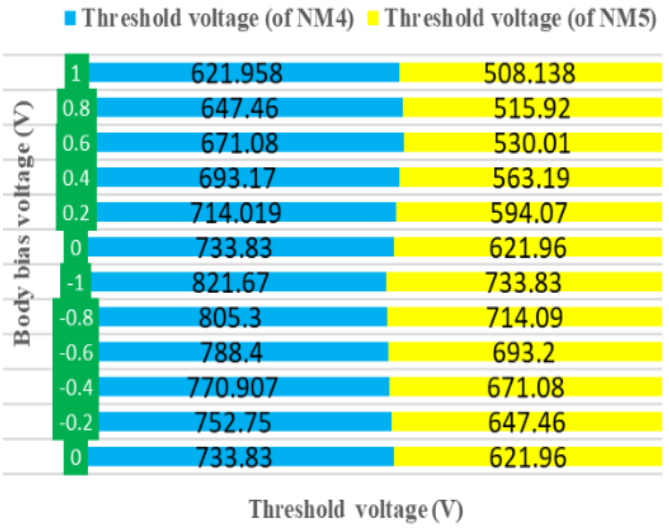

Fig.2 Impact of body biasing voltage on Threshold voltage of access transistor

and NM5 decreases by 15.24% and 18.30% respectively for the bias voltage variation from 0 to 1V while threshold voltage increases by 11.97% and 17.99% respectively for NM4 and NM5 for reverse body voltage variation from 0 to -1 V.

Reverse body biasing of NMOS

The substrate of PMOS transistor is coupled to supply voltage and substrate of NMOS transistor is decreased beyond ground voltage, it indicates the reverse body biasing of NMOS.

The simulation result of impact of reverse body bias of NMOS on transient power, delay and energy (power delay product-PDP) is shown in Fig.3. It can be observed that transient power is increasing but it is less prominent to the reduction of delay, resulting in the reduction of energy as

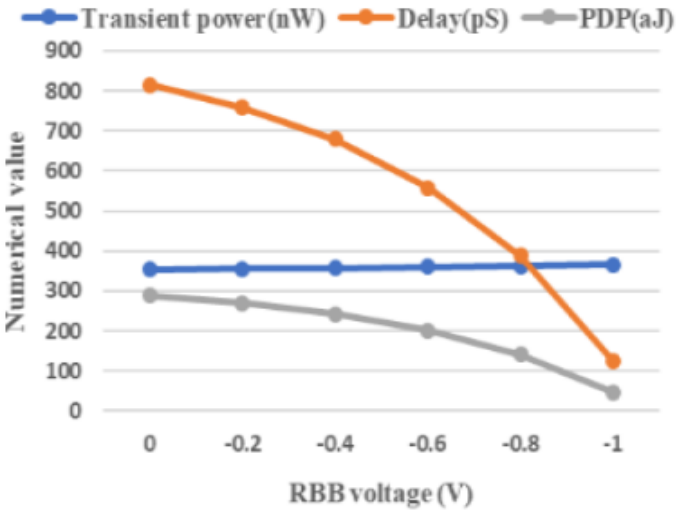

Fig.3 Impact of RBB voltage on delay, transient power and PDP

RBB voltage reduces from 0 to -1 V. The transient power is increases by 3.22% while the delay and energy consumption decrease by 84.56 % and 84.06 % respectively.

The effect of RBB voltage on leakage power at 1 V of supply is seen in the Fig.4. It reduces by 30.62 % for variation of RBB voltage from 0 to -1 V.

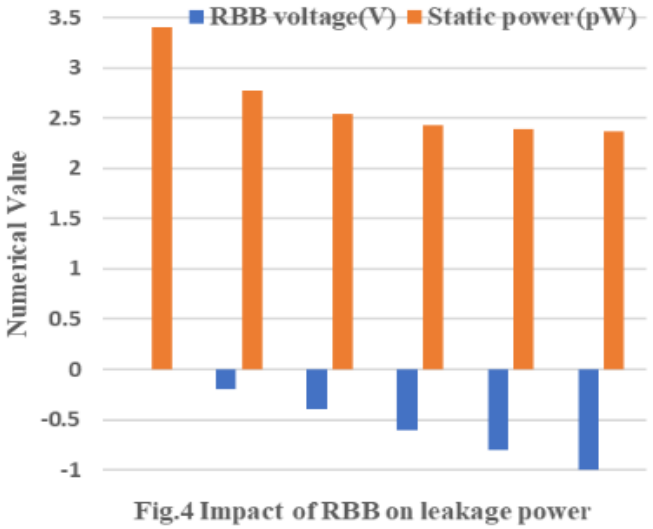

Fig.4 Impact of RBB on leakage power

Fig.5 illustrates the parametric analysis of leakage power with variation of supply voltage from 0 to 1 V at different temperature ranging between -67 ^{0}C to 127 ^{0}C.

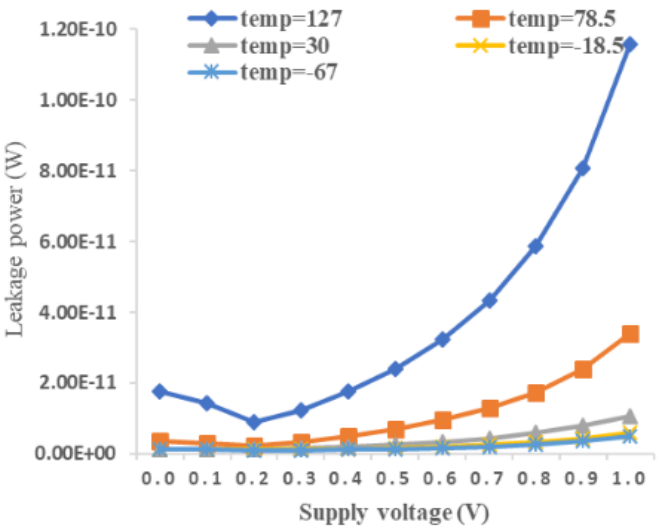

Fig.5 Leakage power variation with supply voltage at different temperature (deg. cel.)

The leakage power trend with variation of supply voltage at different RBB voltage at 27 ^{0}C temperature can be observed from Fig.6. The leakage power is maximum for -1 V of body

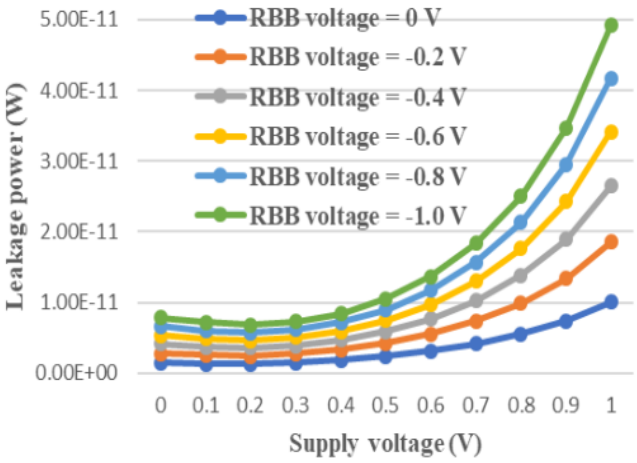

Fig.6 Effect of supply voltage on leakage power at differrnt RBB voltage

biasing voltage and minimum for zero body biasing voltage. For lesser value of voltage, the leakage power is less but it increases exponentially after 0.5 V of voltage.

The combined outcome of temperature and RBB voltage on leakage power with variation of supply voltage is observed in Fig.7. The leakage power is maximum for condition of 127^{0}C and 0 RBB voltage followed by same temperature with -0.5 V and -1.0 V respectively.

The simulation work is also carried out to examine the collective impact of variation of access transistor width and RBB voltage at distinct supply voltage as shown in Fig.8 . It is seen that the leakage power is least for the access transistor width of 120 n and -1 V of RBB voltage and maximum for 360 n width and 0 V RBB voltage. The analysis depicts that the leakage power increases with increase of width and decrease of RBB voltage.

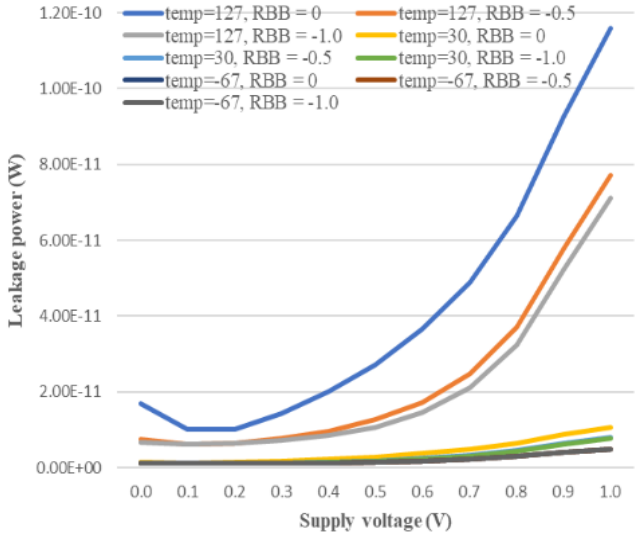

Fig. 7 Impact of both temperature (degree celcius) and RBB voltage (V) on leakage power

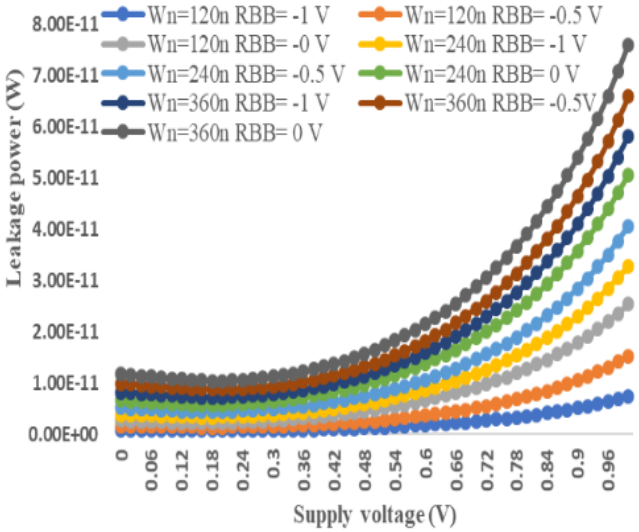

Fig.8 Impact of supply voltage on leakage power with different access transistor width and RBB voltage

IV. CONCLUSION

This paper investigates the consequences of body biasing technique implemented on NMOS transistor of 10T SRAM memory cell. The forward and reverse body biasing approach is implemented on the access transistor of memory to examine affect on threshold voltage. Reverse body biasing is imposed on NMOS and the PMOS body remains at the source potential. The reverse biasing varied from 0 to -1 V at room temperature and observed that it has dominant effects on reduction of leakage power, delay, and PDP while a marginal increase of transient power is also observed. The impact of source voltage variation on leakage power with different RBB voltage, temperature and both are detected. It is seen that the leakage power decreases with decrease of temperature and increase of RBB voltage. The leakage power trend for width of access transistors along with biasing voltage are observed for different supply voltage. It is concluded that as width of transistor increases with RBB voltage, the leakage power increases.

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