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Three-Phase Symmetric Cascading Z-Source Seven Levels Multilevel Inverter Excited by Multi Carrier Sinusoidal Pulse Width Modulation Scheme

Rajnish Kumar Sharma, G. Irusapparajan, D.Periyaazhagar

Abstract: ***The Multilevel Z sources Inverter have been documented as attractive topologies used for elevated voltage adaptation. As the digit of levels improved, the synthesized set of steps output waveform have many ladder, imminent the preferred sine waveform but the major weakness of MLI be its amplitude of ac output voltage is imperfect to DC input sources voltage summing up. To conquer this drawback seven level cascading symmetric multilevel inverter based Z source inverter have been projected. This work focuses on different multi-carrier sinusoidal PWM scheme for the seven level three phase Z source symmetric cascading inverter. Performance parameters of seven level three phase Z source symmetric cascading inverter has been analyzed. A simulation circuit model of seven level three phase Z source symmetric cascading inverter urbanized using MATLAB/SIMULINK and its presentation have been urbanized.***

Keywords: Multi-level Inverter, symmetric multilevel inverter. Z source, Root Mean Square

I. INTRODUCTION

MLI is a valuable and realistic solution for rising power demand and dipping harmonics of output AC waveforms. Purpose of a MLI is to produce a beloved voltage wave form from numerous levels of DC source voltages. A whole investigation of the decreased switch MLI topology with different type is as described in [1]. The topologies can create twenty seven level ac output voltages through the assist of twelve switches and three dc sources. It has been examine with a variety of unipolar multicarrier PWM types [2]. The primary function of MLI is to synthesize a preferred ac voltage beginning some separate dc sources, which could be obtain beginning batteries, solar cells, or fuel cells [3]. Multilevel inverter produces a preferred output voltage as of some levels of key in DC voltage sources. By means of an growing amount of DC input voltage sources, the inverter output voltage waveform stage growing.[4] [5].

The multilevel inverters encompass more reward which comprise minor semiconductor voltage stress, superior harmonic presentation, small EMI and lesser switching loss. A nine level grid coupled inverter topologies with photovoltaic construction operated with absence of one phase transformer is investigated in [6–8].Z source three level inverter topologies are implemented [9]. Analyses of common mode out voltage and PWM strategy for variable speed drive [10]. A variety of unipolar PWM schemes for a one phase 5-level cascading inverters [11].

II. Z-SOURC E SEVEN LEVEL CASCADED INVERTER

The figure.1 shown the 2-port system that configuration of a capacitors (C1, C2) and inductors (L1, L2) and linked in X form is engaged to present an impedance source pairing the inverter to the input dc source.

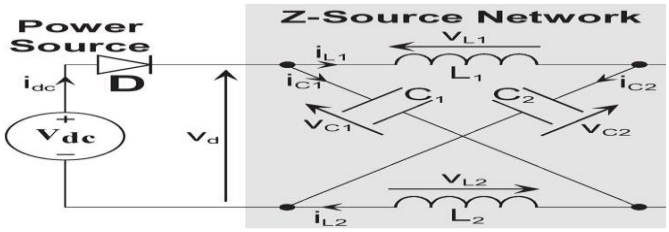

Fig. 1 Z- Source Circuit model

A diode is attached in the Z source arrangement as showing Figure. 1 to manage repeal current flow. Voltage surroundings Z-source inverter can be visualize all energetic and void switching model of voltage source inverter.

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*Correspondence Author(s)
Rajnish Kumar Sharma, Department of Electrical and Electronics Engineering, Bharath University, Chennai, India
G. Irusapparajan, Department of Electrical and Electronics Engineering, Mailam Engineering College, Mailam, India
D.Periyaazhagar, Department of Electrical and Electronics Engineering, Krishnasamy College of Engineering and Technology, Cuddalore, India

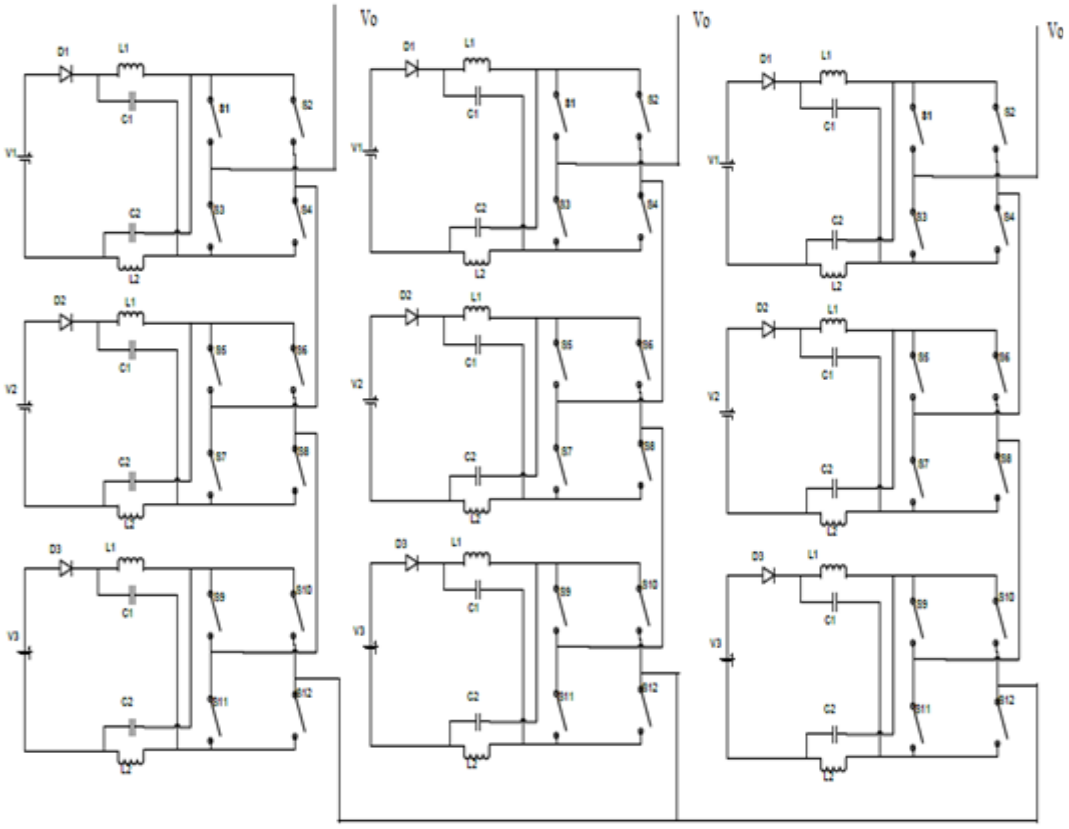

Fig. 2 Seven Level Three phase Z- source cascading inverter

The figure.2 has shown the Seven Level Three phase Z-source cascading inverter. The inverter configuration is based on the sequence association of one-phase inverters with divide impedance dc input sources. The consequential phase voltage is presented by the adding of the voltages created by the dissimilar cells. The quantities of output ac voltage levels are $2m+1$, where m is the quantity of cells. The ac output voltage of every half bridge is associated in sequence such that the created output ac voltage waveforms are the addition of every individual half bridge outputs.

III. MULTI CARRIER PWM SCHEME

Dissimilar types of PWM reins have been investigated in the journalism in [1]. Carrier Based PWM is the majority popular categories. But, carrier based PWM is frequently used for superior voltage steps. While the SVPWM are complicated for creating pulses for additional than 5-levels due to the job loss of switching state [12-15].Therefore, carrier based PWM control is preferred as the organize system for the projected topology in this expose. Variety of carrier based PWM is used to produce switching pulses in the projected topologies. In carrier based PWM scheme, several carriers ("m" level inverter ac output need "(m–1)" carriers) are created collectively which are constantly compared with sine reference signal and generate the PWM pulse [16].

There are several carriers planning to realize the PWM scheme. In this effort the subsequent scheme is carried out.

1. PD (Phase disposition) PWM scheme.
2. POD (Phase opposition disposition) PWM scheme.
3. APOD (Alternate phase opposition disposition) PWM scheme.

III.1. PD (Phase disposition) PWM scheme

If the orientation wave is greater than a carrier wave, then the active switching strategy equivalent to facilitate carrier wave are switch on. Or else, the switching strategy switches off is shown in figure.3.

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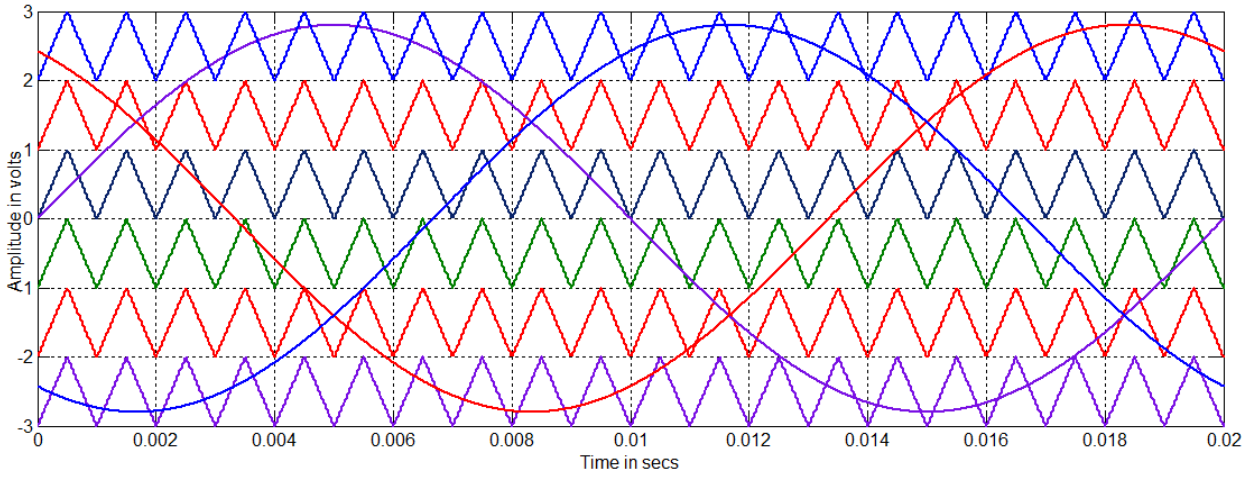

Fig. 3 Carrier wave understanding for PDPWM Scheme

III.2. POD (Phase opposition disposition) PWM scheme

In this PWM plan the carrier wave beyond the zero position are in phase. The carrier wave under are as well in phase, but are 180° phase shifted as of those beyond zero as exposed in Figure.4.

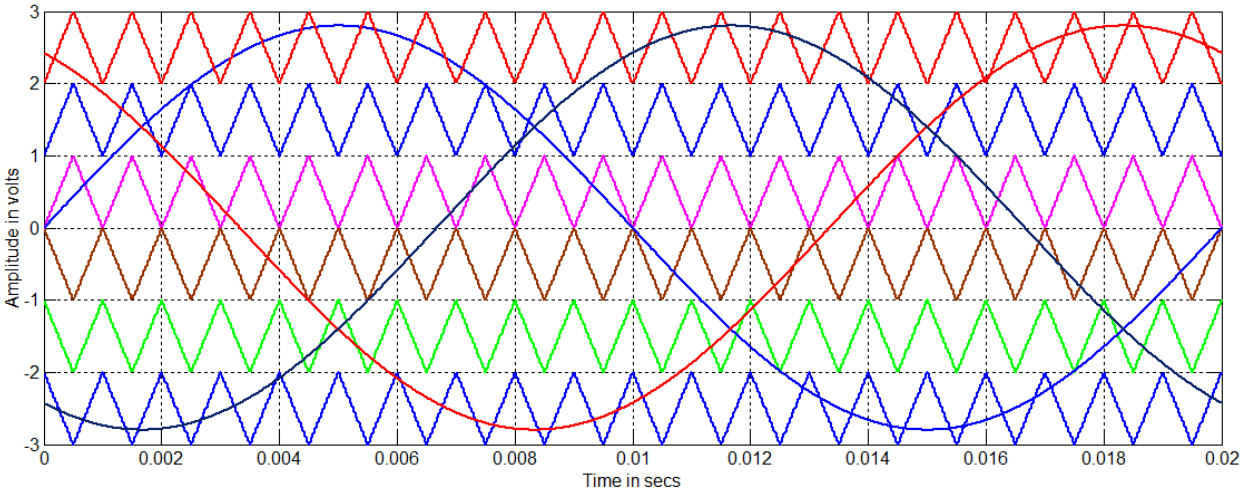

Fig. 4 Carrier wave understanding for POD PWM Scheme

III.3. APOD (Alternate phase opposition disposition) PWM scheme

In this PWM plan the carrier waves of similar amplitude are phase displaced as of each other by 180° alternately. The carrier understanding is exposed in Figure.5.

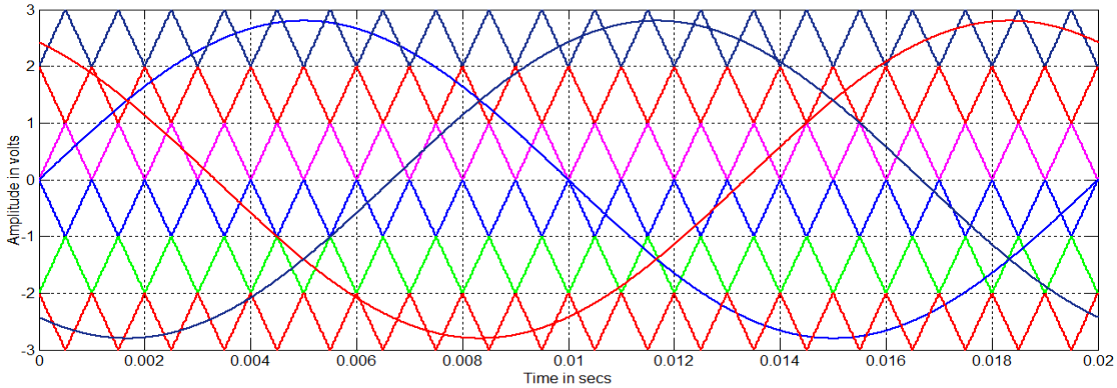

Fig. 5 Carrier wave understanding for APOD PWM Scheme

IV. SIMULATION AND RESULTS

The seven level three phase Z- source cascading inverter is developed in SIMULINK by means of MATLAB. Switching plan for seven levels cascading three phase multilevel inverter by sin PWM strategy are pretend. Simulation is exposed for dissimilar values of modulation index ranging between 0.8 to 1 and the equivalent %THD is measured by means of the FFT block and their values are programmed in Table 1. Figure 5-10 confirm the imitation output ac voltage of three phase Z-source cascading inverter and their harmonic spectrum. Figure.5 exposes the seven level ac output voltage developed by PD PWM Scheme and its FFT plan is revealed in Figure.6. Figure.7 exposes the seven level ac output voltage developed by POD PWM Scheme and its FFT plan is revealed in Figure.8. Figure.9 exposes the seven level ac output voltage developed by APOD PWM Scheme and its FFT plan is revealed in Figure 10. Table 1 and Table 2 exposes the %THD of the ac output voltage and V_{RMS} for a variety of modulation index of three phase seven level Z-Source cascading inverter correspondingly.

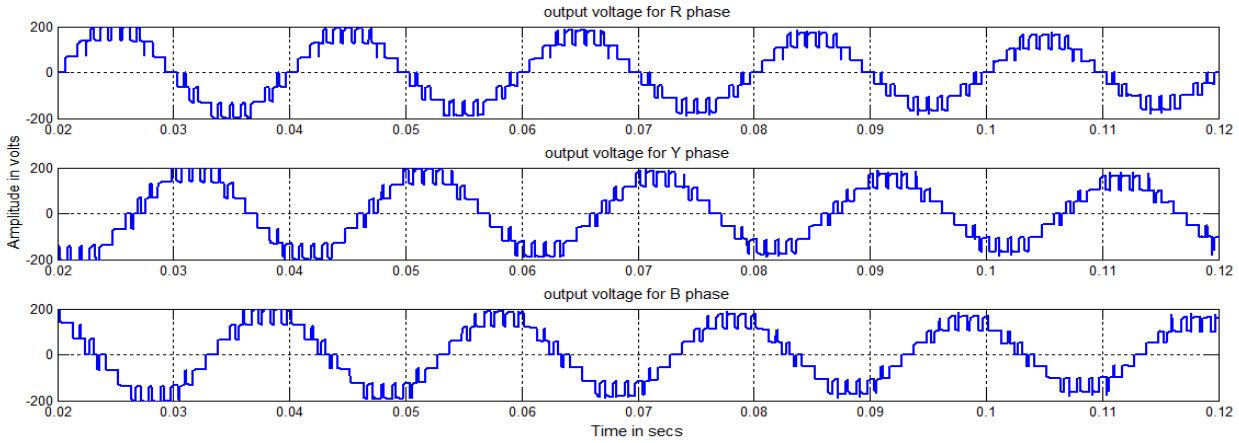

Fig. 6 AC Output voltage developed by PD PWM Scheme

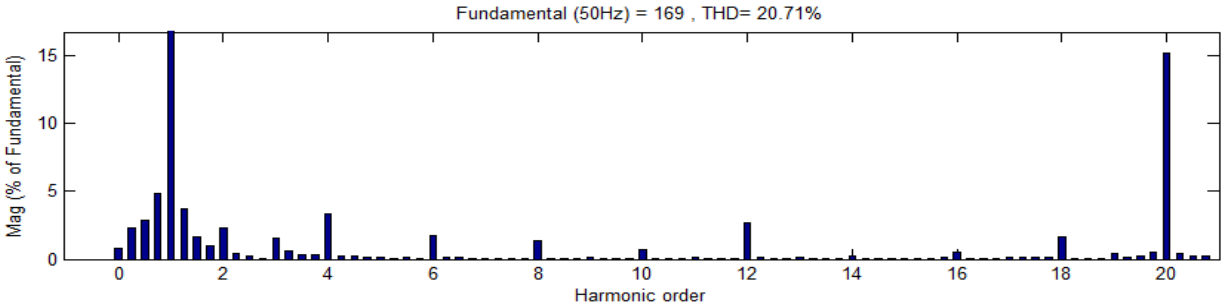

Fig. 7 FFT plan for an ac output voltage of PD PWM scheme

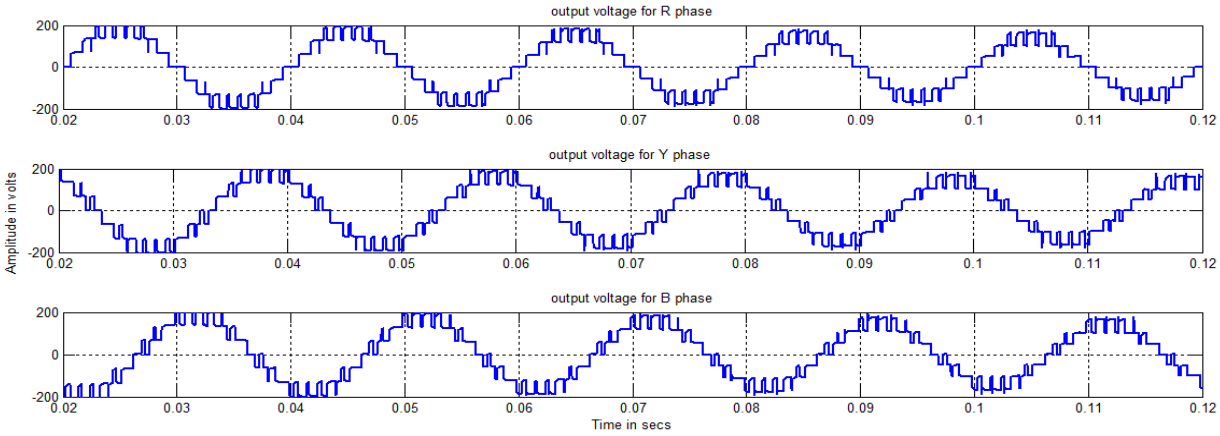

Fig. 8 AC Output voltage developed by POD PWM Scheme

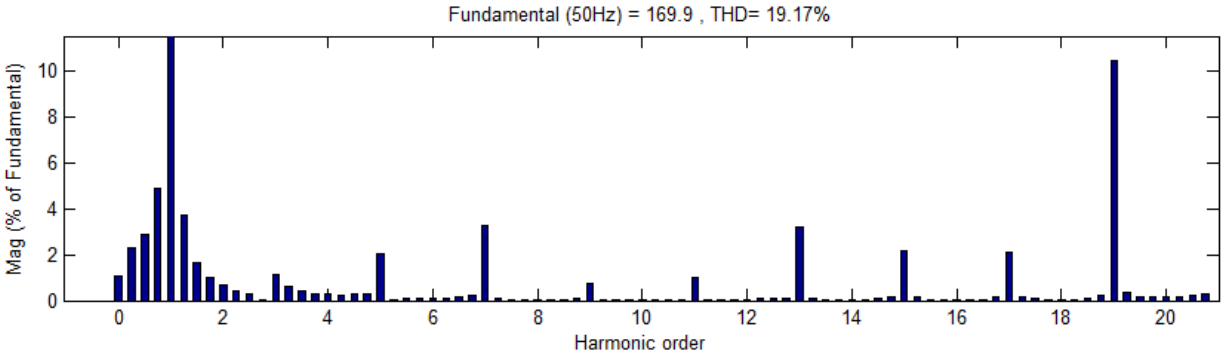

Fig. 9 FFT plan for an ac output voltage of POD PWM scheme

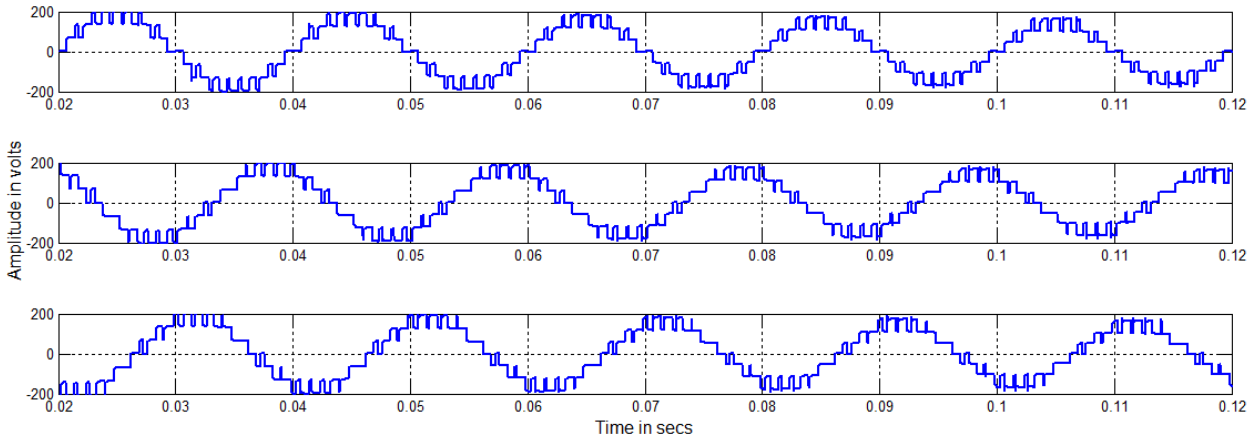

Fig. 10 AC Output voltage developed by APOD PWM Scheme

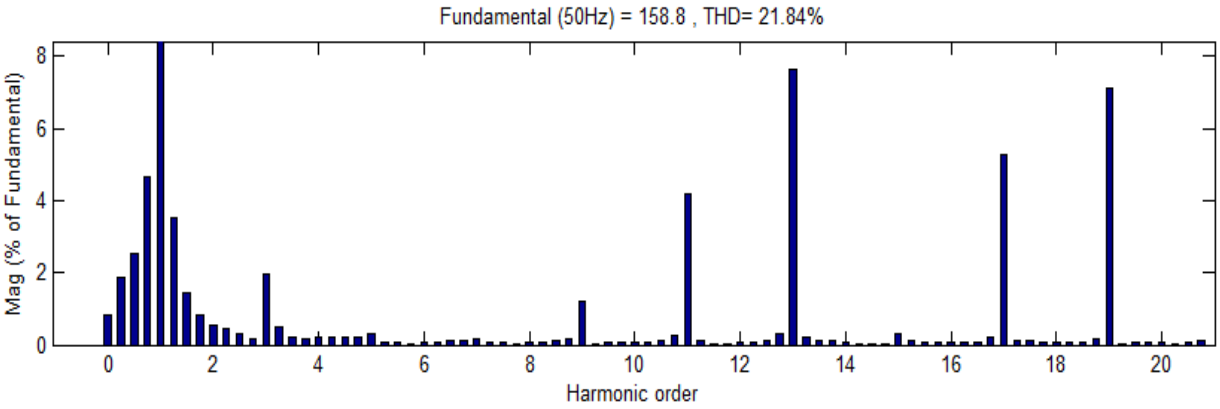

Fig. 11 FFT plan for an ac output voltage of APOD PWM scheme

Table. 1 % THD for dissimilar Modulation Index

Modulation index	PD plan	POD Plan	APOD Plan
1	16.34	19.70	17.22
0.9	20.12	21.32	23.22
0.8	23.11	24.16	24.56

Table.2. V_{RMS} for dissimilar Modulation Index

Modulation index	PD plan	POD Plan	APOD Plan
1	125.34	124.70	117.22
0.9	122.12	113.32	112.22
0.8	112.11	111.16	110.56

V. CONCLUSION

In this manuscript, the seven level three phase Z- source cascading inverter have been offered. Seven level three phase Z- source cascading inverter gives superior output ac voltage throughout its Z-source arrangement. Performance factors like V_{RMS} and %THD has been calculated, accessible and analyzed. It is originate to the PD PWM plan provides lesser %THD and superior V_{RMS}.

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