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Three Phase 9-Level Hybridised Cascaded Multi-Level Inverter for Use in Smart Grid

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Abstract: ***Smart grid technology can be best utilized by having proper grid supporting equipment. This paper demonstrates the use of a three-phase, 9-level, hybridised cascaded multi-level inverter topology in a smart grid. A pulse width modulation scheme with phase disposition is employed in this inverter to control the firing signals to operate this circuit. These firing signals can be monitored and controlled for optimal usage in smart grid operation. Operational principles with switching equations are described in detail. Crucial voltage identification has been performed by analyzing the THD in output during source shortages by performing Fast Fourier transform analysis. Least THD of 15.82% is attained in the output voltage waveform of the proposed three phase inverter topology.***

Keywords: inverter; hybridised, cascaded, 9-level; grid; smartgrid.

I.INTRODUCTION

Smart grids can play a vital role in the world's technological advancement. A smart grid helps in the effective utilization of power by optimizing resources[1]. With the present day scenario of diminishing renewable energy resources, smart grids enable to connect all grid components to a central control hub to monitor and control the usage of power accordingly. A renewable energy based inverter when connected in synchronization through a smart grid to the main electrical grid results in lesser losses and better power utilization cum saving.Using modern inverters[2-3] the power conversion can be implemented with improved power quality. In previous developments, the diode-clamped[4], flying-capacitor[5,6], and cascaded H-bridge (CHB) multi-level inverters[7] were implemented and replaced the 3-level inverters[8] in medium and high-voltage applications[9] such as motors[10] and static var-compensator[11] applications.

Multi-level inverter topologies have better features of HV capability, reduced common mode voltages, almost sinusoidal outputs and helps in a smaller or even absence of output filter, that makes them suitable for use in applications of distributed generation[12] and also high power applications like traction[13, 14]. One of the most famous modulation strategies for the multi-level inverter topologies is sinusoidal pulse width modulation (PWM)[15], which is used for two modes of carrier arrangements, namely level shifted (LS-PWM) which is commonly known as phase disposition, and phase shifted (PS-PWM)[16,17]; and other well used modulation methods include multi-level SHE (selective harmonic elimination) and multi-level SVM[18, 19] (space vector modulation). The main drawback of NPC inverter topology for implementation above three levels is the requirement of a capacitor voltage balancing control circuit and the high voltage applied across the clamped diodes; whereas the flying capacitor multi-level inverter uses the capacitors as clamping devices. The advantage of being used without the need of a transformer and redundant phase leg states which allow the switching stresses to be equally distributed among the power switches [20,21]is a very important characteristic of the FC topology in comparison with NPC topology. But, these inverters have the disadvantage of using numerous storage capacitors for high voltage levels, which can be quoted as a disadvantage.

A double flying capacitor multi-cell topology has been presented in Reference 22 which was implemented by adding two low-frequency switches to the standard configuration of the FC multi-level inverter. The main advantage of the proposed inverter in comparison with the flying capacitor multi-level inverter is the increase in the RMS value by two times of the output voltage and the voltage levels count and the neutering of the midpoint of the dc source. But, two extra switches must operate at the peak of the output voltage which also restricts the usage of this inverter in high voltage applications.

Asymmetric and/or hybrid multi-level inverters have been presented in References 23 and24 in which the values of the dc voltage source magnitudes are unequal or alter dynamically. These topologies minimize the size and cost; and improve the reliability, since lesser switches and capacitors are employed[25]. The hybrid multi-level topologies include different multi-level topologies with unequal values of dc voltage sources and different modulation techniques used as per the different switches used for commutation. With appropriate selection of switching devices, the converter cost can be significantly reduced; but the application of different multi-level topologies leads to the deprivation of modularity and instills problems in switching frequency and restricts the modulation and control methods[26].

The series connection of basic H-bridge inverters results in the multi-level CHB inverter configurations[27], which have been known to have better operation. This inverter topology is a viable option for higher levels of operation because of its modular design and also because of the ease of control strategy. An NPC PWM 3-phase inverter having four switches in each arm has an output of 5-level voltage that

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results in considerable suppression of the harmonic components when compared with the traditional full-bridge 3-level PWM inverters, which is not the case for single/three-phase PWM inverters. Majority of inverters adopt the full-bridge operation using sinusoidal modulation technique. The output voltage in them has two levels: zero and positive supply dc voltage levels in the positive half cycle making the harmonic components of the output voltage dependent on the carrier frequency. In order to expel these shortcomings, Sung-Jun Park proposed a 5-level PWM inverter which synthesizes five voltage levels per cycle. This inverter topology attenuated the harmonic components of the output waveforms compared with that of traditional full-bridge 3-level PWM inverter under symmetric dc voltage source and switching frequency.

This paper presents a three-phase, 9-level hybridised multi-level cascaded inverter topology, providing nine voltage levels per cycle per phase at the inverter output terminals. An additional clamping switch has been connected to improve the overall harmonic profile of the output waveforms. The major advantage is that the component-count of the proposed inverter configuration is highly reduced when compared with the conventional CHB inverter, for similar output voltage and levels. Principles of operation and the switching functions are discussed in detail. Simulations in MATLAB/Simulink results are discussed to verify the validity of the three phase inverter topology.

II. SMART GRID OPERATION

Most present generation grids have not altered for many decades and this characteristic of not evolving is a loss to the power sector. It is pitiful to be dependent on techniques that involve human interrogation and operation for faults occurring over an electrical grid. A century before today, electricity generation and consumption was limited to a few groups; and over time, development has been done by getting all the electrical grids on to a common frame, by interconnecting everything to a grid. This interconnection resulted in a massive grid that runs on a complex architecture and control strategy that is difficult to control and deal with. Recent advances in technology is giving options of updating the electrical grids to be smart in nature. As per the definition by National Institute of Standards and Technology(NIST), USA, a smart grid is "A modernized grid that enables bidirectional flows of energy and uses two-way communication and control capabilities that will lead to an array of new functionalities and applications"[28]; which means that the grid must be able to feed the load, and it must also be in a position to take energy from load points to be utilized at a place where there is requirement of power; and this power must be able to controlled and utilized in any way possible. As per Reference 29, Dr. S. Chakrabarti of IIT Kanpur states IEE defines smart grid to consist of the power and energy layer, the communication layer, and the IT/computer layer; which is a representation of the most important sections of the smart grid. The power and energy layer consist of the existing grid is to be interconnected to the various micro-grids, and the communication layer states the utilization of data collected from sensors connected over a smart grid and the IT/computer layer handles the data collected and requires coding to take the necessary action as and when needed. A smart grid typically consists of a number of sensors placed at the consumer, transmission and distribution sectors which are combinedly called as a smart grid. A smart grid can recognize a fault anywhere in the grid and take necessary action to isolate the fault causing path and also to reroute power to the power dependent loads so that less loads are affected by the outage. Also, the sensors placed properly help in identifying any fault accurately along with the location so that necessary action can be taken imminently to rectify the fault. Apart from this a smart grid has the capability to adapt to the load changes; the entire system is connected to the smart grid, and this enables the switch on and switch off of necessary units as per the load demand. A smart grid also does the task of collection and analysis of data through the cooperation of the consumer; i.e. the system collects data over a period of time, and algorithms are developed to understand and predict the increase or decrease of load requirement and thereby the system acts accordingly. Automation can be achieved without human intervention if a smart grid is installed perfectly. The inverter used in this chapter has the capability to function to satisfy the needs of a smart grid. Since renewable energy sources are not continuous or constant in nature, the smart grid adapts to the load requirement and draws power from suitable sources to maintain the load. This capability of the smart grid is very important as the main reason for blackouts or failing of a grid is due to unstable load requirements.

A smart grid uses advanced techniques to process the data available and it helps the grid to be ready and prevent any kind of power outage, as there is data available about the load requirement changes. The smart transmission grid control center shown in Figure 1 controls the entire operation of the grid; it controls when a source is to be connected to a grid, when to disconnect a faulty load and when to increase the power generation and when to decrease the generation i.e. it is like the central processing unit of the entire grid that controls through all the data available through the sensors. The communication infrastructure plays the role of collection of data to be processed by the smart transmission grid control center and also to send control signals to the required device when needed. It communicates with all the components available on the grid and gives instructions to them i.e. to control the operation of a circuit breaker, to send power through a different path after rerouting, etc. While connected to a smart grid, advanced technology of using a smart energy meter result in consumer's control of their load. The consumers can have a clear picture of the loads being used by them and over a period of time; thereby helping them reduce their load if possible during peak hours to help the environment and to prevent any outages in the grid. And since majority of the power bill is generated based on usage during peak hours, the consumer has the option to reduce the power consumption cost by using automation or Internet of things[30] to use certain power consuming loads

during low demand hours that is advantageous to both the consumer as well as the grid integrity. Smart grid takes time to be implemented over the entire grid, but once implemented properly, it results in a flawless grid with minimal losses.

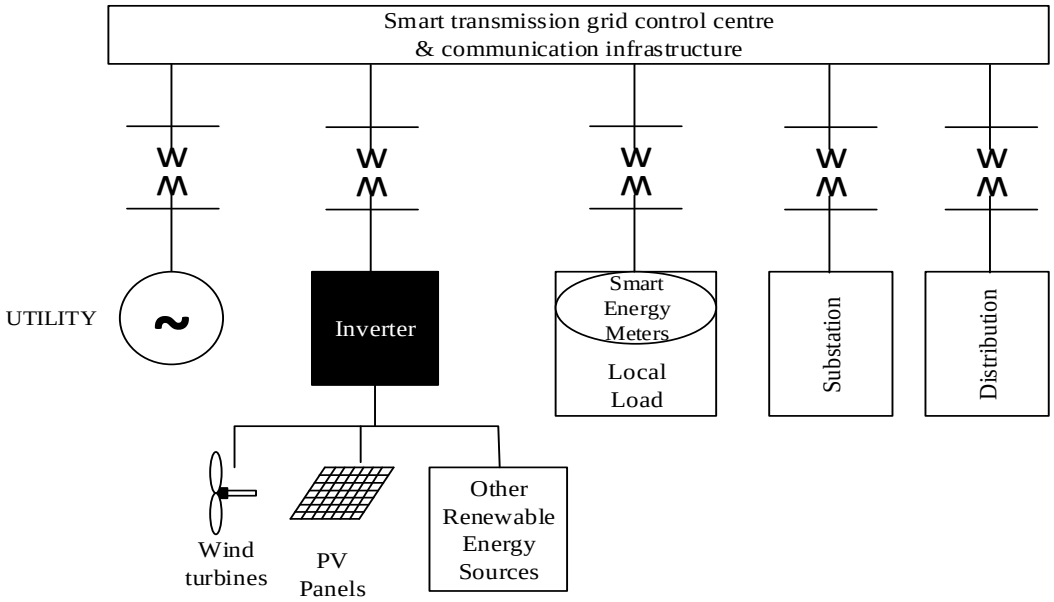

Fig. 1 Smart grid representation along with the inverter

III.BASIC INVERTER TOPOLOGY

The proposed three-phase, 9-level cascade multi-level inverter, whose one phase is shown in Fig. 2is a cascaded multi-level inverter. Each of the two cells comprises a conventional H-bridge with one bidirectional switch connected to the center point of two dc sources. Proper switching of the inverter results in nine output-voltage levels: V_A, $2V_A$, $3V_A$, $4V_A$, 0, $-V_A$, $-2V_A$, $-3V_A$, $-4V_A$. The highest number of voltage levels attainable by cascading x-number of 5-level inverter is 4x + 1.

Similar result was obtained by cascading NPC converter with a higher number of switching components. The additional switches G_{1L} and G_{1R} must be properly switched for controlling the direction of the load current. Table 1 shows the switching combinations that generated the nine output voltage levels (V_A, $2V_A$, $3V_A$, $4V_A$, 0, $-V_A$, $-2V_A$, $-3V_A$, $-4V_A$).

The switching functions of a phase of the proposed three-phase 9-level hybridised cascaded multi-level inverter are realized by the use of basic logical AND, OR and NOT gates, which are as given in equations 1-10 in Section 4.The inverter is a robust model which can be used for different modulation indexes too. The area of discussion in this chapter confines to a modulation index of 1 with crucial voltage identification being the main aim. All the switches used are IGBTs which are controlled by a PWM scheme are discussed in Section 4. A single phase output has been discussed in detail as other phases correspondingly produce the same output.

The actual representation of a single phase in the proposed three phase inverter is shown in Fig.2.with ten IGBTs and 16 Diodes; and 4 symmetric sources. A hardware implementation can be incorporated by selecting devices as per the magnitude of the sources used. The main area of study is regarding the operation of the inverter.

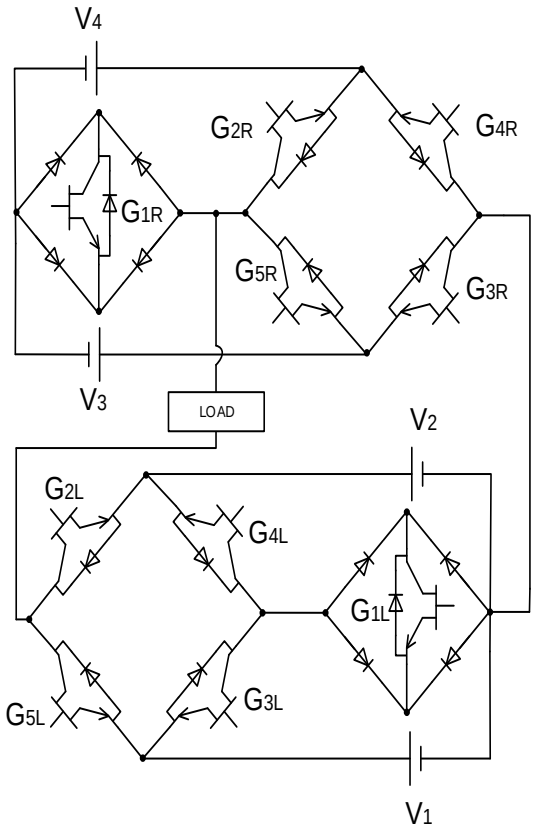

Fig. 2 1-phase of the proposed inverter model

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Table. 1 Switching combinations for a single phase

G_{1L}	G_{2L}	G_{3L}	G_{4L}	G_{5L}	G_{1R}	G_{2R}	G_{3R}	G_{4R}	G_{5R}	V_0
0	0	1	0	0	1	0	1	0	0	V
0	0	1	0	0	0	1	1	0	0	2V
1	0	1	0	0	0	1	1	0	0	3V
0	1	1	0	0	0	1	1	0	0	4V
0	0	1	0	0	0	0	1	0	0	0V
0	0	0	0	1	0	0	0	0	1	0V
0	0	0	1	0	1	0	0	1	1	-V
0	0	0	1	0	0	0	0	1	1	-2V
1	0	0	1	0	0	0	0	1	1	-3V
0	0	0	1	1	0	0	0	1	1	-4V

The switching pattern of the gate pulses are as given in Table 1. The table describes each and every switching pattern for producing each level in the output. The switching table changes for phases B and C as per the reference waveform used. Since the input voltage sources are all symmetrical, the output V_0 is referred as V, 2V, 3V, 4V, -V, -2V, -3V, -4V in the given table.

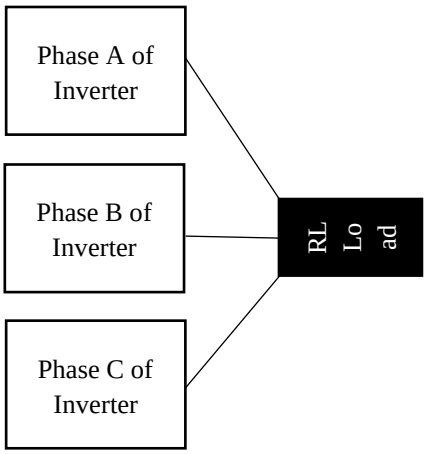

Fig. 3 Three phase layout of the proposed inverter

IV.MODULATION TECHNIQUE

The entire power electronic circuit of an inverter is controlled by the modulation technique of the inverter. A phase disposition pulse width modulation scheme is used to control the firing pulses of the switches. A reference waveform which is a sinusoidal signal of frequency 50Hz in this case is compared with carrier waveforms, which are triangular pulses with a frequency of 5KHz are used for the generation of pulses to control the switches. The governing equations of the topology are shown from equations 1-10.

$$G_{1L} = \bar{R} \leq C_1 \quad (1)$$

$$G_{2L} = \overline{(\bar{R} \leq C_1)} + (\bar{R} \leq C_2) \quad (2)$$

$$G_{3L} = \overline{(\bar{R} \leq C_2)} + (\bar{R} \leq C_3) \quad (3)$$

$$G_{4L} = \overline{(\bar{R} \leq C_3)} + (\bar{R} \leq C_4) \quad (4)$$

$$G_{5L} = \overline{(\bar{R} \leq C_4)} \quad (5)$$

$$G_{1R} = R \leq C_1 \quad (6)$$

$$G_{2R} = \overline{(R \leq C_1)} + (R \leq C_2) \quad (7)$$

$$G_{3R} = \overline{(R \leq C_2)} + (R \leq C_3) \quad (8)$$

$$G_{4R} = \overline{(R \leq C_3)} + (R \leq C_4) \quad (9)$$

$$G_{5R} = \overline{(R \leq C_4)} \quad (10)$$

Where G_{1L}, G_{2L}, G_{3L}, G_{4L}, G_{5L}, G_{1R}, G_{2R}, G_{3R}, G_{4R}, G_{5R} are the gate pulses generated, R is the rectified sinusoidal reference waveform, C_1, C_2, C_3, C_4 are carrier triangular waveforms of 5kHz ranging from [0-0.25], [0.25-0.5], [0.5-0.75], [0.75-1] respectively.

V.SIMULATION RESULTS

MATLAB's SIMULINK environment is used for the simulation of the proposed three phase topology and processing of the gate signals used to drive the circuit components. This is a symmetric modulated inverter and the output voltage is the sum of the input voltage sources used. This topology was simulated with V_1=V_2=V_3=V_4=12.5V per phase in the present simulation; the detailed results of a single phase of the simulated topology i.e. the reference, carrier signals and gate pulses has been shown in Figure 4, and the three phase output has been shown in Figure 5. The load used is an RL-load of 10Ω, 100mH per phase.

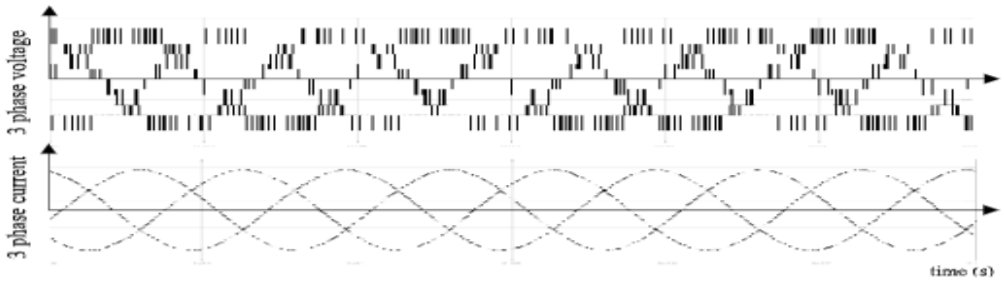

Fig. 4 Three phase output voltage and current observed

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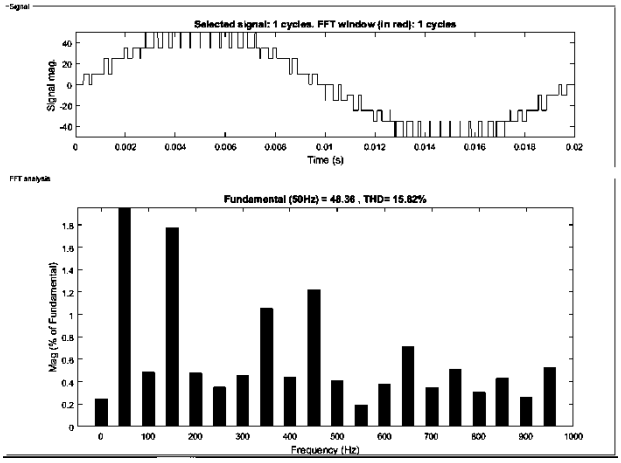

Fig. 5 THD of a phase of the three phase inverter

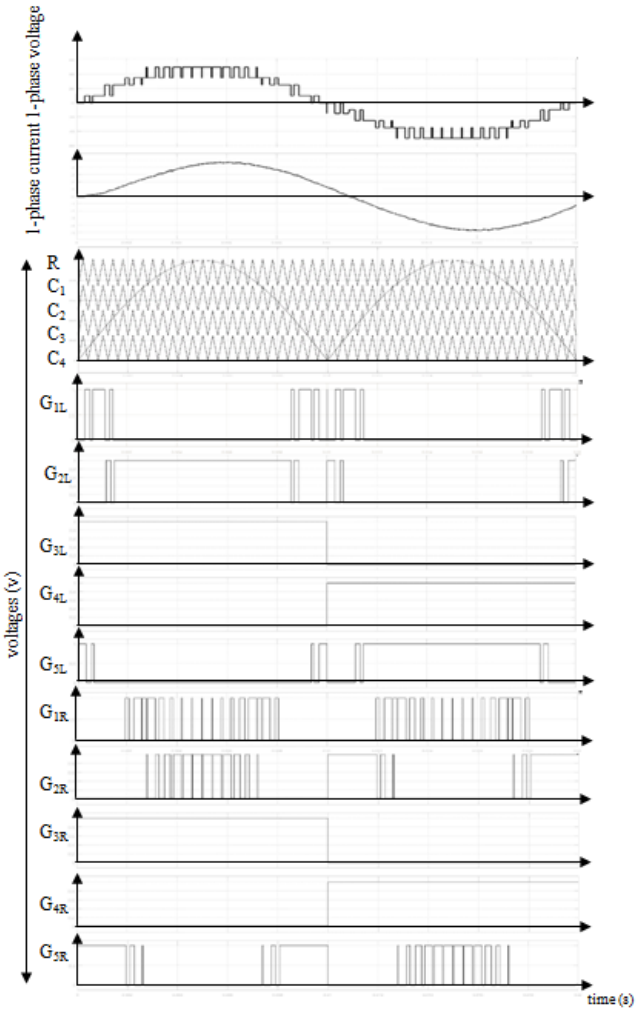

Fig. 6 Single phase output voltage and current with corresponding gate pulses

VI.CRUCIAL VOLTAGE IDENTIFICATION

A crucial voltage source is that which when disrupted would change the circuit's parameters to the maximum. Simulation tests have been carried out to recognize the crucial voltage in the proposed topology so as to take the necessary precautions when implemented in hardware. Recognizing the crucial voltage source enables us to select a source of consistent magnitude at the crucial source point so as to avoid any derange in the circuit output.

Case 1 (When V_1=0V)

The voltage source V_1 is set to zero in simulation, so as to observe the behavior of the proposed topology. The voltage and current vary as shown in Fig. 7and the harmonic distortion is shown in Fig. 8.

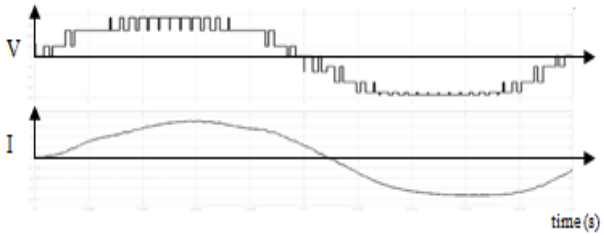

Fig. 7 Voltage and current when V_1=0V

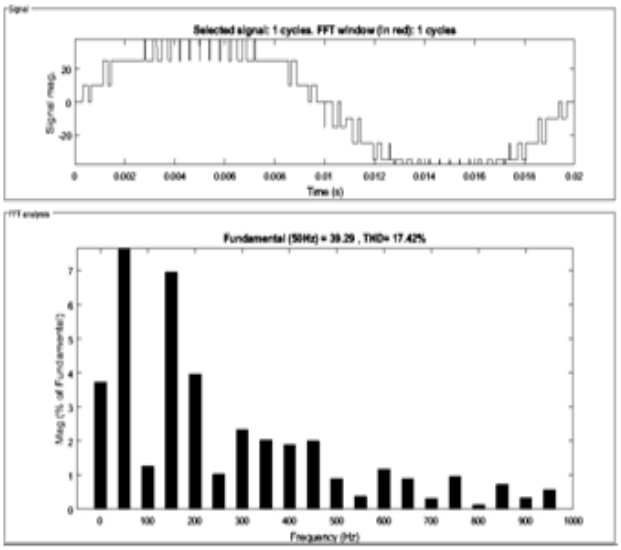

Fig. 8 THD at the condition when V_1=0

The number of voltage steps are reduced to 7 and the THD is increased to 17.42%.

Case 2 (When V_2=0V)

The voltage source V_2 is set to zero in simulation, so as to observe the behavior of the proposed topology. The voltage and current waveforms generated are as shown in Fig.9and the harmonic distortion is as shown in Fig.10.

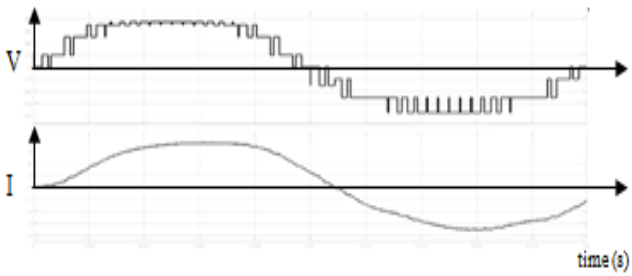

Fig. 9 Voltage and current when V_2=0V

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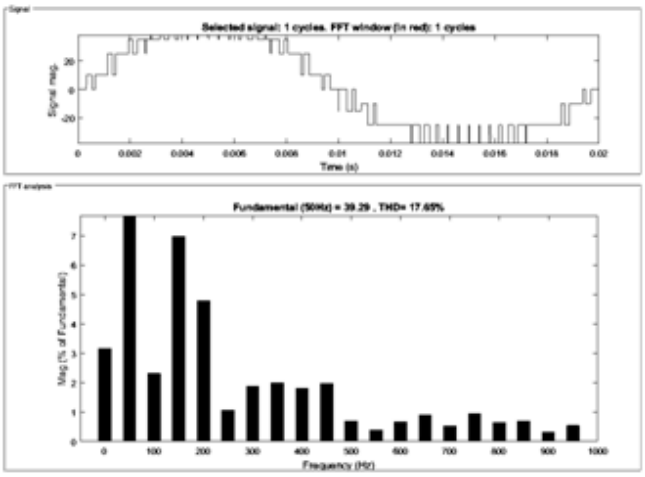

Fig. 10 THD at the condition when V_2=0

The number of voltage levels are reduced to 7 and the THD is increased to 17.65% which is higher than the case when V_1=0.

Case 3 (When V_3=0V)

The voltage source V_3 is set to zero in simulation, so as to observe the behavior of the proposed topology. The voltage and current waveforms generated are as shown in Fig.11.and the harmonic distortion is as shown in Fig.12.

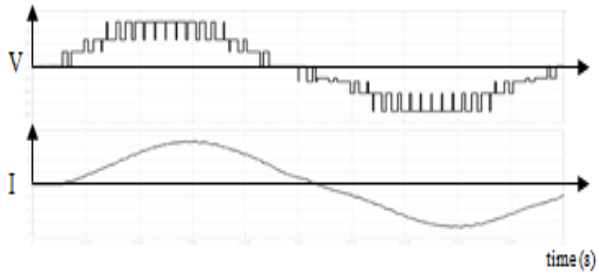

Fig. 11 Voltage and current when V_3=0V

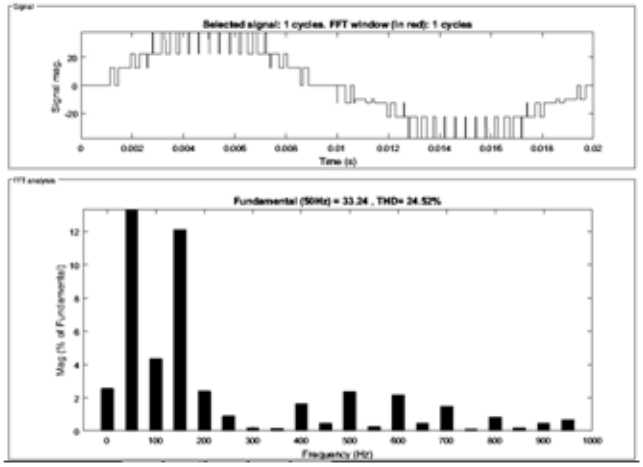

Fig. 12 THD at the condition when V_3=0

The number of voltage steps are reduced to 7 and the THD is increased to 24.52% which is higher than the case when V_1=0 and V_2=0.

Case 4 (When V_4=0V)

The voltage source V_4 is set to zero in simulation, so as to observe the behavior of the proposed topology. The voltage and current vary as shown in Fig.13and the harmonic distortion is as shown in Fig.14.

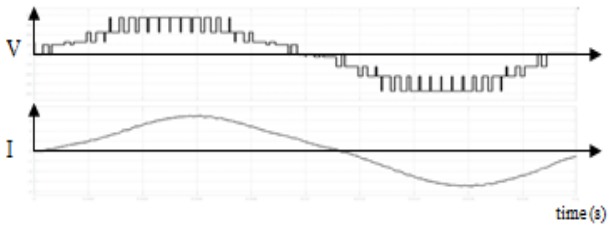

Fig. 13 Voltage and current when V_4=0V

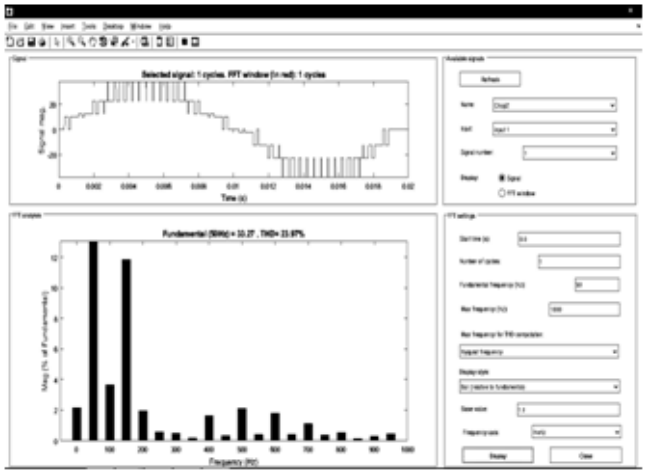

Fig. 14 THD at the condition when V_4=0

The number of voltage levels are reduced to 7 and the THD is increased to 23.59%. which is higher than the case when V_1=0 and V_2=0, but lesser than the case when V_3=0.

VII.RESULTS &DISCUSSIONS

A Three Phase 9-Level Hybridised Cascaded Multi-Level Inverter for use in Smart grid was implemented and its crucial voltage was identified in this paper. The proposed three phase topology can be implemented in a smart grid comprising of similar voltage magnitude sources. The ability to monitor and control the switching pulses results in complete control and working of the inverter linked with the smart grid. The exhibited harmonic profile is reasonable at 15.82% and the crucial voltage identification test resulted in the harmonic distortions of 17.42% when V_1=0, 17.65% when V_2=0, 24.52% when V_3=0, and 23.59% when V_4=0; this test shows that $V_3$is the most crucial voltage source in the inverter setup in of the available three phases.

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So, special precautions must be considered during hardware implementation to keep the voltage source 3 in all the phases stable.

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