Crucial Voltage Identification of a Seven Level Multilevel Inverters using AMM for Microgrid Applications

B.K.Karunakar Rao, K. Vaisakh

Abstract: ***This paper presents a single-phase efficient and generalized basic topology that is adaptable for multilevel inverters. The proposed structure is run by a switching pattern of the power switches i.e, subharmonic pulse width modulation (SHPWM) or comparison of triangular carrier high-frequency waveforms with a sinusoidal reference waveform. This chapter shows an asymmetric modulation method (AMM) hybrid modulation inverter with its working and performance verified through the simulation studies conducted in MATLAB Simulink software. A test for crucial voltage identification has also been carried out that recognizes the most important voltage source that must be maintained constant, else it would adversely effect the circuit's operation.***

Keywords: converter; hybrid inverter; novel topology

I. INTRODUCTION

The increase of power demand through the years puts a strong effect over the environment. The multilevel inverters play a significant role in diminishing the gap between enhancing the demand and production of power. From many years low voltage inverters are available but high power and high voltage inverters are needed in the industry. Multilevel inverters can handle low and medium power to high power and high-frequency standards with various switching patterns. Multilevel inverters are normally designed with isolated dc input sources or a series capacitors bank to generate sinusoidal waveforms as output. The advantage of multilevel inverters is they form a waveform with minute voltage steps for getting very low harmonic distortion and less amount of dv/dt.Most of the applications are utilizing multilevel traditional inverters.[1-4], Fundamental multilevel inverters[5-7] and cascaded multilevel inverters. The circuit design and desired results of an inverter depend on the switching pattern of a control circuit, the output of controllers are nothing but a pulse train of average time.[8], using some conventional carrier-based sinusoidal PWM techniques some techniques involved in minimizing the harmonic distortion. Modulation methods basically target to produce pulse trains along with average time and collaboration of reference sinusoidal waveforms with carrier signals [10-11].

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Multilevel inverters nowadays are realized with many modulation methods like subharmonic PWM (SHPWM), selective harmonic elimination PWM (SHEPWM), space vector PWM (SVPWM) and some hybrid modulation methods, etc.[12-21]

The method of modulation technique used in the proposed asymmetrical multilevel inverter basically evolved from the hybrid modulation methods[18-20]. In this proposed asymmetrical cascaded multilevel inverter concept of asymmetrical modulation method is used for obtaining the desired result[22-23]. in this concept it is observed that low power cells are producing high-frequency PWM waveforms and rest of them produce a low frequency stepped waveforms and collectively work to get the PWM waveform.

This chapter is proposes single phase generalized structure for multilevel inverters as to having an advantage of structural savings as well as optimum improvement in performance. The reduction in the count of the components used results in a further decrease in power losses and thereby increases the overall efficiency of the proposed topology. For a similar number of levels, this topology results in reduction of components used compared to the cascaded H-bridge and other previously existing topologies.

The equations that guide the multicarrier modulation technique are given along with the working of the inverter under various operating conditions in the MATLAB/Simulink platform to explore the performance of the proposed structure.

II. BASIC INVERTER TOPOLOGY

The proposed single-phase, 7-level generalized multilevel inverter is a combination of DC sources connected as separate H-bridges in series as shown in figure1. The results of each individual dc sources are collectively controlled to give the circuit output. The proposed topology's switching pattern is designed taking care not to switch on parallel switches at once to prevent a short circuit in the structure during operation. The proposed topology is capable of producing seven voltage levels and different output voltage levels synthesized by different switching patterns.

There are numerous switching strategies available for controlling an inverter accurately and for developing a switching pattern based on comparison between single modulation waveform per phase and high-frequency carrier signals as shown in the figure.2, there are three kinds of carrier signal dispositions taken into account they are 1)

alternative phase (APO), 2) phase opposition (PO) and 3) phase homology.

III. MODULATION STRATEGY FOR SUGGESTED MODULE

The switching functions of the proposed single-phase 7-level generalized multilevel inverters are realized by the use of basic logical AND, OR and NOT gates, which are as given in section 4.

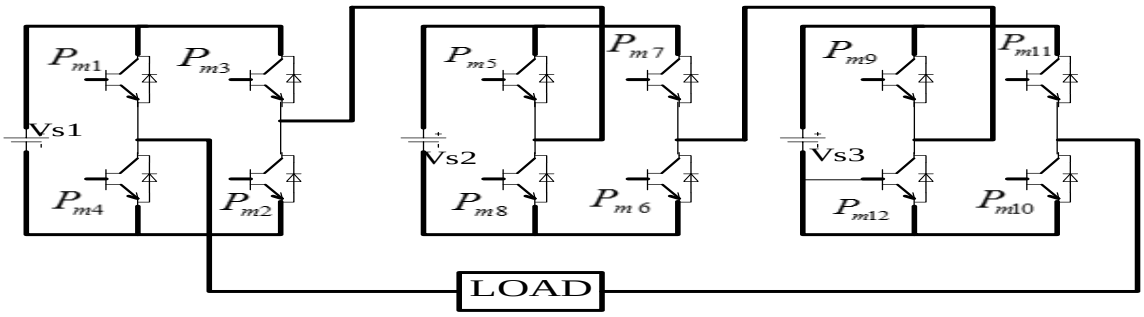

Fig. 1 phase of the proposed inverter model

The reference wave is a sinusoid with frequency f_r and amplitude A_r, the carrier signals for N-level inverter uses N-1 carrier signal of the frequency f_c and peak-peak amplitude A_c, and so the carrier signals come adjoining each one. The reference wave at zero level is put in the middle of the carrier signals. If the reference waveform is higher than triangular then switch operation is ON, if the reference signal is less than carrier signals the switch operation goes to OFF condition.

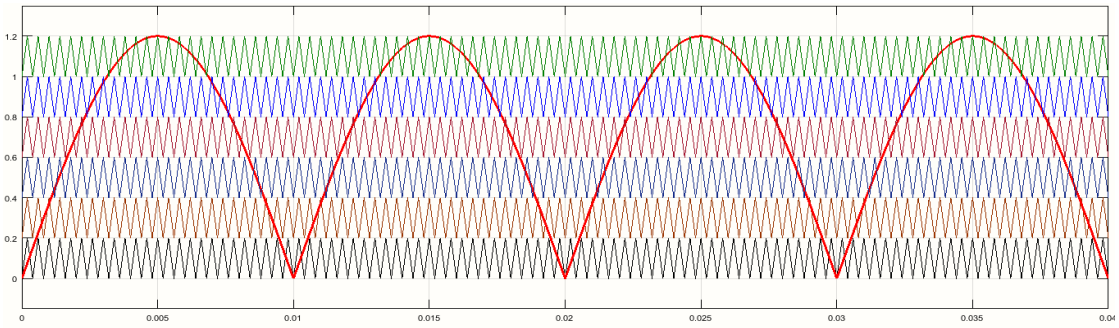

Fig. 2 single phase MLI carrier signals and reference signal R

IV. PULSE GENERATING EQUATIONS

$$P_{m1} = [(Abs(ref) > T_{g1}).U_1)] + [(Abs(ref) < T_{g1}).\overline{U_1})] \quad (1)$$

$$P_{m2} = ref < 0 \quad (2)$$

$$P_{m3} = ref > 0 \quad (3)$$

$$P_{m4} = [(Abs(ref) < T_{g6}).U_4)] + [(Abs(ref) > T_{g1}).\overline{U_4})] \quad (4)$$

$$P_{m5} = [(Abs(ref) > T_{g3}).U_5)] + [(Abs(ref) > T_{g2}).\overline{U_5})] \quad (5)$$

$$P_{m6} = ref > 0 = P_{m7} \quad (6)$$

$$P_{m8} = [(Abs(ref) < T_{g2}).U_8)] + [(Abs(ref) > T_{g3}).\overline{U_8})] \quad (7)$$

$$P_{m9} = [(Abs(ref) > T_{g4}).U_9)] + [(Abs(ref) < T_{g5}).\overline{U_9})] \quad (8)$$

$$P_{m10} = ref > 0 \quad (9)$$

$$P_{m11} = \overline{ref > 0} \quad (10)$$

$$P_{m12} = [(Abs(ref) < T_{g5}).U_{12})] + [(Abs(ref) > T_{g4}).\overline{U_{12}}) \quad (11)$$

Where P_{m1}, P_{m2}, P_{m3}, P_{m4}, P_{m5}, P_{m6}, P_{m7}, P_{m8}, P_{m9}, P_{m10}, P_{m11}, P_{m12} are the gate pulses required for controlling the circuit, R is the sinusoidal reference waveform, C_1, C_2, C_3, C_4, C_5, C_6 are carrier waveforms of 0.2, 0.4, 0.6, 0.8, 1, 1.2 respectively.

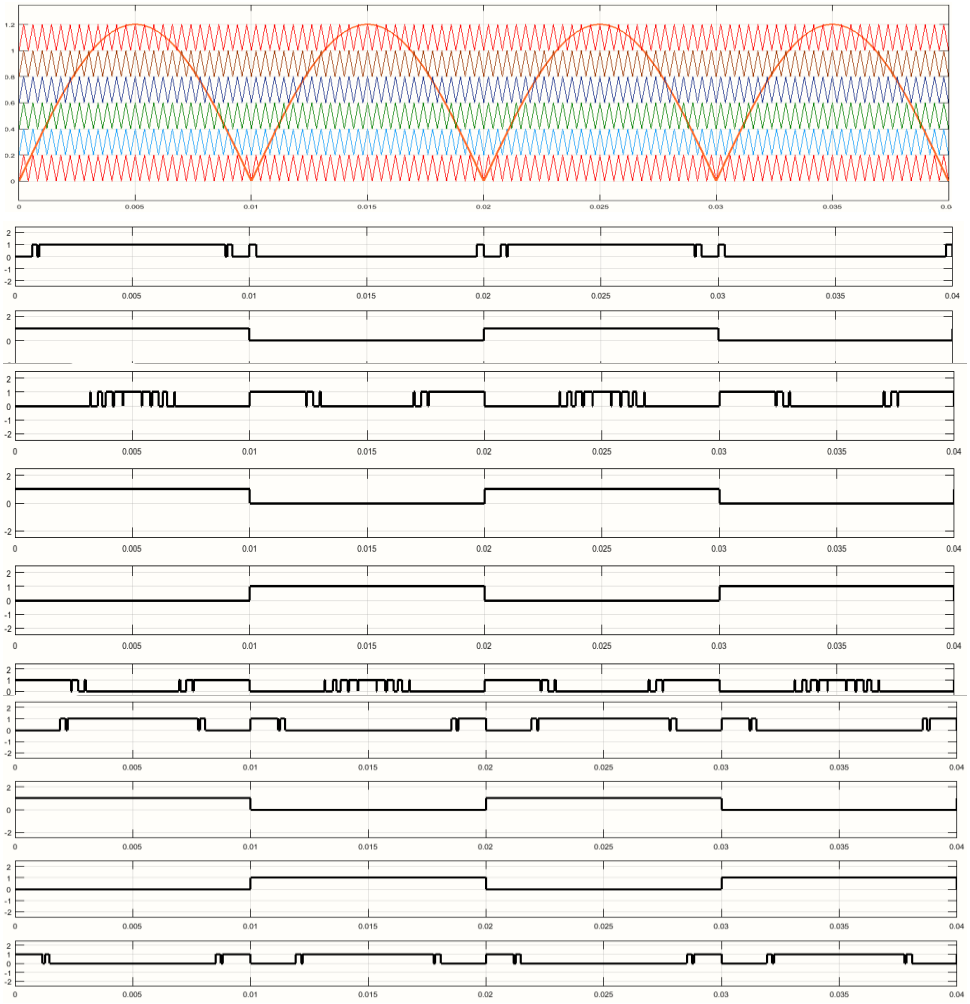

Fig. 3 seven level cascaded MLI carrier signals encounter with reference signal and corresponding gate signals

Fig.4 shows the seven levels of cascaded multilevel inverter, its resultant output V_{out} is the sum of the all unit outputs V_{s1}, V_{s2} and V_{s3}.This asymmetric modulation method is derived from hybrid modulation method. The output voltage is sinusoidal stepped waveform formed by the units of outputs V_1, V_2, V_3 respectively. So the desired output is the summation of V_1, V_2, and V_3.

Multicarrier PWM and space vector modulation techniques are of prominence in the field of multilevel inverter [16], but these control schemes are generally used for switching of higher frequencies. In this paper, the inverter is controlled by lower frequency; the main consideration being prevention of short circuit. Multicarrier PWM approach has been utilized in the present topology where carrier signals are compared with sinusoidal signal. There are eight carrier signals at 0.2, 0.4, 0.6, 0.8 and -0.2, -0.4, -0.6, -0.8, and two reference sinusoidal waveforms are used with a peak of 1V.The THD of the active system is 18.67%., shown in fig.5

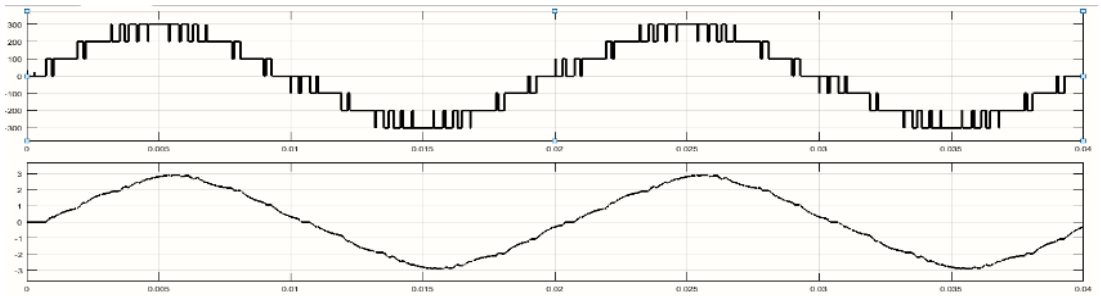

Fig. 4 seven level cascaded MLI resultant output voltage & current waveform

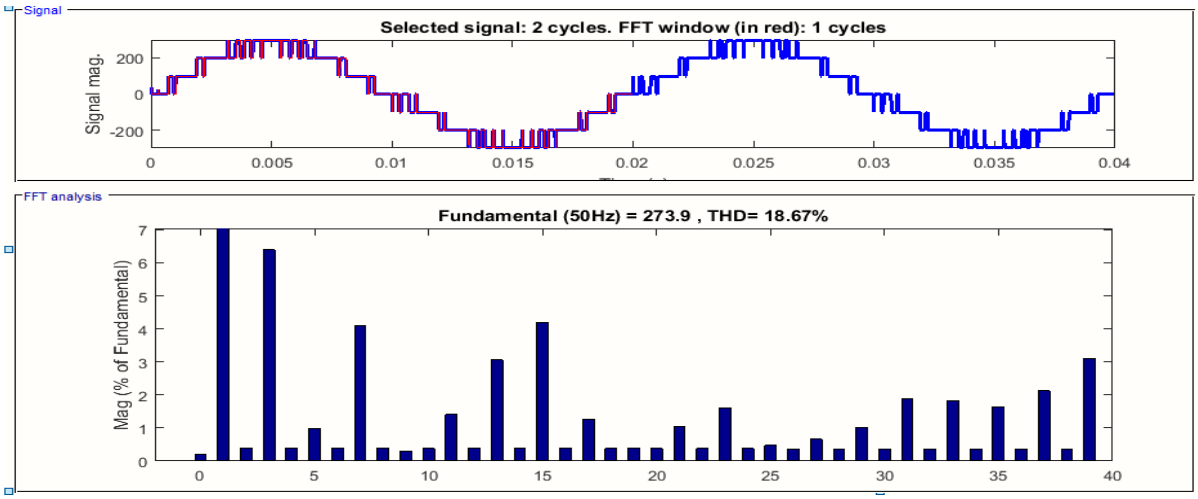

Fig. 5 FFT Analysis of a Single phase of output voltage waveform, THD = 18.67%

V. CIRCUIT SIMULATION RESULTS

Identification of Crucial Voltage of Single Phase Seven Level Asymmetrical Multilevel Inverter

The simulation results of the waveforms are shown along with the corresponding FFT analysis spectrum from figure 6 to 11and the output waveform parameters show that voltage source number 1 is the most crucial voltage source as maximum THD is observed when voltage source 1 is removed.

Case 1: V_1=100V, V_2=100V, V_3=0V

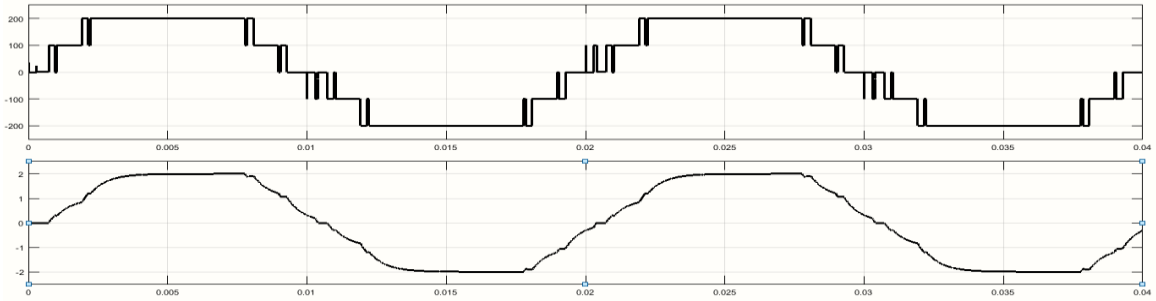

Fig. 6 Single phase of output voltage and current waveform when V_3= 0V

From Figure 6,it can be observed that the output voltage yields 200V, because the V_3 voltage source is switched off i.e, the third voltage source is disabled from the circuit and the resultant voltage is 200V with seven levels in output and peak to peak voltage is 400V and RMS Value is 162V.The waveform for current is noted to be having a peak of 2 A while having 7 levels of voltage with a peak of 200V as shown in the figure. Peak to peak and RMS Values of currents are 4A and 1.58A.

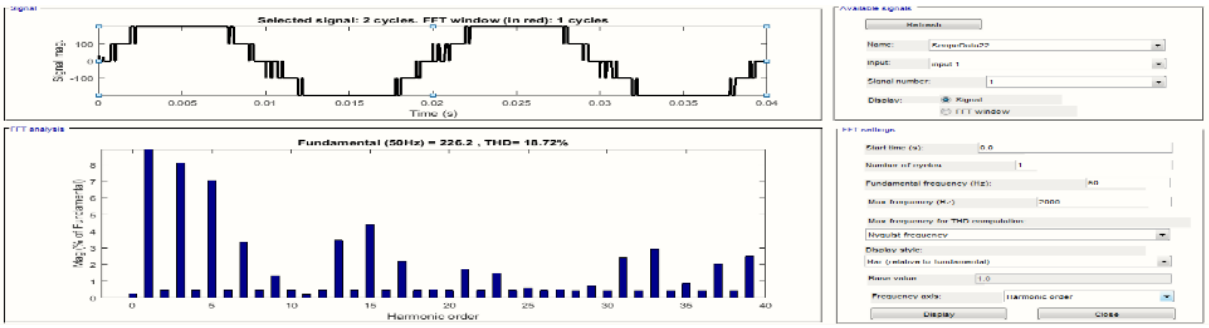

Fig. 7 FFT Analysis of a Single phase of output voltage waveform when V= 200V, THD=18.72%.

Harmonic spectrum of the line-line voltage with fundamental frequency of 50Hz and a corresponding carrier frequency of 2K Hz yields a THD of 18.72% as shown in Figure. 7

Case 2: V_1=100V, V_2=0V, V_3=100V

When V_2 is short circuited, it is observed that the output voltage has a reduced number of levels when compared to the actual design of the circuit. There are 5 levels observed in output and the resultant voltage has shifted its origin to -1 on Y-axis. The positive half cycle above zero on the y=0 axis has three levels and the negative half cycle below zero on the y=0 axis has 2 levels similar to the case when V_3=0. The variation in the current waveform is shown in Figure 8.

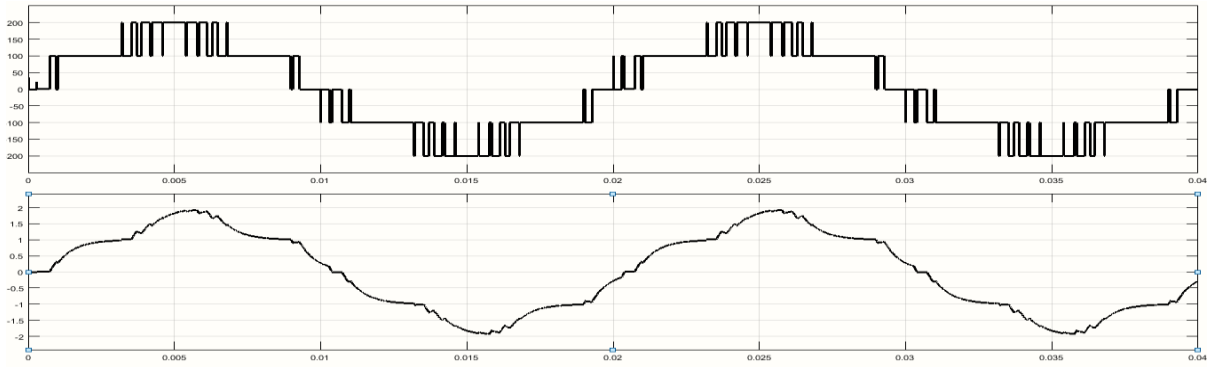

Fig. 8 Single phase of output voltage &current waveform when V_2=0.

Study of the output current waveform when V_2=0 shows a reduced positive peak at 1.93A and a negative surge near the origin. The negative peak of -1.93A remains unchanged for this case of operation. The output is similar to the case when V_1=0 and the output voltage THD analysis is as shown in Figure.9.

The current waveform observed has a peak of 1.93A with five levels when voltage sources like 100V, 0V, 100V. The peak to peak and RMS current values are 3.86A and 1.19A respectively.

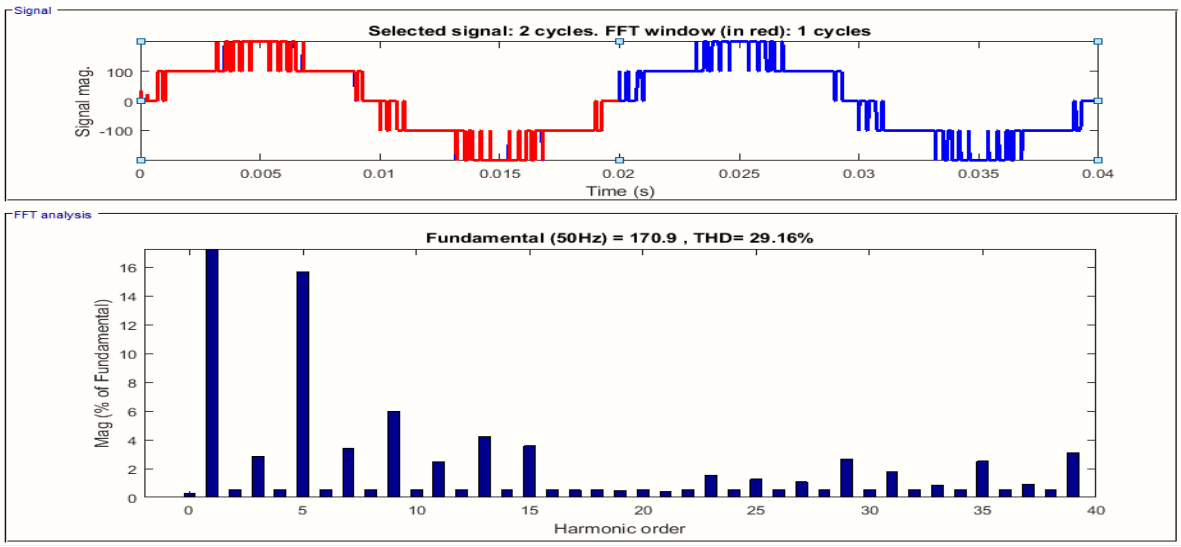

Fig. 9 FFT Analysis of a Single phase of output voltage waveform when V= 200V, THD=29.16%

From Figure.9, it can be observed that the THD of the output waveform has increased by 29.16% relative to its original harmonic distortion when V_2=0 and it is better than the output when V_3=0 (THD=18.72%), and this shows that the circuit's operation is adversely affected by the short circuit in voltage source 2.

Harmonic spectrum of the line-line voltage with fundamental frequency of 50Hz and a corresponding carrier frequency of 2K Hz a THD of 29.16% has shown in Figure.9.

Case3: V_1=0V, V_2 =100V, V_3 =100V

When $V_1$is short circuited, it is observed that the output voltage has a reduced number of levels when compared to the actual design of the circuit. There are 5 levels observed in output and the resultant voltage has shifted its origin to -1 on Y-axis. The positive half cycle above zero on the y=0 axis has two levels and the negative half cycle below zero on the y=0 axis has 3 levels similar to the case when V_2=0. The variation in the current waveform is shown in Figure 10.

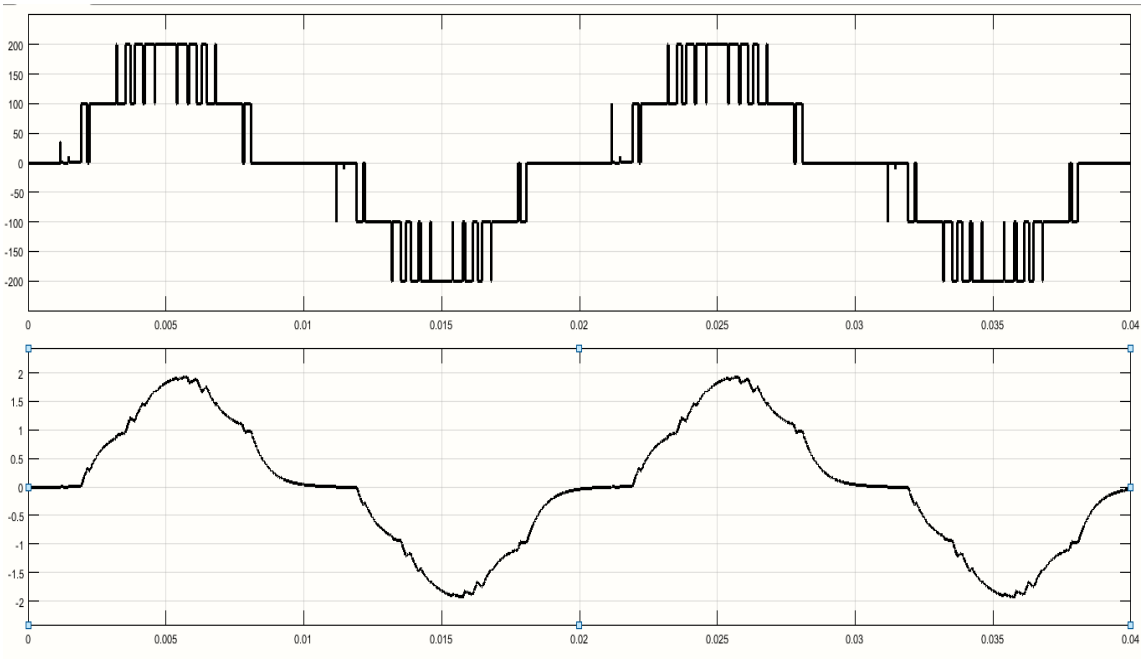

Fig. 10 Single phase of output voltage and current waveform when V_1=0V

The voltage waveform has peak of 200V with 5 levels when the voltage sources are 0V,100V and 100V, the peak to peak and RMS voltages are 400V and 115V respectively.

Study of the output current waveform when V_1=0 shows a reduced positive peak at 1.93A and a negative surge near the origin. The negative peak of -1.93A remains unchanged for this case of operation. The output is similar to the case when V_2=0 and the output voltage THD analysis is as shown in Figure.11.

The current waveform observed has a peak of 1.93A with five levels when voltage sources like 0V,100V, 100V. The peak to peak and RMS current values are 3.86A and 1.09A respectively.

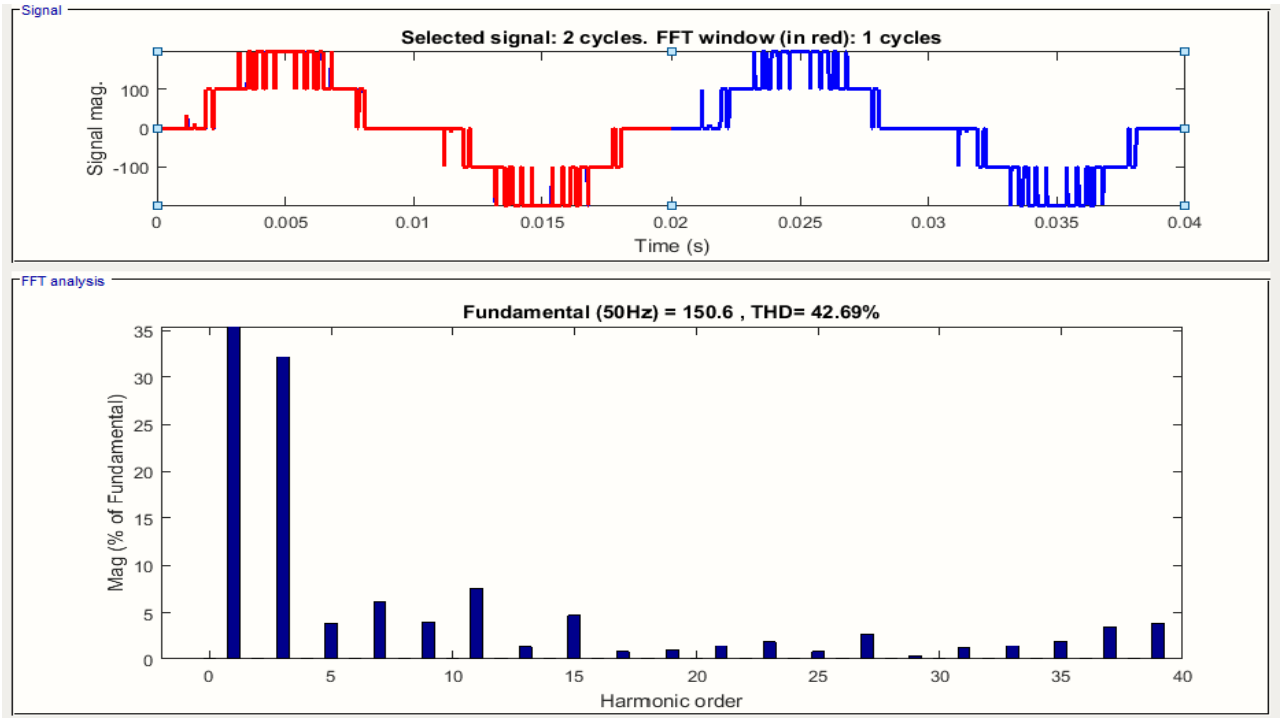

Fig. 11 FFT Analysis of a Single phase of output voltage waveform when V_1=0, THD=42.69%

Table. 1 Consolidated values of voltages, currents and THDs

S.No	I/p. Voltage	O/p.Voltage	Peak to Peak Voltage	RmsVoltage	O/p Current	Peak To Peak Current	Rms Current	THD	Fund.Freq	Max.Freq	N.oOf Levels
Case-1	100V, 100V, 0V	200V	400V	162V	2.0A	4A	1.58A	18.72 %	50Hz	2K	5
Case-2	100V, 0V, 100V	200V	400V	126V	1.93 A	3.86 A	1.19A	29.16 %	50Hz	2K	5
Case-3	0V, 100V, 100V	200V	400V	115V	1.93 A	3.86 A	1.09A	42.69 %	50 Hz	2K	5
Case-4	100V, 100V, 100V	300V	600V	197V	2.93 A	5.86 A	1.90A	18.67 %	50 Hz	2K	7

VI. CONCLUSION

Harmonic spectrum of the line-line voltage with fundamental frequency of 50Hz and a corresponding carrier frequency of 2K Hz a THD of 42.69% has shown in Figure. 11consolidated values of voltage, current and corresponding THDs are shown in table 1.

From Figure 11, it can be observed that the THD of the output waveform has increased by 42.69% relative to its original harmonic distortion when V_1=0 and it is shows more THD than the output when V_2=0 (THD=29.16%), and this shows that the circuit's operation is adversely affected by the short circuit in voltage source one.

The proposed MLI is a boost type MLI and the main advantage of this kind of MLIs are reduce count of device components used in the circuit design. A staircase voltage waveform is produced from this model and the suggested seven level model is used in a number of applications like medium voltage inverters for motor drive and PV cells working with multilevel grid-connected inverters which are working at high frequency. The entire work has been done in MATLAB software version 16a. The simulation results are verified and the analysis for the asymmetrical multilevel inverter has been described in detail. During physical realization care should be taken to keep the crucial voltage constant as that would disrupt the output with a high THD of 42.69%. The presented topology can be implemented using renewable energy sources for stable operation for a wide range of applications.

REFERENCES

1. Zhang, F., Du, L., Peng, F.Z., Qian, Z.: 'A new design method for high power high-efficiency switched-capacitor DC–DC converters', IEEE Trans. Power Electron. 2008, 23, pp. 832–840.
2. Hammond, P.W.: 'Medium voltage PWM drive and method'. US Patent 5 625 545, 1997.
3. Corzine, K., Familiant, Y.: 'A new cascaded multilevel H-bridge drive', IEEE Trans. Power Electron., 2002, 17, pp. 125–131.
4. Rodriguez, J., Moran, L., Pontt, J., et al.: 'High-voltage multilevel converter with regeneration capability', IEEE Trans. Ind. Electron., 2002, 49, pp. 839–846.
5. Nabae, A., Takahashi, I., Akagi, H.: 'New neutral-point-clamped PWM inverter', IEEE Trans. Ind. Appl., 1981, IA-17, pp. 518–523.
6. Meynard, T.A., Foch, H.: 'Multi-level conversion: high voltage choppers and voltage-source inverters'. 23rd Annual IEEE Power Electronics Specialists Conf., PESC '92 Record, 1992, vol. 1, pp. 397–403.
7. Suh, B.-S., Hyun, D.-S.: 'New N-level high voltage inversion system', IEEE Trans. Ind. Electron., 1997, 44, pp. 107–115.
8. Green, R.M., Boys, J.T.: 'Implementation of pulse width modulated inverter modulation strategies', IEEE Trans. Ind. Appl., 1982, IA-18, pp. 138–145.
9. Agelidis, V.G., Calais, M.: 'Application specific harmonic performance evaluation of multicarrier PWM techniques'. 29th Annual IEEE Presented at Power Electronics Specialists Conf. 1998, PESC '98 Record, 1998.
10. Holmes, D.G., Lipo, T.A.: 'Pulse width modulation for power converters: principles and practice' (IEEE Press, Hoboken, Wiley-Interscience, Piscataway, NJ, 2003).
11. Ben-Brahim, L., Tadakuma, S.: 'A novel multilevel carrier-based PWM control method for GTO inverter in low index modulation region', IEEE Trans. Ind. Appl., 2006, 42, pp. 121–127.
12. Mwinyiwiwa, B., Wolanski, Z., Ooi, B.-T.: 'Microprocessor implemented SPWM for multi converters with phase-shifted triangle carriers', IEEE Trans. Ind. Appl., 1998, 34, pp. 487–494.
13. Tolbert, L.M., Fang Zheng, P., Habetler, T.G.: 'Multilevel converters for large electric drives', IEEE Trans. Ind. Appl., 1999, 35, pp. 36–44.
14. Carrara, G., Gardella, S., Marchesoni, M., Salutari, R., Sciutto, G.: 'A new multilevel PWM method: a theoretical analysis', IEEE Trans. Power Electron., 1992, 7, pp. 497–505.
15. sTeodorescu, R., Blaabjerg, F.: 'Multilevel converter – a survey'. Presented at EPE '99, CD-ROM, 1999.
16. Rodriguez, J., Lai, J.-S., Peng, F.Z.: 'Multilevel inverters: a survey of topologies, controls, and applications', IEEE Trans. Ind. Electron., 2002, 49, pp. 724–738.
17. Wenxi, Y., Haibing, H., Zhengyu, L.: 'Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter', IEEE Trans. Power Electron., 2008, 23, pp. 45–51.
18. Zhichao, W., Yunping, Z., Ding, K.: 'An evaluation of spectral characteristic of novel hybrid asymmetric modulated 9-level inverter'. IEEE 36th Conf. on Power Electronics Specialists, 2005, pp. 855–860.
19. Ding, K., Yunping, Z., Zhan, W., Zhichao, W., Yun, Z.: 'Novel hybrid diode-clamp cascade multilevel converter for high power application'. Proc. Chinese Society of Electrical Engineering, 2004, vol. 24, pp. 62–67.

20. Manjrekar, M.D., Steimer, P.K., Lipo, T.A.: 'Hybrid multilevel power conversion system: a competitive solution for high-power applications', IEEE Trans. Ind. Appl., 2000, 36, pp. 834–841.
21. Rech, C., Pinheiro, J.R.: 'Impact of hybrid multilevel modulation strategies on input and output harmonic performances', IEEE Trans. Power Electron., 2007, 22, pp. 967–977.
22. Zhang, F., Du, L., Peng, F.Z., Qian, Z.: 'A new design method for high power high-efficiency switched-capacitor DC–DC converters', IEEE Trans. Power Electron., 2008, 23, pp. 832–840.
23. Hammond, P.W.: 'Medium voltage PWM drive and method'. US Patent 5 625 545, 1997.