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# Analytical Modeling and Simulation of Nanoscale Fully Depleted Dual Metal Gate SOI MOSFET

**Prashant Kumar, Munish Vashishath, P. K. Bansal**

***Abstract*: *The demand and development of scaled semiconductors devices for upcoming challenges in VLSI technology is unending. CMOS technology plays a very important role in fulfilling this criterion. The conventional MOSFET exhibits short channel effects (SCE) and performance degradation when scaled down in the nanometer regime. In order to meet the required enhanced performance and to further increase the device density new materials and new device structures have been developed. This paper analyses the performance characteristics of one of such improved device structure i.e Fully Depleted Silicon over Insulator (FDSOI) which also incorporate the gate having two metals of different work function specifically called Dual Material Gate (DMG) SOI MOSFET. The analytical modeling for this device structure has also been carried out. The simulation characteristics match closely with analytical results and as the surface potential profile of the device has step function in ensures that this device effectively reduces the SCE.***

***Index Terms*: *DIBL, DMG, Ion/Ioff, SCE, SOI, TCAD.***

## I. INTRODUCTION

It is very much evident that low power and high-speed semiconductor devices are the need of hours. These targets have somehow been achieved with improved design and with the introduction of new materials [1-2]. The device density is a major concern for VLSI circuits, to improve the device density the dimension of the semiconductor devices is reduced drastically. The MOSFET, which is the basic building block of many VLSI circuit, are also made smaller with the reduction in channel length. This channel length has now approached into nano regimes and with further reduction in this channel length, the control of gate on the channel of MOSFET degrade [3]. This degradation of control of gate is termed as Short Channel Effects (SCE), hence to further down scaling the channel length the control on SCE is required. These SCE not only result in a shift of threshold voltage but also affect device working with high drain voltage due to DIBL and hot electron effects [4].

The Silicon on Insulator (SOI) device structures has been proposed by many researchers [5-8], which promised to improve the SCE of MOSFET. The SOI structure has a very thin layer of silicon over the relatively thick oxide layer. This oxide layer isolates the thin silicon layer from silicon substrate which in turn reduces various parasitic capacitances and reduces the probability of latch-up occurrence in the circuit [9]. The SOI structure also best suited for scaling of devices as they provide the steeper slope due to which aggressive scaling of the threshold voltage is possible which is desired for low power application of semiconductor devices [10]. SOI MOSFET in comparison to it's counter parts provide better result in term of low power dissipation, low parasitics, high speed and reduced SCEs [11-12]. However, still, there are some SCE which arise when SOI is in nano regimes. To improve the SOI characteristics for very narrow channel device, many improved SOI structure is suggested by researchers [3,13-15]. The Dual Material Gate (DMG) is one of such structure having a metal gate made with two dissimilar metals having different work-function. In DMG the work function at drain side is kept lower than that of metal used in the gate at source side for N-MOSFET. The P-MOSFET is having the reverse order of work function metal on the gate. The difference in the work function of metal gates produces a step in the channel which effectively reduces the SCE. The paper discusses the gate material engineering where the performance comparison of DMG MOSFET with respect to bulk MOSFET is presented The device was simulated using Silvaco's TCAD software at 32nm channel length. The comparisons of the two structures were carried out in term of threshold voltages roll-off, DIBL, trans-conductance and on to off current ratio. The surface potential profile effectively shows the effectiveness of the semiconductor device in suppressing the short channel effects [16-17].

## II. SHORT CHANNEL EFFECTS

SOI devices were made to effectively suppress the SCEs but still, SOI devices are not able to completely free from SCE [15]. The short channel effects mainly found in SOI devices are kink effect (at high drain voltage, for transistor operating above threshold), self heating mechanism as the buried oxide makes a good thermal isolation to Silicon substrate, drain current overshoot, latch effect which is observed when SOI MOSFET operates at subthreshold region and complexity in formation of thin Silicon films [18-20].

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A few short channel effects observed in SOI are as

### A. Drain Induced Barrier Lowering (DIBL)

The barrier potential exists due to the difference of potential of the source and potential of channel region also a difference of diffusion and drift current in source and channel regions affect the barrier height [3]. The gate voltage controls this barrier height but in case of NMOS, the holes produced adjacent to drain region because of impact ionization, build up in device substrate and effectively bias the body with positive potential, which in turn reduces the threshold voltage [2]. For short-channel devices, this rate of holes generation due to impact ionization is increased with constant drain voltage. This result in floating body effects in SOI [21].

### B. Channel Length Modulation (CLM)

The increased drain voltage causes the increase in depletion region width towards the drain region and the effective length of channel reduces in case of short channel MOSFET [2]. This reduction in channel length is called channel length modulation. The effective channel length becomes equal to the difference of metal gate and depletion of drain and source regions. When the device channel length is effectively shorter, this effect is very dominating and may even result in punch through an effect when channel length effectively reduces to zero [22]. The channel length can be reduced by proper scaling and also with an increased doping density of the devices [5].

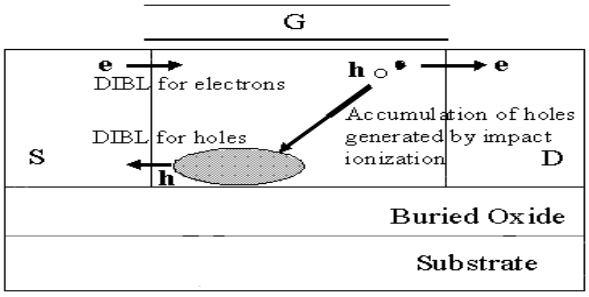


Figure 1. The mechanisms determining SCE in SOI MOSFETs [2]

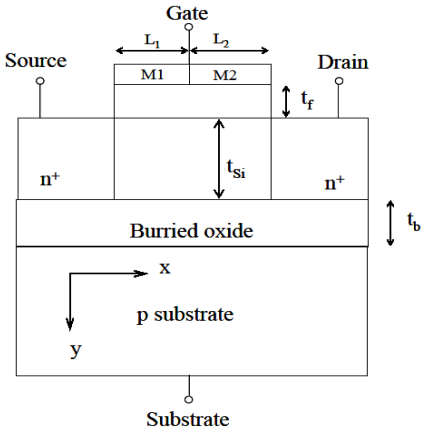


Figure 2. Cross-sectional Schematic of DMG-FD-SOI MOSFET

## III. DEVICE STRUCTURE

The 2D simulator ATLAS from Silvaco is used to produce the simulated schematic of the fully depleted dual metal gate SOI structure. The cross-sectional view is having a metal gate with metal 1 and metal 2 having length L1 and L2. The Molybdenum and aluminium are used for the formation of the gate of the structure. The gate towards the drain has lower work-function metal, result in a reduction in the maximum value of the electric field [3].

The 2D simulation of the device structure is carried out keeping the source and drain doping at $6x10^{21}$ $cm^{-3}$ and body is doped at $6x10^{15}$ $cm^{-3}$[21]. The gate oxide thickness for the front gate is 2nm, drain/source thickness is 4nm and the thickness of Silicon film is kept at 6nm. The other parameters used for FD-DMG-SOI simulation are as under in Table I.

Table I. Various simulation parameters specification

| **Device parameters** | **DMG** | **SMG** |
|---|---|---|
| Channel length (L) | 32nm | 32nm |
| Front gate oxide thickness($t_f$) | 2 nm | 2 nm |
| Drain/ Source Doping | $6 \times 10^{21} cm^{-3}$ | $6 \times 10^{21} cm^{-3}$ |
| Body doping ($N_A$) | $6 \times 10^{15} cm^{-3}$ | $6 \times 10^{16} cm^{-3}$ |
| Source/Drain thickness ($t_{Si}$) | 4 nm | 4 nm |
| BOX thickness ($t_b$) | 6 nm | 6 nm |
| ΦM for SMG gate | - | 4.24eV |
| ΦM for M1 | 4.5eV | - |
| Φ for M2 | 4.1eV | - |

## IV. METHODOLOGY AND MODELS

The device characteristics and surface potential profile were obtained by carrying out 2D simulation using Silvaco ATLAS [23]. The 2D simulation model uses the drift and diffusion model. In the high field regions, the FLDMOB mobility model has been used for velocity saturation [8]. Since the mobility depends upon temperature density of dopant, vertical and parallel electric field hence a CVT mobility model was utilized [8], which completely replicate the above characteristics. The Fermi carrier statics models were employed for the reduction of carrier density in high doping regions [21],

$$DIBL=(V_{Th\ HIGH}-V_{Th\ LOW}) / (V_{DS\ High}-V_{DS\ Low})$$

The work function for SMG SOI is taken as ΦM=4.24eV (Aluminium). The DMG SOI uses two metal having work-function as ΦM1=4.1eV (Molybdenum) 4.5eV (Aluminum) for better control of the gate.

## V. ANALYTICAL MODEL

Poisson's Equation was used to develop the analytical model of the DMG SOI [24]. The potential distribution of the surface in the channel is given by

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$$\frac{\partial^2 \psi_p(x,y)}{\partial x^2}+\frac{\partial^2 \psi_p(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{Si}}$$
$$0 \le x \le L; 0 \le y \le t_{Si} \quad (1)$$

Where p=1, 2

The potential distribution is approximated using the parabolic profile for DMG SOI MOSFET and solving the equation (1) further we get [24].

$$\psi_p(x,y)=B_0(x)+B_1(x)\,y+B_2(x)\,y^2 \quad (2)$$

The constant $B_0(x)$, $B_1(x)$ and $B_2(x)$ can be attained by substituting conditions at the boundary.

For obtaining surface potential, the corresponding boundary conditions are:

(1) Surface potential $\psi_s(x)$ depend on x only

$$\psi(x,y)=\psi_s(x) \quad (3)$$

(2) The center potential $\psi_c(x)$ depend on x only

$$\psi(0,y)=\psi_c(x)=B_0(x) \quad (4)$$

(3) The continuous electric flux for metal gate exist at the interfaces of the gates/oxide. Therefore,

$$\left.\frac{d\psi_p(x,y)}{dy}\right|_{y=t_{Si}}=\frac{C_{ox}}{\varepsilon_{Si}}(v_{gs}-\psi_p(x)-v_{fbp})=2yB_2(x) \quad (5)$$

Using the boundary condition equations [(3)-(5)] in the surface potential equation (2) and then substituting in equation (1).

Surface potential is expressed as

$$\frac{d^2\psi_s(x)}{dx^2}-\psi_s(x)\left(\frac{2C_{ox}}{\varepsilon_{Si}t_{Si}}\right)+(v_{gs}-v_{fbp})\left(\frac{2C_{ox}}{\varepsilon_{Si}t_{Si}}\right)=\frac{qN_a}{\varepsilon_{Si}} \quad (6)$$

$$\frac{d^2\psi_s(x)}{dx^2}-\theta^2\psi_s(x)=\zeta \quad (7)$$

Where $\theta^2=\frac{2C_{ox}}{\varepsilon_{Si}t_{Si}}$

$$\zeta=\frac{qN_a}{\varepsilon_{Si}}-\theta^2(v_{gs}-v_{fbp}) \quad (8)$$

$$\frac{d^2\psi_{s1}(x)}{dx^2}-\theta^2\psi_{s1}(x)=\zeta_1 \qquad 0 \le x \le l_1 \quad (9)$$

$$\frac{d^2\psi_{s2}(x)}{dx^2}-\theta^2\psi_{s2}(x)=\zeta_2 \qquad l_1 \le x \le l_1+l_2 \quad (10)$$

$$v_{fbp}=\phi_{mp}-\{\chi_s+E_g-q\phi_{fp}\} \quad (11)$$

$$\phi_{fp}=\frac{KT}{q}\ln\left(\frac{N_a}{n_i}\right) \quad (12)$$

The solution of second order differential equation (9), through the complementary and the particular integral functions is given as

$$\psi_{sp}(x)=\alpha_p e^{(\theta x)}+\beta_p e^{(-\theta x)}-\frac{\zeta_p}{\theta^2}$$

$$D_p=\frac{\zeta_p}{\theta^2}$$

$$\delta_p=\exp(\theta x)$$

$$\delta_P^{-1}=\exp(-\theta x) \quad (13)$$

Where $\alpha_P$ & $\beta_P$ are arbitrary constants, which are calculated with the help of continuity conditions for the surface potential distribution ($\psi$) and the field distribution (E) at the interfaces of different metal gates [3].

(1) The potential $\psi_{s1}$, at source can be written as

$$\psi_{s1}(x)|_{X=0}=V_{bi} \quad (14)$$

$$V_{bi}=\frac{KT}{q}\ln\left(\frac{N_aN_d}{n_i^2}\right) \quad (15)$$

(2) The potential $\psi_{s2}$, at drain can be written as

$$\psi_{s2}(x)|_{X=l}=V_{bi}+V_{ds} \quad (16)$$

(3) The surface potential $\phi$ is continuous functions at the interfaces of different metal gates [7] given by

$$\psi_{sp}(x)|_{x=l_p}=\psi_{s(p+1)}(x)|_{x=l_p} \quad (17)$$

(4) The electric fields E is continuous functions at the interfaces of dissimilar metal gates and can be written as

$$\left.\frac{d[\psi_{sp}(x)]}{dx}\right|_{x=l_p}=\left.\frac{d[\psi_{s(p+1)}(x)]}{dx}\right|_{x=l_p} \quad (18)$$

The electric field distribution can be achieved by differentiating surface potential w.r.t. x. The electric field profile finds out the velocity of electron transport through MOSFET channel.

$$E_{p(x)}=-\frac{d\psi_{sp}(x)}{dx}=\theta(\beta_p e^{(-\theta x)}-\alpha_p e^{(\theta x)}) \quad (19)$$

$$E(x)=\begin{cases}E_1(x); 0 \le x \le L_1\\ E_2(x); L_1 \le x \le L_1+L_2\end{cases} \quad (20)$$

## VI. SIMULATION RESULT AND DISCUSSION

The various output parameters extracted from simulation result for DMG SOI and SMG SOI MOSFET has been discussed below.

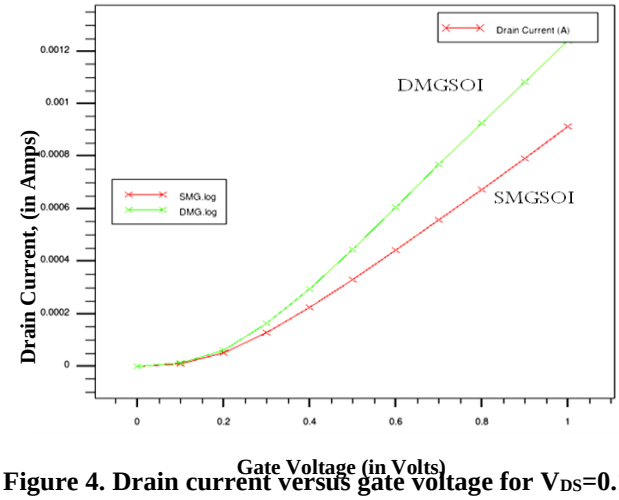


**Figure 4. Drain current versus gate voltage for $V_{DS}$=0.1**

### A. Transfer Characteristics

It is a curve plotted between drain current and gate to source voltage for a constant drain to source voltage.



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It is clearly evident from figure 3 that dual-material SOI has a higher value of drain current at the same value of threshold voltage.

### B. Output Characteristics

It is a curve plotted between drain current and gate to source voltage for a constant drain to source voltage.

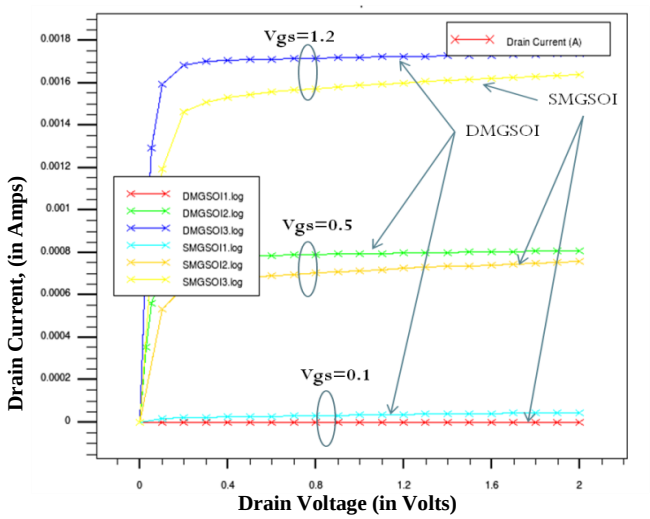


**Figure 4 Drain current versus drain voltage**

It is clearly evident from the graph that the dual material SOI MOSFET is free from Channel Length Modulation as compared to single material SOI MOSFET.

### C. Transconduction (Gm)

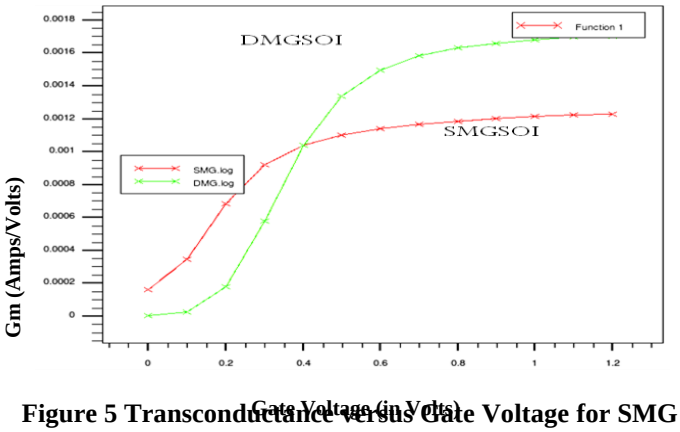


**Figure 5 Transconductance versus Gate Voltage for SMG and DMG SOI MOSFET**

It is a curve between transconductance (Gm) i.e. ratio of change in drain voltage to the change in gate voltage and gate bias (0V-to-1V) with the same value of $V_{DS}$ (const.)=1V.

It is evident from figure 5 there is an increment of Gm in DMGSOI as compared to that of SMGSOI which leads to higher intrinsic gain which gives better analog application [25].

### D. Drain Induced Barrier Lowering (DIBL)

Figure 6 shows the simulation result for the surface potential for various drain biases at a different point along the channel. The existence of a dual material gate ensures the drain voltage has a negligible effect on surface potential under material M1. Therefore, the variation in the drain potential does not impact the channel under material M1 [12].

It can be seen that the shift is negligible in the minimum potential point for the various value of drain voltage. This results in the reduction of DIBL for the DMG-SOI MOSFET [10].

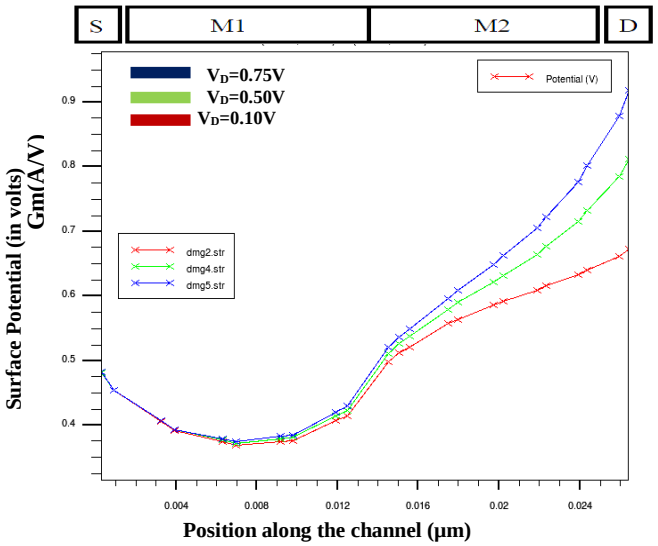


**Figure 6 Surface potential profiles for DMG-SOI MOSFET at various drain voltage along the channel**

The Following tables list the comparisons of performance and Short Channel Effects (SCE) parameters observed with the simulation of SMG and DMG SOI MOSFET.

**TABLE II. Output parameters of DMGSOI MOSFET and SMGSOI MOSFET at 32nm technology**

| Parameters | SMG | DMG |
|---|---|---|
| Threshold Voltage, $V_T$ (V) | 0.16 | 0.21 |
| Drain Current, $I_D$ (A) | $9.5x10^{-4}$ | $17x10^{-4}$ |
| Gm (A/V) | 0.0012 | 0.0017 |
| Gds (A/V) | 0.015 | 0.025 |

**TABLE III. SCEs comparison of DMGSOI MOSFET with SMGSOI MOSFET at 32nm technology**

| Parameters | SMG | DMG |
|---|---|---|
| OFF Current, $I_{OFF}$ (A) | $2.14x10^{-6}$ | $6.48x10^{-8}$ |
| Subthreshold Slope, $S_t$ (V/Decade) | 0.100 | 0.102 |
| DIBL (Unit Less) | 0.500 | 0.311 |

## VII. CONCLUSION

The reported work examined the efficiency of DMG to suppress the SCEs and the comparison of this structure is carried out with SMG SOI MOSFET at 32nm technology. It is concluded from the result the shift in minima of surface potential with varied drain bias is negligible in DMG SOI MOSFET which shows excellent immunity again SCEs like DIBL, CLM and Hot Carrier effect.

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The gate engineering mechanism can be utilized for optimum threshold voltage and channel length profile of the device i.e., without going through the fabrication processes and changing doping profiles. The unique features of the DMG are extracted i.e. reduced DIBL, improved Subthreshold Slope with simultaneous transconductance enhancement, and increase in drain current.

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**Prashant Kumar** has completed his B.E. in Electronics and Communication Engineering, M Tech. in VLSI Design and currently pursuing his Ph.D. in the semiconductor Device Modeling. He has more than 25 publications in various Journals and Conferences. He is an active member of Institutions of Engineers (IE) and AMIE. He is having a teaching experience of 11 years. His research interest includes semiconductor device modeling and circuits simulations.

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