

# Long Channel Keeper based Open Loop Difference Amplifier Domino for Noise Tolerant Low Power OR Gates

Manish Tiwari, Vijayshri Chaurasia



**Abstract:** This paper proposes an open loop difference amplifier with long channel keeper technique for domino logic circuits implemented as wide fan in OR gate. Currently OR gates suffer from high capacitive loading and delays due to such loading. The proposed design uses single stage of comparison and dual keeper arrangement to generate and hold the output logic state. This technique effectively reduces the high input loading from capacitance and manages the power consumption by switching based on the generated difference voltage. As compared to standard footerless domino SFLD, the proposed design OLDA has shown to reduce power consumption by 42% in 64 bit configuration. It has increased average noise immunity by 2.03 times, while maintaining same speed as compared to SFLD. All simulations are done in CMOS technology with 90nm PTM LP models.

**Keywords:** Dynamic logic circuits, OR gate domino, Long channel keeper, Low power digital VLSI design.

## I. INTRODUCTION

Dynamic logic circuits are an upcoming style of circuit design that involves clock driven transistor operation and the logic does not need a permanent latch to hold its output. Such factors allow it to operate at low power consumption as well as high speed [1-3]. With many applications demanding power optimizations as their key component like data storage systems that go in standby often and other applications that require high speed at inconsistent supply of power. Such applications are highly favored by novel technological innovations and dynamic logic circuit has proved to be one of the most versatile tools for logic gate designers [4, 5]. Such dynamic gates have applications in multiplexers, high speed data paths like registers, memories etc. Due to aggressive downscaling of technologies, the need for novel dynamic circuit designs have emerged in order to cope up with the leakage related power losses, over loading of inputs and other concerns on reliability [6, 7]. For this reason, novel domino circuit designs have been presented in the literature in order to cope up with the charge sharing and charge leakage related issues. While it does provide high speed and low power consumption, with further downscaling the domino circuit designs [8-12] need more stability and precise feedback mechanisms in order to reduce power losses further and allow

novel structures to be built with dynamic logic gates. Power consumption of a circuit is one of the key areas of further improvement in dynamic logic circuits. Since it depends on many factors, the power will be divided into 3 main components [13] in order to analyze the circuit precisely.

$$P_{total} = P_{switching} + P_{short-circuit} + P_{leakage} \quad (1)$$

$P_{switching}$  represents power consumption during the voltage switching. It occurs due to the natural charging and discharging cycle for parasitic capacitive load. This will be the major concern for deep node technologies.

$$P_{switching} = \alpha C_{eff} V_{DD} V_{swing} f \quad (2)$$

Here  $\alpha$  denotes the activity factor for switching.  $C_{eff}$  denotes the effective capacitance and  $f$  denotes the frequency of switching.  $V_{DD}$  stands for supply voltage and  $V_{swing}$  represents the voltage swing at output node.

The aggressive downscaling of technology has led to accompany drastic power consumption losses with better performance of circuits [14]. Since the subthreshold leakage current has an exponential relation with the new threshold voltage, that is lesser than it was for long channel transistors as shown in (4), this led to a subsequent rise in leakage power losses too. Static power losses are more subsequent on the rise as compared to dynamic power losses at deeper nodes, however we need to use optimum circuit design strategies to tackle both of them.

$$I_{sub\_th} = I_0 (1 - e^{-\frac{V_{DS}}{V_t}}) e^{\left(\frac{V_{GS} - V_{TH} + \eta V_{DS}}{\eta V_t}\right)} \quad (3)$$

The base current is shown below as:

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (n - 1) V_t^2 \quad (4)$$

In the above equations,  $V_t$  denotes the thermal voltage.  $V_{DS}$  stands for the drain to source voltage.  $V_{GS}$  denotes the gate to source voltage.  $V_{TH}$  denotes the threshold voltage further explained in (6).  $\eta$  stands for the coefficient of drain induced barrier lowering.  $W/L$  represents the aspect ratio for a transistor.  $n$  denotes the coefficient for subthreshold swing and  $\mu_0$  represents mobility at zero bias voltage.  $C_{ox}$  stands for gate oxide capacitance.

$$V_{TH} = V_{T0} + \gamma (\sqrt{\varphi_S + V_{sb}} - \sqrt{\varphi_S}) \quad (5)$$

As shown above,  $V_{T0}$  denotes the threshold voltage at no body bias.  $\gamma$  represents body bias factor.  $\varphi_S$  stands for potential that is needed to create the inversion layer.  $V_{sb}$  represents the transistor biasing from source to body.

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This is responsible for inducing body bias effect where  $V_{TH}$  is heightened due to extra added reverse bias across p type substrate and n type channel boundary for NMOS, thus resulting in an increased bulk depletion charge.

This paper proposes a feedback based circuit technique to lower power consumptions losses in wide fan in OR gates using an open loop comparator based amplifier. Most industry applications are based on logic gate operation and subsequently they require a wide fan in and wide fan out for realistic operations. Such applications are required to run at high speed, while reducing the power losses concerned and therefore dynamic logic gates prove to be favorable for designing such gates. This paper presents comparator based difference amplifier or CDA technique to show a low power high performing domino OR gate. Further sections are organized as follows. A brief literature survey with previous techniques has been explained in section 2 of this paper. The sections 3 and 4 discuss the proposed circuit operation and the results compared to other such designs in this area, respectively. Lastly section 5 gives the conclusion for the paper with future applications and assesses the final performance enhancement and limitations of the proposed circuit design. All simulations have been performed at 90nm CMOS technology with circuit temperature at 110°C in order to assess worst case scenario for the circuit. 1 voltage supply has been used for drain voltage. All comparisons for wide fan in gates have been performed for 8 bit, 16 bit, 32 bit and 64 bit inputs, with one output for the logic gate.

II. LITERATURE SURVEY

This section discusses conventional domino logic circuit designs. The early design of domino circuit involved a pull down network and a pull up transistor in a standard footed domino circuit or SFD [15]. This is shown in Fig. 1, where the circuit operates in 2 modes as precharge and evaluate. This provides a high speed and low power consumption for logic gate operation. It however lags the ease with which it can be cascaded, which is why most dominos are used in SFLD [16, 17] rather SFD as shown in Fig 2. This allows a higher speed of operation without affecting the current drive of the circuit thereby allowing us to cascade many dominos and maintaining high performance of logic gates.

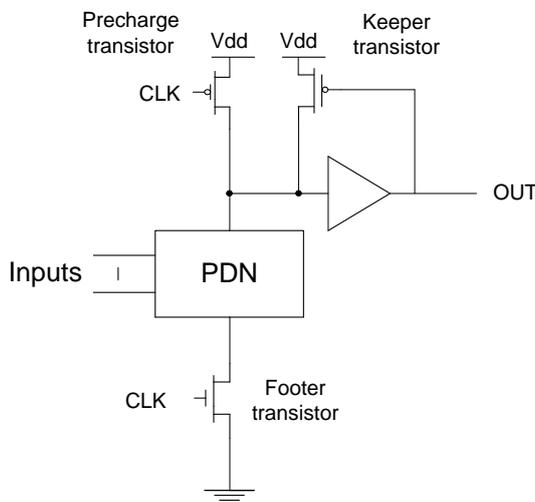


Fig. 1 Domino circuit OR gate in standard footed configuration or SFD

The operation of logic gate is performed by domino circuits in 2 phases as precharge and evaluate phase. The output state can only be high or low depending upon the input combinations of any or all input be high, or all inputs are low. Even if the inputs are at logic 0, they still are vulnerable to leakage currents [18]. For this reason, leakage sources in a circuit need to be addressed. Most important ones are the subthreshold leakage current ( $I_{sub\_th}$ ) and tunneling leakage current in the gate oxide ( $I_G$ ). Other sources of leakage have small affect on power losses and they can be considered negligible.

Such leakage issues in domino circuit leads to 4 prominent problems as charge leakage, charge sharing, capacitive coupling and clock feed through [19]. Charge leakage occurs in domino circuit due to the existence of direct path between voltage supply to ground and this path gets created during switching events. Appropriate selection of transistor size and transconductance is required to control this leakage. Even after that, circuit strategies are employed to keep such charge leakage and sharing related power losses to minimum. Charge sharing relates to the output stage not being able to provide the correct output, even when the input combination directs to that. This happens because due to the charge sharing between different stages of a domino circuit, optimum current is not generated in the output thereby leading to delay related mismatches between input combination and output. Such can be avoided by keeping an isolation stage in between input and output, such that output is no more driven by the input combinations. This is explained in detail in section 3 of this paper. Capacitive coupling is the extra input loading that is produced when all inputs are bunched together in one single and independent PDN. Clock feed through relates to the clock cycle related discrepancies and can be corrected if we operate the circuit in a given frequency range and use proper paths for the logic transitions. At high frequencies, this creates a major problem and this is why in order to maintain optimum operating conditions in a circuit, this parameter becomes of crucial importance. Furthermore, gates with high number of inputs require additional circuitry to manage the capacitive coupling and charge sharing between the stages. Therefore better designs are needed to implement domino circuits in cascade configuration and to operate them with high number of inputs.

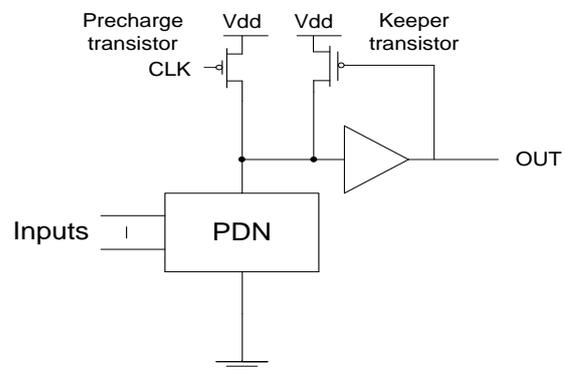


Fig. 2 Domino circuit OR gate in standard footer less configuration or SFLD



One important measure to tackle charge sharing and leakage was to use a keeper transistor in order to keep the output state at low level during evaluate phase. This is done in order to prevent the logic output from getting flipped to high state via charge leakage fault. Keeper is responsible for maintaining high voltage before the output node such that the output stays at 0 when it is needed to be. The keeper transistor requires certain specifications to be maintained in order to keep the circuit robust and circuit operation efficient. For most circuits, keeper transistor should be as small as possible because it is already a PMOS transistor which is larger than NMOS. Keeper sizing has to be managed in order to keep circuit at manageable delay, as keeper transistor adds slight delay to the circuits. And it affects noise tolerance of the circuit too. The overall performance of circuit is not degraded by keeper, but can be further improved if keeper circuits are modified accordingly. There exists a trade off conditions between the delay of circuit and the circuit tolerance to noise. Keeper sizing limitations can be better analyzed by observing the keeper ratio of a given domino circuit as shown in (7).

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{\text{Keeper-transistor}}}{\mu_n \left(\frac{W}{L}\right)_{\text{Evaluation-network}}} \quad (6)$$

In the above equation, W and L represents the width and length of the transistor respectively.  $\mu_p$  represents hole mobility and  $\mu_n$  represents electron mobility. With increase in keeper ratio aka by using PMOS transistor of long width, the noise tolerance of the circuit improves too but at the cost of excessive power consumption and extra delay introduced in the circuit. With the issue of contention in circuits due to parallel leakage paths in inputs, it further increases the need for optimum keeper transistor sizing. In the latest applications of logic gates, it is needed to keep a wide fan in gates and for this reason, this paper focuses on a comparative study of wide fan in gates at 8 bit, 16 bit, 32 bit and 64 bit.

The wide variety of circuit techniques and design strategies can be categorized in 2 parts. One are those that focus on altering and improving the keeper circuit in order to control the contention current and improve performance [20-23]. Others aim at modifying the PDN via sizing the transistors appropriately in order to reduce current leakage losses in precharge and evaluate phase [24-32]. This section discusses latest circuit techniques for designing high performance domino logic gates.

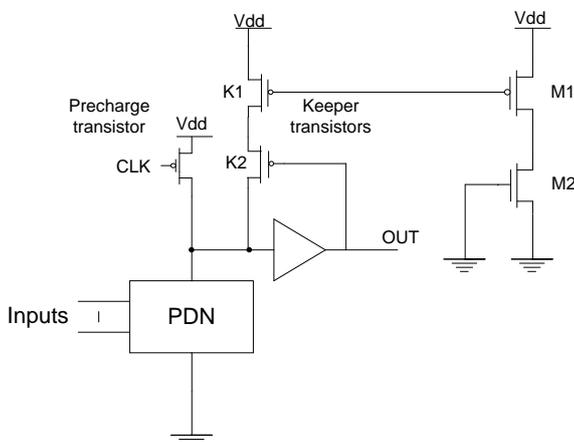


Fig. 3 Domino circuit OR gate with Leakage Current Replica or LCR design

One of the keeper modification strategies is the Leakage current replica or LCR technique [26]. It is shown in Fig. 3, where the leakage of pull down network is being replicated by the additional LCR network called as LCR keeper and such kind of mirroring helps to reduce leakage drastically. Other important parameters as effects of PVT variation on delay of the circuit are also reduced to make it reproducible and feasible design for industry. It can be seen that via Monte Carlo analysis, process, voltage and temperature ranges are taken at the extreme set points and the delay variability has been reduced thereby making a more stable circuit. LCR technique is limited by the precision needed in it for matching the transistors in keeper network. It also incurs high power losses due to the input driven output and keeper respectively. Such an issue becomes more problematic when high number of inputs are used for the logic gate operation like it is done in many new generation processors.

The reduction of leakage via leakage mirroring can be done in another way as shown in Fig. 4(a) and 4(b). This is controlled keeper current by comparison domino or CKCCD technique [27]. It does not rely on precise matching of transistors, instead it has a dedicated reference circuit to determine and mirror the leakage current. While providing better noise tolerance for the circuit, it also reduces total power losses in the circuit. It has strong control over the keeper circuit but input current drives the inverter thereby slowing down the circuit and PDN incurs high input capacitive loading and needs separate measures to reduce power losses further in the circuit.

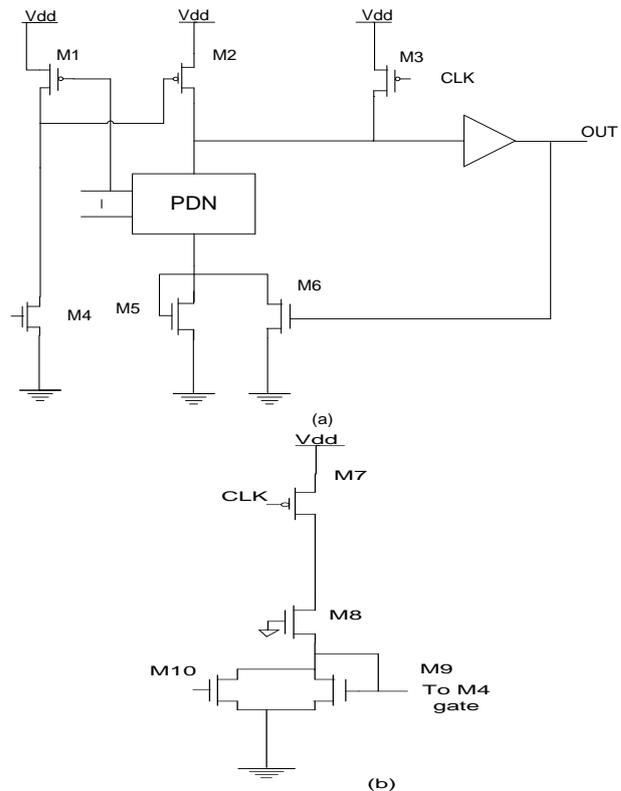


Fig. 4 (a) Domino circuit OR gate with Controlled keeper current comparison domino or CKCCD design and (b) Reference block for CKCCD

The leakage current mirroring strategy always involves a reference circuit to compare the current thereby leading to reduced contention in the circuit. As shown in [28], here the current from pull up network and reference current are being compared and mirrored. This results in lower power consumption and higher noise tolerance of the logic gate along with stronger control over the switching operation due to footer transistor thereby increasing the robustness of the circuit too.

The input capacitive loading has been a major problem for domino gates, especially for wide fan in logic gates. Using diode partitioning technique [29] the input paths can be isolated with each other thereby avoiding the capacitance getting added in series. This is done via using a general purpose diode with every group of input fan in. This paper has used 4 inputs with one diode combination. Such technique has best applications in high input fan in circuits like tag comparators, processor paths etc. All applications with high fan in even up to 64 to 128 bits will benefit from this technique. It is limited in terms of its ability to be used with other domino techniques since it requires a separate keeper arrangement for its successful operation. Even with a weak keeper, it still is heavy enough to incur power losses [30]. Therefore this technique provides a low power and low delay solution to domino gates, it is limited in terms of integration with other techniques and power losses will be high for deeper node technologies.

A brief analysis of these techniques shows that keeper control strategies are optimum to reduce contention current and partitioning strategy has shown beneficial to reduce capacitive loading of the inputs. However it is still needed to modify the circuit such that it does not affect the cascaded operation of the gate with other circuit stages. Even further the diode partitioning incurs a high output voltage swing due to multiple keepers for partitions. This creates a tradeoff situation between the number of inputs we can increase with the power consumption losses it incurs. Such concerns are cornered by novel techniques like CCD and CKCCD which use isolation strategy to prevent output voltage swing getting affected adversely. But due to the precise matching requirement, this technique falls at risk with big systems that use such gates as a small part of it. PVT variations affects such matching of transistors along with the technology nodes being used, therefore better techniques are needed to provide the benefits in all such areas especially when we use high input gates in battery operated circuits that puts the logic value at risk of getting corrupted. Novel domino circuit strategies are needed to further enhance the operation of the circuit while maintaining high performance aka high noise tolerance and low power operation at all process corners.

III. PROPOSED CIRCUIT

The proposed design is open loop difference amplifier based long channel keeper domino or OLDA domino. It aims at reducing the output voltage swing thereby reducing the power consumption of the circuit. It does so by using the interim property of 2 voltage nodal states in OR gate where either one or more inputs are high, or all inputs are off. Since the difference between these voltage states is high enough to qualify for operating a difference amplifier, the design uses an open loop comparator to compare the voltage difference and generate the output signal. The proposed circuit can be

divided into 2 parts: the input logic block and the output logic block.

The input logic block uses input transistors in PDN to implement the OR gate function, as shown in Fig. 7. Input block will contain 8, 16, 32 and 64 transistors depending upon the fan in of OR gate. The output logic block, as shown in Fig. 8, uses the advanced comparator in a difference amplifier configuration to produce an output voltage that depends on the voltage difference between nodes N1 and N2.

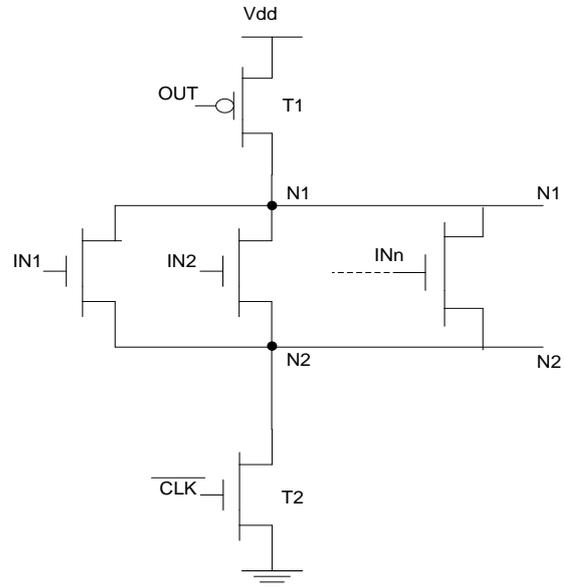


Fig. 5 Domino circuit OR gate basic input logic block

The comparator block comprises of a differential pair of transistors as M3 and M4. Conventionally input voltage is applied to the gate of M3 and reference voltage is applied to gate of M4. The range of input voltages has been set to cover the complete voltage swing in the circuit. These are NMOS transistors driven by tail current transistor M5. Transistors M1 and M2 act as a diode load for M3 and M4, because of the shorting of their drain and gate terminals together.

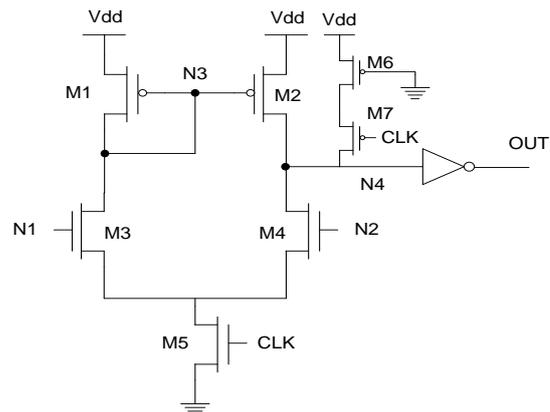


Fig. 6 Domino circuit’s logic output block of OLDA domino

The domino gates designed in [24-32] have one common feature of clock driven pull up transistors. This provides robustness to the circuit by allowing non overlapped signal flow between evaluate and precharge phase.



Such feature works well on moderate frequency operations below 100-300 MHz, but in order to operate higher frequency operations on domino circuits, typically above 500MHz to 1.5 GHz, the pull up transistor has to be driven by output. This way we can achieve a domino circuit with higher speed and lower power consumption as compared to conventional domino circuits. The drawback of using this technique is that in case of cascaded stages of domino, the output driven transistor reduces the current drive and places the next stage at risk of flipping its state. To eliminate this issue, output is not driven directly by the input stages, rather it has isolation stage of a comparator. This does not benefit much in reducing the power consumption, but it helps in providing high current throughout the output and increases the speed of operation of the circuit. This way the output driven transistor T1 can turn on and off swiftly. It is also responsible for holding N1 high which is input to M3 aka the input voltage for comparator. Such an arrangement prevents any leakage from disrupting the natural switching of cycles. T2 provides the discharge path in precharge phase to N2. It allows for complete reset of logic outputs for next evaluate phase. Another advantage of this arrangement is it reduces the leakage via high capacitance of wide fan in gates. As compared to other domino circuits that directly discharges its output via all transistors in PDN; the advanced comparator circuit does so indirectly via M4. Therefore only one transistor receives the full current drive and circuit operation is fast with less leakage.

Transistor sizing has to be precise in order to achieve high speed operation of the circuit. While M5 is clock controlled, M4 is controlled by the input voltage at node N2. This allows circuit to establish strong control over the circuit operation and these are sized in a way that threshold voltage of gate is higher than threshold voltage for other transistors in PDN. This increases noise tolerance of the circuit and reduces leakage even further. However it leads to small delay in the circuit. This is overcome by keeping a clock controlled keeper instead of convention output controlled keepers. As explained in section 2, keeper sizing is important to provide low leakage and high noise tolerance, along with accuracy and overall performance of the circuit. For technology nodes above 180nm, circuits can work efficiently with a weak PMOS keeper transistor. It is kept to be minimum width, as shown in (8), in order to avoid contention current related power losses.

$$I_{Dp} = K_p' \left(\frac{W}{L}\right) \int_{V=0}^{V=V_{SDp}} [V_{SGp} - |V_{Tp}| - V(y)] dV \quad (8)$$

Here  $I_{Dp}$  is drain current for p channel MOSFET.  $K_p'$  refers to process transconductance and is set by the processing specifications.  $V_{SDp}$  is source to drain voltage for p type MOSFET.  $V_{SGp}$  is source gate voltage.  $|V_{Tp}|$  is threshold voltage and  $V(y)$  is voltage on differential length  $dy$  over the length of the channel.  $\frac{W}{L}$  refers to the aspect ratio of the transistor.

A weak PMOS keeper worked efficiently for higher technology nodes, but as we go into deeper technology nodes aka smaller transistors, a minimum width PMOS keeper size is still relatively high enough to disrupt the circuit operation. This situation is rectified by increasing the length of effective keeper by using 2 keepers M6 and M7 in series such that M6 acts as the long channel device that is supposed to be turned

on all the time while M7 being the minimum size keeper that is run by the inverter output itself. Since we have used the output to drive pull up transistor T1 and also in order to effectively turn off the circuit for high frequency operation, M7 is controlled by the clock signal in the proposed circuit. The entire operation of dynamic logic circuits works in 2 phases: precharge and evaluate, as explained below.

#### A. Precharge Phase

The circuit precharges the pre-inverter circuit capacitance to high and output to low state in this phase. Clock is low (CLK=0) along with the input signals, while node N4 is at high voltage. This is done via M7 transistor turned on by clock signal, thereby increasing the voltage on this node and charging the pre output capacitance to high, thereby reducing the voltage on output to low state. T1 is turned on in this stage, rendering voltage at node N1 high. N2 is low in this phase.

#### B. Evaluate Phase

In this phase, clock is high (CLK=1). Only 2 output logic states can occur depending upon whether all inputs are low or if at least one input is high. M6 will be turned off, M5 is turned on, T1 will be on at the start of this phase and T2 will be off in all cases. N4 will start with high state to low or high depending upon the input combination. These 2 scenarios are detailed below.

If all inputs are low, N1 remains in high voltage state while N2 remains in a low voltage state. Small leakage currents affect the N2 voltage and prevent it from reaching 0. However such leakage is only limited to tiny values which will not affect the circuit states. Furthermore due to the transistor bias  $V_{SBn}$  the body bias effect will increase  $V_{Tn}$  in this state. It will further lower the leakage in this part of the circuit. The comparator will get its input N1 at high voltage and input N2 at low voltage. Since M5 is on, comparator gets activated with M4 and M6 off. This allows N4 node to stay at higher level and gradually reduce to low level while the circuit gets its logic operation done. Here output driven transistor only acts as activator of the circuit due to the isolation of PDN from the output stage. And secondly voltage supply is not used to keep this node at high level. This reduced dynamic power consumption further. And the output remains at low voltage level. If at least one of the inputs is high, aka at least any one of the transistors IN1 to INn turned on, N2 will reach a high voltage thereby turning on M4. This results in node N4 discharge via M5. Sizing of M6 and M7 is done in order to minimize the leakage current as well as dynamic power losses in this part of the circuit. Output goes to high voltage and we get high output for the given input combination to OR gate.

### IV. EVALUATION PARAMETERS

Area, speed and power metrics have been explained previously. In the sections below, noise tolerance measurement will be explained along with a novel parameter to evaluate overall performance of the circuit.

### A. Noise Tolerance

There are multiple sources of noise in every circuit, most of which are not a function of technology or process of the circuit; rather they are related to the interfacing and topology of the circuit. Noise performance is even more required for circuits that involve interfaced logic circuits with different supply rails. For advanced dynamic circuits, noise tends to be a very important parameter for the overall performance of the circuit. The aim is to avoid any deviation from the expected values of voltages and currents at different nodes of the circuit. Due to many sources of noise in a circuit, some amount of noise is unavoidable and the ultimate issue is that overall circuit operation should stay unhampered. This is the simplest approach to find noise related stability of a circuit called as the small signal unity gain failure criteria [31]. For a circuit stabilized at preset operating point, input noise is introduced and the respective change in output noise is measured. Noise immunity is said to be low and the circuit deemed unstable if it satisfies the condition given in (9).

$$\left| \frac{dV_{out}}{dV_{in}} \right| > 1 \quad (9)$$

This approach is a convenient way for a designer working on a circuit level. However this is not a necessary criterion for the circuit to be stable and a better way is introduced here to assess the noise tolerance of a circuit. While the standard industry approach is to use customer owned tooling or COT approach [32], but for assessing circuits on a single stage of operation, a simpler approach has been presented here to calculate the Average Noise Immunity (ANI) of the circuit.

Conventionally a pulse signal of fixed duty cycle is used to imitate noise at the input end and the output is checked for changes. In order to get the logic correct aka noise margin has to be checked at the operating point in the worst case scenario. The input signal might differ in its frequency and amplitude from the output signal which may affect the accuracy of observed noise tolerance. Therefore in order to maintain the simplicity of this test along with high accuracy, this paper observes noise over a duty cycle of variable duration that should be equal to the duration of the output. This way we will generate an average noise immunity reading called as ANI. A value less than 1 implies that the circuit is stable and noise tolerant. And based on this stability check, we can further develop the sophistication of the circuit.

### B. Gross Performance of Circuit

Individual comparisons of circuits have been given in further sections. But in order to analyze all major performance parameters in one single parameter, we have formulated a new performance parameter called gross performance of circuit design or GPC. It describes 4 major parameters area, speed, power and also noise via one single metric. This enables multiple parameter comparisons instead of a singular comparison between different techniques that need not be base lined at one parameter. GPC will be taken as a figure of merit to justify the efficacy of this circuit in comparison to others.

In order to derive GPC, this paper first considers the 2 most important parameters for high speed domino circuit applications as delay and power. These 2 are strongly interrelated in an inverse relationship, which is why they are

specified together as power-delay product or PDP [33]. For a given technology node and circuit topology, it stays more or less the same as given in (10). The average power  $P_{avg}$  is multiplied with the worst case propagation delay  $t_{pd}$  to give the PDP. This is due to the fact that dynamic CMOS works on the charging and discharging of capacitors aka the flow of charges determines the speed of the circuit. But this flow of charges always incurs power losses as it is the very flow of stored energy. Therefore for every switching event, there is a power loss that is observed by PDP. This leads to an inverse relationship where the faster a circuit gets to be, the more power consumption occurs. This is why PDP has been a very useful performance metric for CMOS design.

$$PDP = P_{avg} t_{pd} \quad (10)$$

PDP is useful in many applications but not all. It assumed dynamic power consumption to be the highest contributor of power loss. While it assessed the energy losses in a switching event, it also assumed highest gate frequency; therefore the optimum voltage would come out to be the lowest possible voltage as per the given conditions. This is why this paper uses Energy delay product or EDP as the basis of GPC because it lets designers acquire an optimum possible supply voltage [34] and is better at assessing the overall performance of the circuit. EDP is multiplied by area A of the design to cope for the combined negative performance parameters aka the lesser it is the better it is. And ANI forms the numerator since it is a positive performance parameter. GPC is given in (11) below.

$$GPC = \frac{ANI_n}{P_n \times t_n^2 \times A_n} \quad (11)$$

In order to assess each circuit on common grounds, the circuits are simulated at same temperature, voltage and technology. This allows for a fair comparison between them. Normalized values have been used to distinctly assess the design importance as compared to one base circuit Standard foot less domino [24].

## V. DESIGN EVALUATION AND DISCUSSION

The simulations have been performed on 90nm CMOS technology using 1 Volt supply at a temperature of 110 °C to properly assess the operation of circuit on relatively high temperatures. The circuit is compared with previous techniques under same simulation environment and other variables in order to uniquely focus on one performance parameter over other. Area, speed and power have been the traditional performance metrics for major critical application domains [30]. However with deeper technology nodes new performance parameters need to be assessed with them. These are noise tolerance, reliability, stability to corner variations and robustness of the circuit.

Wide fan in gates are assessed for 8 bit, 16 bit, 32 bit and 64 bit inputs. For microprocessor and read paths, even higher bit lines are needed which will be discussed in future work of this area. While the circuit can work for comparatively higher frequencies, but in order to compare circuits on same environment, circuit frequency is kept at 1 GHz and at the same fan out for all techniques.

The calculation of performance parameters needs to be on the practical working conditions of the circuit. For this purpose, input is taken from a cascaded stage such that the rise time and fall time expressions shape up the practical level values instead of ideal values. Table 1 shows the comparison of ANI and ANI normalized to SFLD, for different designs as standard footless domino or SFLD, leakage current replica or LCR, controlled keeper current comparison domino or CKCCD, and current comparison domino or CCD, with the proposed design open loop difference amplifier based long channel keeper technique or OLDA domino. All designs are kept at same delay for better qualitative comparison. At initial combination of 8 inputs, the proposed design has acquired 53% increase in ANI as compared to the base design SFLD, while providing a nominal increase as compared to next best design CCD. This result is enhanced for 64 bit input combination where OLDA acquires 103% increase in ANI and it is still 9% higher than the next best design of CCD. ANI shows the stability of the circuit under various noise sources and the reliability of the output. Since OLDA uses difference of input and amplification, the output is not adversely affected from the noise, thereby giving a proportional improvement in all input combinations. It is also due to the cutting off of various sources of noise under standby conditions. Higher noise immunity is much needed property for applications that are susceptible to coupling and interconnect problems and OLDA offers a robust design with high noise tolerance at a given delay and performance.

**Table 1:** Average Noise Immunity, absolute and normalized, for different techniques and different fan-ins are observed in this section. All techniques are compared for the same delay.

Fan-in		SFLD	LCR	DPD	CKCCD	CCD	OLDA Proposed
8	ANI	0.45	0.37	0.48	0.66	0.68	<b>0.69</b>
	ANI <sub>n</sub>	1	0.82	1.07	1.47	1.51	<b>1.53</b>
16	ANI	0.39	0.32	0.46	0.63	0.66	<b>0.64</b>
	ANI <sub>n</sub>	1	0.82	1.18	1.62	1.69	<b>1.64</b>
32	ANI	0.34	0.29	0.45	0.57	0.61	<b>0.62</b>
	ANI <sub>n</sub>	1	0.85	1.32	1.68	1.79	<b>1.82</b>
64	ANI	0.29	0.25	0.44	0.54	0.54	<b>0.59</b>
	ANI <sub>n</sub>	1	0.86	1.52	1.86	1.86	<b>2.03</b>

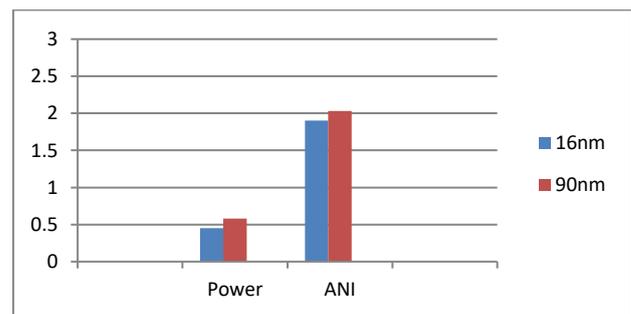
Power consumption has been compared in table 2 for these techniques. In order to compare with the base design, all techniques are normalized to the base circuit design SFLD. And since all circuits are built in a way to have the same delay, such results are a very good indicator of the efficiency of proposed design. While maintaining the same speed of operation, it was able to reduce power consumption. However since the current from the difference amplifier is driving the output transistor, it falls at the risk of low current throughput and therefore the circuit might incur extra delay due to that. For this reason, when the power was compared at same delays, the comparative analysis showed that the proposed design has acquired a marginal 6% reduction in power consumption at the expense of 5 extra transistors at 8 input combination. However as the inputs are increased, the capacitive loading dependent leakage outweighs the dc

grounding of node N4 and therefore a reduction in net power consumption is observed at higher inputs. At 64 input combination 42% reduction in power is observed as compared to SFLD and 6% decrease as compared to the next best design of CCD.

**Table 2:** Power consumption, absolute and normalized, for different techniques is given below. All techniques are compared at the same delay at each input combination.

Fan-in		SFLD	LCR	DPD	CKCCD	CCD	OLDA proposed
8	$P_t$	25.3	24.5	29	<b>20</b>	23	24
	$P_{tn}$	1	0.97	1.15	<b>0.79</b>	0.91	0.94
16	$P_t$	29.4	27.6	34.2	23.6	<b>22.3</b>	23.8
	$P_{tn}$	1	0.94	1.16	0.8	<b>0.76</b>	0.78
32	$P_t$	34.75	34	39.3	30	<b>24.9</b>	25.1
	$P_{tn}$	1	0.98	1.13	0.86	<b>0.71</b>	0.72
64	$P_t$	44	40	48	38	27.5	<b>25.9</b>
	$P_{tn}$	1	0.91	1.09	0.86	0.63	<b>0.58</b>

Every technique has to be compared on similar ground for a discreet qualitative analysis. This is why we need to assess the performance of the circuit technique at different technology nodes. As shown in Fig 7, the proposed design OLDA is rebuilt on 16nm technology node by using low power PTM LP model. And this is compared to the same design at 90nm technology node. Since the efficacy of design was seen best with 64 inputs, this is used to compare power and ANI, while keeping the delay normalized to SFLD. On that note it is clear that the proposed design gives stronger noise immunity with respect to the base design at the expense of small power loss. When we are dealing with lesser technology nodes, the dynamic power losses are reduced due to smaller voltage swings, but it results in a much stringent criterion for noise margin. This is why noise immunity is a much more crucial factor at deeper technology nodes.



**Fig 7:** Worst case delay, power and ANI are compared for OLDA domino at 2 different technology nodes, 16nm and 90nm. All are normalized to SFLD performance parameters.

The calculations of power, speed, and noise immunity have been explained in previous sections. The area estimation is done by using standard formula for transistor sizes. Since 32 input combination is mostly studied in such applications and many more techniques have been formulated on this input combination, the analysis is done for 32 inputs OR gate in table 3.

Using high numbers of gates was an important scenario to check for high speed applications such as read paths, register memories etc. This is to provide a consolidated data for all these circuit techniques and also to provide a tradeoff for OLDA technique with respect to other techniques. CKCCD technique holds lowest power consumption for 8 bit inputs, but when we increase the inputs and thereby the switching in the circuit, OLDA achieves the lowest power consumption for higher number of inputs. Area of the chip is increased in many novel designs that have higher noise tolerance than SFLD, but the it provides very high power consumption on higher number of inputs as shown in the table. Also in case of interfaced designs where not just one logic family, but many logic families work together in a single circuit, CKCCD will be at a disadvantage. This concern is overcome in OLDA while still assessing and optimizing the area requirements. Many industrial applications focus on low power and high speed as their major determining factors., along with area optimizations and these will also benefit from OLDA because of lower power consumption that helps with the battery life as well as high speed and high noise tolerance.

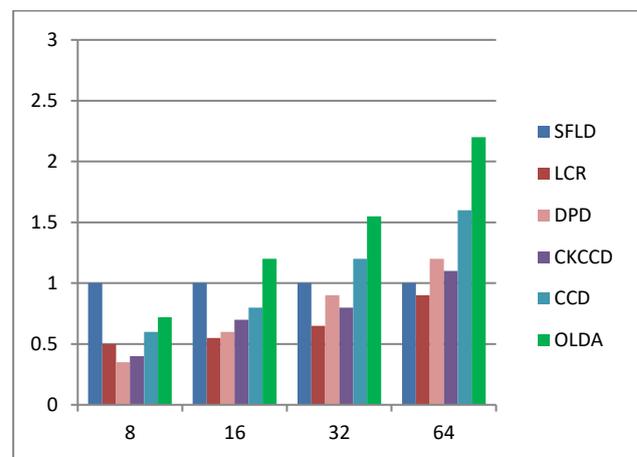
Many circuit techniques have used different features to reduce the input capacitance of high fan in circuits. DPD uses a diode partitioning technique wherein the capacitance no more works in series rather are split in between. This does introduce additional circuitry, but it works well for very high fan in gates. However due to the cascading issue, other designs are preferred as CCD and CKCCD. CCD design provides low power consumption since it avoids the direct leakage paths and precisely controls the output voltage swing. It utilizes PMOS transistors for its inputs to maintain node current operation of the circuit. However including PMOS switches the circuit back to large area and high capacitance. This circuit therefore incurs low speed concerns. CKCCD uses NMOS for the inputs, however unlike other circuits, the comparison dependent circuits involve high precision matching of circuits and small changes in node voltage have high impact on its operation. In case of substantial delay in a signal or voluntary cut off, its operation gets affected, thereby leading to less reliability. This is why for high speed applications that are also double sided operational, it is difficult to maintain overall topology of the system coherent enough to be completely compatible with such comparison dependent circuits. On the other hand, SFLD uses a basic circuit operation to achieve the same such that area is most optimized but has average performance due to the high input capacitance it has. OLDA isolates the output logic voltage from the input fan in capacitance, thereby effectively reducing the capacitance and allowing faster operation of the circuit. This is why, the proposed circuit offers lower area than CCD, with similar power consumption and higher noise immunity. And this statistic also improves at 64 input combination where the power is lowered further than CCD by 6% and by 42% as compared to SFLD.

**Table 3:** Comparison of performance parameters for different designs is shown below. All circuits operate with same delay of 90ps. Gate operation is 32 bit input OR gate.

	SFLD	LCR	DPD	CKCCD	CCD	OLDA Proposed
Total transistor	36	39	84	44	48	43

Area	125	133	291	151	238.5	149
Area (Normalized to SFLD)	1	1.06	2.32	1.2	1.91	1.19
Power	34.75	34	39.3	30	24.9	25.1
Power (Normalized to SFLD)	1	0.98	1.13	0.86	0.71	0.72
ANI	0.34	0.29	0.45	0.57	0.61	0.62
ANI (Normalized to SFLD)	1	0.85	1.32	1.68	1.79	1.82
GPC	1	0.67	0.93	0.83	1.2	1.55

The GPC of this design has been compared with other designs in Fig. 8 below. As mentioned earlier, the application of this design mainly concerns high bit lines like read paths, micro processor ALU and advanced MUX. For this reason, the circuit design has focused on superior performance at higher number of inputs. The more we reach to higher inputs of OR gate, the better performance gets. And GPC of design clearly surpasses other designs at higher number of inputs due to considerable reduction in input capacitive loading and the output driven PMOS, thereby leading to a reduced voltage swing at the output.



**Fig. 8** GPC comparison for different techniques at 4 different fan-ins as 8 bit, 16 bit, 32 bit and 64 bit.

At different stages of chip development, different criteria come into play like placement of interconnect lines, proper usage of voltage supply rails, back up scenario for failure modes etc. These are affected by the sizing optimizations of transistors. While all circuit topologies are affected by the choice of these parameters, some topologies depend on it much strongly than the others. For this reason, high precision techniques like current mirror circuits, leakage follower circuits and delay based circuits; these depend heavily on the precise choice of transistor parameters. But this leads to a lower reliability of these techniques as compared to OLDA.



In order to assess the reliability and stability of a circuit, these designs are simulated under variable process, temperature and voltage conditions.

While process and temperature are dependent on the fabrication technologies, voltage supply depends on the way the circuit is operated and set up for the final build of chip. In Fig. 9 and Fig. 10, the process corners have been evaluated for all 5 front end corners as TT, FF, FS, SF and SS. 2 temperatures have been used at considerable extremes as 25 °C and 110°C. Voltage supply is also varied at 0.9, 1 and 1.1 Volts. The delay has been normalized to SFLD in this analysis. As mentioned in section 1, this circuit is able to work efficiently under low voltage supply of 0.9 volts too due to optimum sizing and use of signal amplifications stages. This is represented in the graphs shown below. While there can be many corners for a design process, these are most important for circuit level evaluation and hence are focused at OLDA and SFLD for design stability and performance under variable process parameters. Simulation results show that OLDA design has work at optimal performance in design corners and works especially well on corners that test on slow PMOS operation. This is due to the use of least possible PMOS transistors in the design and entire PDN is operated via NMOS transistors only.

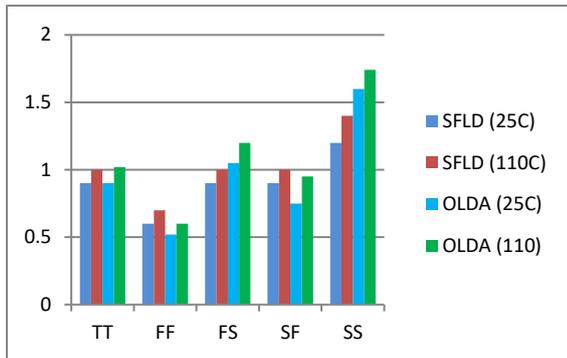


Fig. 9. Corner analysis for proposed circuit OLDA with SFLD at varying temperature and front end process corners on normalized delay of the circuit.

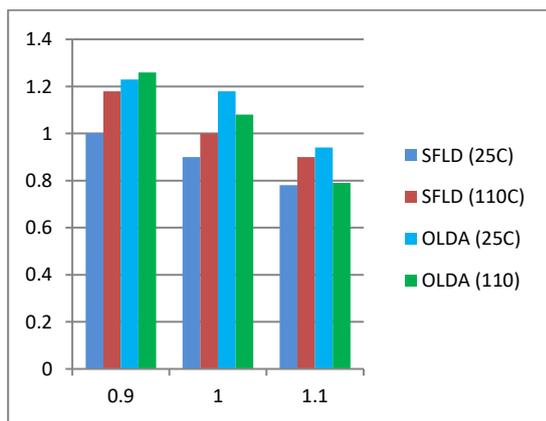


Fig. 10 Corner analysis for proposed circuit OLDA with SFLD at varying temperature and voltage corners on normalized delay of the circuit.

## VI. CONCLUSION

One of the most recurring issues with domino circuit designs has been the loading of input stage with high capacitance and this issue has been resolved by the proposed design of open loop difference amplifier based long channel

keeper domino. Secondly the proposed design has successfully reduced the delay in the circuit by adjusting the output voltage dependence on the comparison of 2 node voltages instead of its reliance on just one. Furthermore the isolation of stages and mixing of clocked and non-clocked feedback led to a reduced voltage swing in the output, that in turn reduces total power consumption and increases noise tolerance. All designs were simulated on a common technology node of 90nm PTM LP model.

The proposed domino circuit can be used for gate operations in many low power and high speed applications such as on chip decoders which require low power battery to be operated, flash memories that need high speed as a major specification and micro processor function paths that can go even higher than 64 bits. Since the proposed design can work with cascaded gates and minimizes the static leakage due to direct path from voltage supply to ground, it can be used in the design of wide fan in gates and would result in a high performance gate operation.

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