Accelerator Design for Ethernet and HDMI IP Systems for IoT using Xilinx Vivado 18.X

Ipseeta Nanda, Nibedita Adhikari

Abstract: ***Xilinx Vivado software is used for designing synthesis and implementation of accelerator. The objective of this paper is to understand the concept of intellectual property (IP), IP reuse, custom IP and IP subsystem and to design the subsystem using Xilinx Vivado is used. This paper attempts to design accelerator to make communication possible between High Definition Multimedia Interface (HDMI) and Ethernet for Internet of Things (IoT) using Xilinx Vivado 18.X [4]. The term is increasingly being also defined as objects that "talk" to each other rather in the manner of Internet of Learning Things (IoLT) based IoT to define objects with that of "realistically talk" to each other, given the rising system external & internal environmental complexity and uncertainty factors facing the objects.***

Keywords: IP, IoT, HDMI, IoLT

I. INTRODUCTION

Field Programmable Gates Array (FPGA) consists of multiple logic gates which can be configured. FPGA is not a vast collection of individual Boolean gates. One can buy ICs that consist of AND gates, OR gates, and so forth but it wouldn't want to build a shift register out of individual gates. Instead, you would buy a shift register IC. It's an array of carefully designed digital sub circuits are called configurable logic blocks (CLBs).CLBs include look-up tables, storage elements (flip-flops or registers), and multiplexers. It allows CLB to carry out different functions like data-storage, arithmetic operations and Boolean. The CLBs work together with one another and with outside circuits. FPGA uses a matrix to communicate with input/output (I/O) blocks for different functions**.** Look Up Tables (LUT) consists of 1-bit memory cells it may either hold '0' or '1' and it is set of multiplexers. CLBs include look-up tables, storage elements i.e flip-flops or registers, and multiplexers. LUTs comprise of 1-bit memory cells programmable to hold either '0' or '1' and a set of multiplexers. One value among these SRAM bits will be available at the LUT's output depending on the value(s) fed to the control line(s) of the multiplexer(s). FPGA is not a vast collection of individual Boolean gates [1][2][3]. The structure of FPGA is shown in Figure3.

II. INTELLECTUAL PROPERTY

It is a piece of logic or integrated circuit layout design which can be reused for creation of other subsystems by the creator or the third party if licensed. IP cores are the blocks which are within application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA) logic designs.

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The need of creation of IP or IP reuse is with the growing complexity and decreasing size of System on Chips, various design methodologies have been developed to facilitate designing issues [17]. HDL descriptions and EDA software (design, simulation, synthesis, verification and so on) design techniques system have played an important role in VLSI. In spite of all these attractive features of this methodology there are many reasons why IP reuse technique is in demand. The Measurement and others are on purpose, using specifications that wait as one part of the entire actions, and not as an independent file [16].

Few such reasons are [11]:

i) To keep away from re-inventing the turn for every innovative creation
ii) To step up the development of innovative products
iii) The option to reduce the failure based on design and verification of a block for the first time
iv) To decrease Time-to-Market
v) Lack of skilled engineers in this field
vi) The main focus can be put on adding new features or functionality to the product instead of wasting time in creation of same design from scratch

Still reusing the IP is not a simple task. A lot of care must be taken before reusing IP blocks such as:

i) Compatibility over various
   a. OS platforms
   b. HDL languages
   c. FPGA devices
ii) Consistency(across IP cores)
   a. File structure
   b. Naming convention
   c. User Experience
iii) Configurability
   a) Parameterized IP
   b) Appropriate placements/timing constraints

III. STRUCTURE OF STANDARDIZED DIRECTORY

A structure of standardized directory is significant for IP reusability [14]. It is well-organized and is simple to utilize database structure which provides compatibility and consistency to designs. IP blocks involve coding, specification and verification stage. Many support file formats which are required for different function.

The capacity to log and maintain follow of design changes is central for overall excellence of the design.
Figure1 shows structure of directory to provide support to the IP development stages.

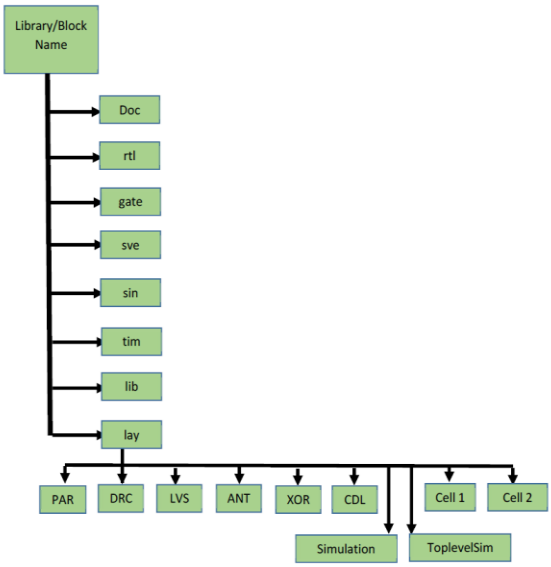

Figure1: Structure of directory to support the IP development stages

In figure1 *doc:* design document area, *rtl*: Verilog/vhdl code and RCS database, *gate*: gate level netlist, *sve:* testbench environment, *syn:* synlib files for ingternal memories, Synthesis file area, *tim:* internal memory STAMP model source files, timing analysis area, *Lib:* contains the .lef, .gds files, *Lay:* layout information for placement.

IV. TYPES OF IP CORES

The IP cores are of three types [11]. Hard IP, Soft IP and Firm IP are the type of IP cores. It is described as follows:
Hard IP cores which consists of hard layouts. It uses physical design libraries and delivered in masked-level designed blocks (GDSII format). It is technology reliant and provides lowest amount portability and flexibility. *Soft IP* cores delivered as RTL VHDL/Verilog code to provide functional of IPs descriptions. These cores provide maximum flexibility and configurability. It matches with the requirements of a exact design application. *Firm IP* cores provide balance between hard IPs high performance and optimization and flexibility of soft IPs.

V. VIVADO HIGH LEVEL SYSNTHESIS

The Xilinx Vivado Deign Suite provides High Level Synthesis (HLS) [6]. IP creation accelerates by allowing C, C++ and System C specifications which is directly targeted into Xilinx programmable devices without manually creating RTL. It provide faster pathway for IP creation. It Provides interfaces such as FIFO, AXI4, AXI4-Lite, and AXI4-Stream. Accelerated verification uses C/C++ test bench simulation, automatic VHDL/ Verilog simulation and test bench generation. Automatically on-chip memories, DSP elements and floating-point library are used of Xilinx. Figure2 shows the overview of design flow.

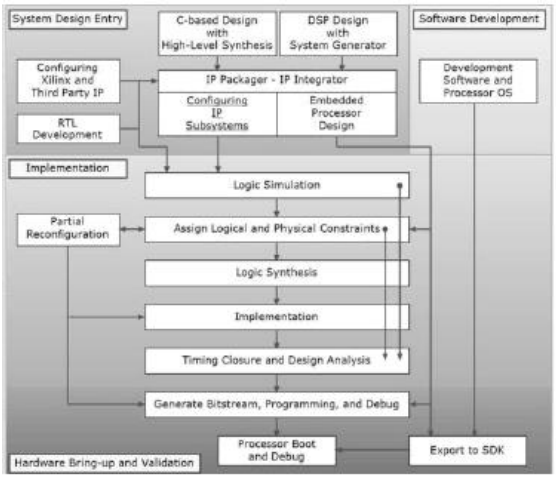

Figure2: Design Flow Overview

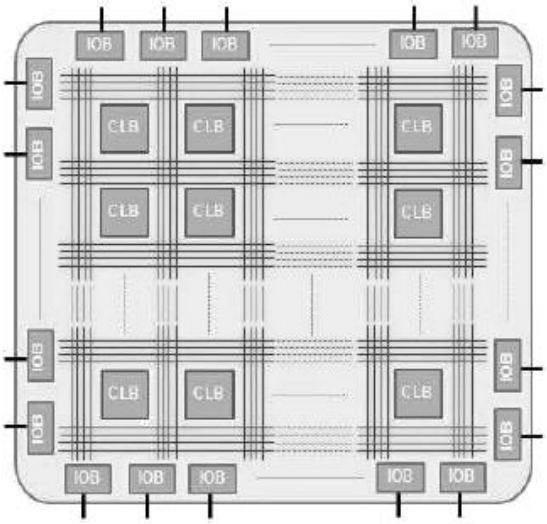

Figure3: Structure of a FPGA

VI. ZEDBOARD ZYNQ 7000 DEVELOPMENT BOARD

The Xilinx Zynq™-7000 ZedBoard development board is All Programmable FPGA SoC. This board provides platform to create a Linux, Android, Windows or other OS/RTOS based design [18]. The processing system (PS) and programmable logic (PL) I/Os act as expansion connectors.

VII. AXI INTERCONNECT SUBSYSTEM

The Advanced eXtensible Interface (AXI) is industry standard bus interface designed for FPGAs based on ARM AMBA (Advanced Microcontroller Bus Architecture) as a protocol for communication between blocks of IP.

There are three types of AXI protocol:

a) AXI4 is capable of doing memory map burst transaction up to 256 data transfer cycles per address phase.

b) AXI4-Lite utilizes for the single bit memory map transaction.

c) AXI-Stream where there is no address channel and it allows an unlimited burst transaction between the master and slave.

AXI transaction channels consists of Writing address channel, Writing data

channel, Write response channel, Read address channel and Read data channel.

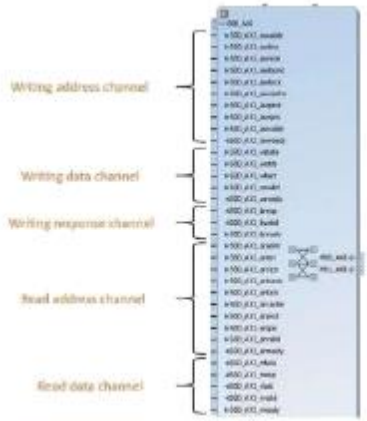

Figure4: AXI Transaction Channels

VIII. COMMUNICATION BETWEEN PL AND PS

AXI_GP ports are used for the general purpose application between the PL and PS. These are the main ports for the PS to access the PL and vise verse. Accelerator Coherency Port is the port provides access to the memory subsystems from the PL to the PS. Through this port, the PL can access the cache memories inside the PS which improves overall performance and power consumption. High performances (HP) are the memory map connection ports provide a high bandwidth data-path from the master modules in PL to the D-ram and on-chip memory (OCM) in PS. The AXI Interconnection is the established language between PS and PL of Zynq. The FPGA vendors such as Xilinx has amazingly made possible to combine software and hardware subsystems within a single chip, and AXI is the main system of communication between these subsystems. For a SoC designer accepting the AXI Interconnection is essential [5][7] .Figure5 shows AXI interconnection using Xilinx Vivado 18.X.

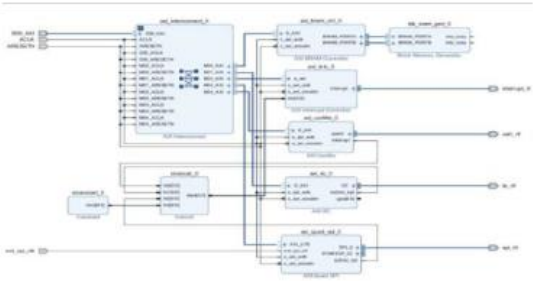

Figure5: AXI Interconnection

IX. GENERATING VIDEO USING ZYNQ-7000 SOC

The Xilinx Test Pattern Generator IP Core generates test patterns for Video System to bring up, evaluation and debug. This provides a large variety of tests patterns[6]. The user then enables to debug, access video system color, quality, edge and motion performance and issues related to quality issues. The AXI-4 Stream to Video out IP core is used to convert AXI4-Stream interface signals to a standard parallel video output interface with timing signals. Many external video sinks which contains standard video timing signals including Vsync, Hsync, Vblank, Hblank, DE and pixel clock where output is interfaced. The video processing blocks with an AXI4-Stream interface to an external video sink (DVI PHY) is enabled by video designers effortlessly and rapidly. With the help the Xilinx Video Timing Controller i.e VTC core to generate the video format timing signals this core works is combined.

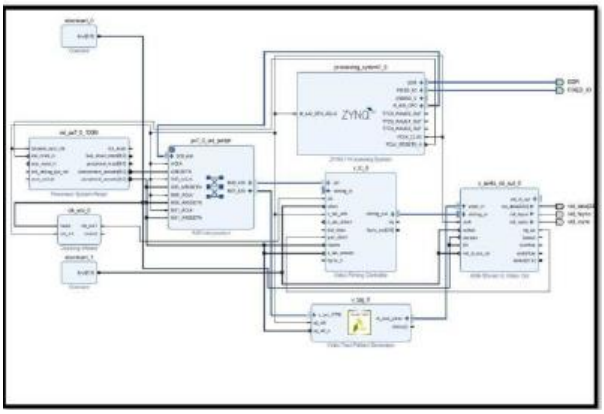

Figure6: Generating video using Zynq using Xilinx Vivado

X. AXI ETHERNET SUBSYSTEM

The AXI Ethernet Subsystem which implements tri-mode Ethernet MAC which supports the make use of of RMII, SGMII, RGMII, and 1000BASEX interface which connects media access control (MAC) to a physical side interface (PHY) chip where reduced media-independent interface (RMII), serial gigabit media independent interface (SGMII) and reduced gigabit media independent interface (RGMII) [8].The AXI Direct Memory Access (AXI DMA) IP provides high-bandwidth direct memory access between memory and AXI4-Stream-type target peripherals. Figure7, 8 and 9 describes AXI Ethernet Subsystem [6].

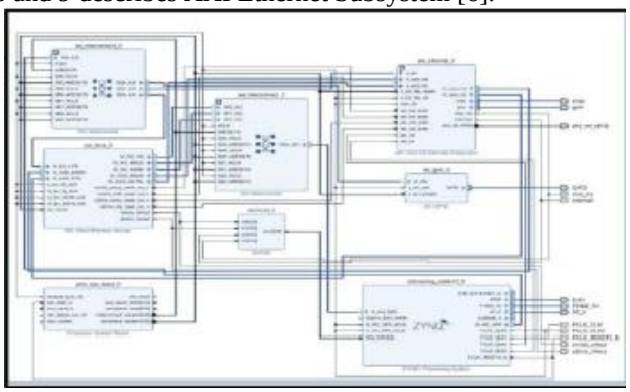

Figure7: Block design of AXI Ethernet Subsystem using Xilinx Vivado

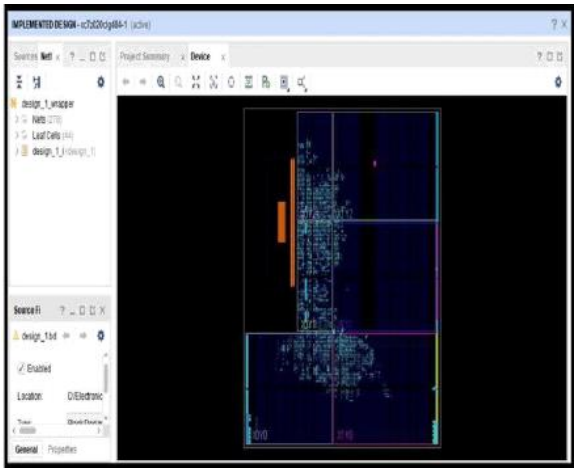

Figure8: Implemented Design floorplan of AXI Ethernet Subsystem using Xilinx Vivado

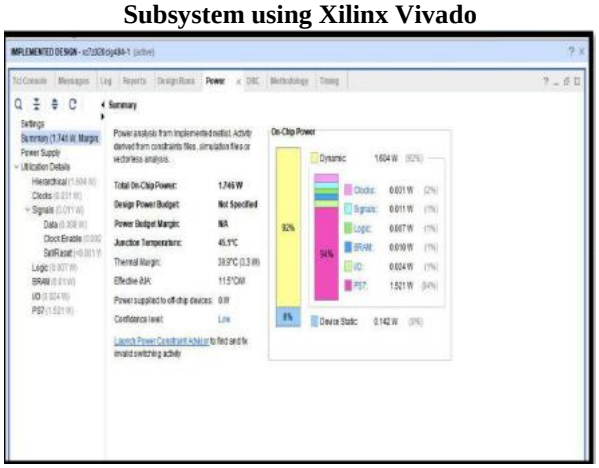

Figure9: Power Analysis of AXI Ethernet Subsystem

XI. AXI HDMI SUBSYSTEM

The HDMI is a proprietary audio or video crossing point. HDMI source acts like display controller for transmitting uncompressed video data and compressed or uncompressed digital audio data [13]. It's a digital replacement for analog video standards. The Video data (RGB/YUV) is AXI4-Stream mapped, pixel repeated, timed and then multiplexed with the AUX Data on a second AXI4-Stream. The video data stream which is produced is then divided into separate video streams for output as HDMI. The three identical data channels for RGB/YUV scramble the data before encoding as Transition Minimized Differential Signaling (TMDS) [13]. The data is oversampled and buffered before being serialized to provide the HDMI output.

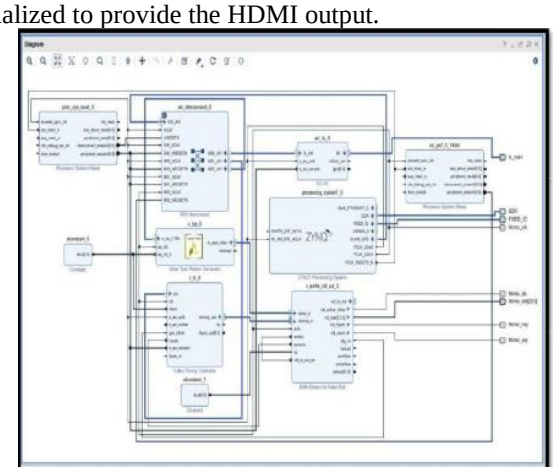

Figure10: Block design of AXI HDMI Subsystem using Xilinx Vivado

The three identical data channels for RGB/YUV scramble the data before encoding as TMDS (Transition Minimized Differential Signaling). The data is then oversampled and buffered before being serialized to provide the HDMI output.

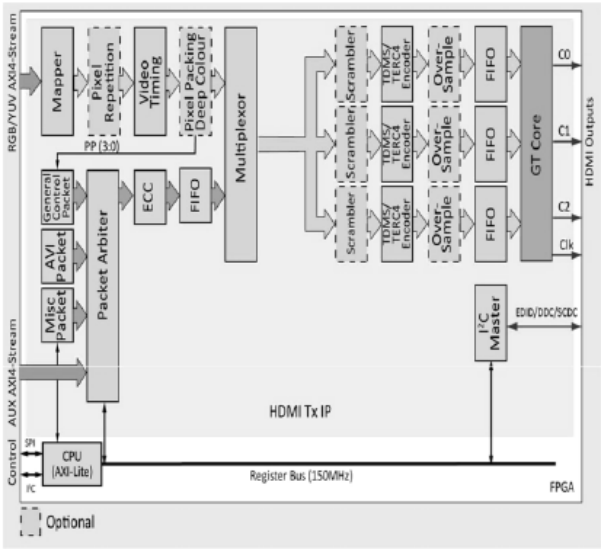

Figure11: Block design of HDMI Transmission (Tx) system

XII. CONCLUSION

The current paper attempts to design accelerator of HDMI and Ethernet is designed with the help of Xilinx Vivado 18.X. Here in this paper the architectural design of HDMI and Ethernet using AXI inter connection is discussed including building of IP system and subsystem. In the broadest sense, the term IoT consists of "things" (devices) from sensors to smart phones and wearable's are connected together which encompass everything connected to the internet. To make communication possible there is requirement of hardware and software connection and building of design for which HDMI and Ethernet AXI connection is build with the help of Xilinx Vivado using Zynq 7000 [9][10].

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