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Balanced XOR/XNOR Circuits using CNTFET

Anitha N, Srividya P

Abstract*: In this work, a standard design methodology in different logic styles using Carbon Nano Tube field effect transistor is proposed to construct Balanced XOR/XNOR circuit. The Proposed methodology is build on different basic cells to optimize area, power dissipation and delay. The circuits for Balanced XOR/XNOR can be designed with selecting a Elementary basic cell including two independent inputs and two complementary outputs. The basic cell is then combined with various correction and optimization techniques to build a perfect XOR/XNOR circuit to avoid weak zero and week one at the output. Simulation results of the proposed circuits shows better performances in terms of delay, power and PDP. The proposed circuits are evaluated using cadence virtouso.

Key words: CNTFET, Adder Circuits, Balanced XOR/XNOR Circuits, Low Power, Delay, power delay product.

I. INTRODUCTION

In an electronic world, Improvement in speed, reduction in power consumption and area are the most important parameters of a circuit. To achieve this, reducing the length of channel to below about 45nm leads to critical problems and challenges such as decreasing gate control, short channel effect, high power density, high sensitivity to process variation and exponential leakage current increment. For these reasons reducing the transistors size finally will stop at a point, leading to the development of new technologies that do not have above problem. Using carbon nano-tube technology, above mentioned problems can be avoided and high speed and lower power dissipation can be achieved by designing an electronic circuits with miniaturization [6].
This paper concentrates on XOR/XNOR design as it finds application in parallel multiplication circuits, comparator, parity checker, multiplexer, adders and so on. A systematic cell design of balanced XOR/XNOR circuits for hybrid CMOS logic using Carbon Nano Tube Field Effect Transistor (CNTFET) is proposed. The work mainly concentrates on reducing the power dissipation, delay and power delay product which forms the important parameters in low power and high speed applications.

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II. ELEMENTARY BASIC CELL FOR BALANCED XOR/XNOR DESIGN

A. Elementary Basic Cell

Elementary basic cell shown in figure 1 consists of four CNTFET transistors, each of which has two inputs and two outputs. Inputs are connected to gate and either drain or source. Outputs are XOR and XNOR functions. The next section explains the different basic cells construction.

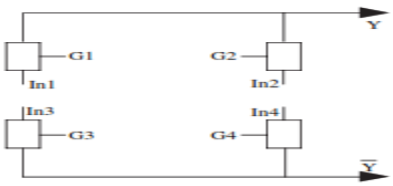

Figure. 1: Elementary Basic Cell

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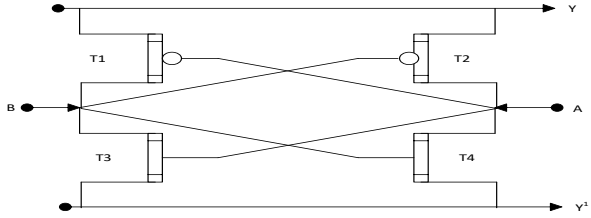
B. Different Basic Cell

Depending on the types of CNTFETs and input excitation different basic cells [3] were constructed as shown in Table1

Table1: Different Basic Cells

Diff. Cell	Types of CNTFETs				Inputs							
					Gate Signals				D or S signals			
	T 1	T 2	T 3	T 4	G1	G2	G3	G 4	In 1	In 2	In 3	In 4
BC1	P	P	N	N	A	B	A	B	B	A	B	A
BC2	N	N	N	N	A^1	B	A	B	B	A^1	B	A
BC3	P	P	P	P	A	B	A^1	B	B	A	B	A^1
BC4	N	P	P	N	B	B	B	B	A^1	A	A^1	A
BC5	P	N	P	N	B^1	B^1	B	B	A^1	A	A^1	A

As per the transistor types and applied inputs five basic cell circuit connections were made shown in Figure. 2 to Figure.6 and working is explained in Table2 to Table6.



. Figure 2: Basic Cell-1

Table2: Basic Cell-1 circuit input and output values.

Inputs		Transistors State				outputs			
A	B	T1	T2	T3	T4	Y	Y^1	Y	Y^1
0	0	on	on	off	off	A, B	--	0-	HiZ
0	1	on	off	off	on	B	A	1	0
1	0	off	on	on	off	A	B	1	0
1	1	off	off	on	on	--	A, B	HiZ	1-

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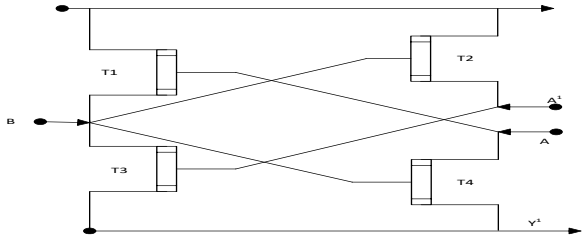

Figure 3: Basic Cell-2

Table3: Basic Cell-2 circuit input and output values.

Inputs		Transistors State				outputs			
A	B	T1	T2	T3	T4	Y	Y^I	Y	Y^I
0	0	off	off	on	off	B	--	0	HiZ
0	1	off	on	on	on	A^I, B	A	1-	0
1	0	on	off	off	off	--	B	HiZ	0
1	1	on	on	on	on	A^I	A, B	0	1-

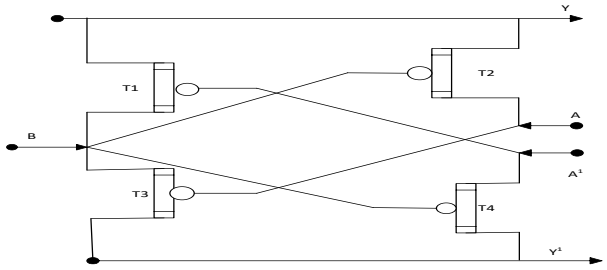

Figure 4: Basic Cell-3

Table4: Basic Cell-3 circuit input and output values.

Inputs		Transistors State				outputs			
A	B	T1	T2	T3	T4	Y	Y^I	Y	Y^I
0	0	off	on	on	on	A, B	A^1	0-	1
0	1	off	off	on	off	B	--	1	HiZ
1	0	on	on	off	on	A	A^1, B	1	0-
1	1	on	off	off	off	--	B	HiZ	1

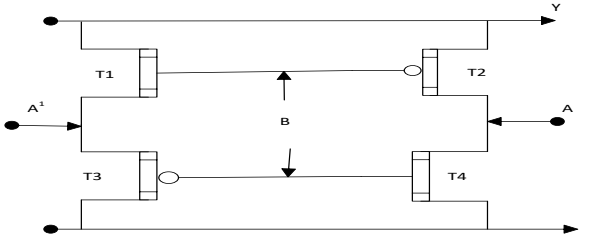

Figure 5: Basic Cell-4

Table5: Basic Cell-4 circuit input and output values.

Inputs		Transistors State				outputs			
A	B	T1	T2	T3	T4	Y	Y^I	Y	Y^I
0	0	off	on	on	off	A	A^1	0-	1
0	1	on	off	off	on	A^1	A	1-	0
1	0	off	on	on	off	A	A^1	1	0-
1	1	on	off	off	on	A^1	A	0	1-

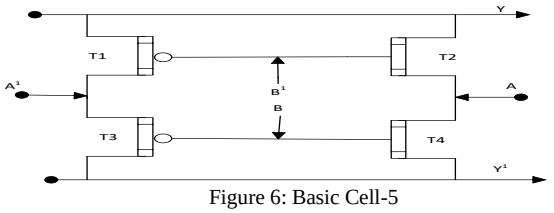

Figure 6: Basic Cell-5

Table6: Basic Cell-5 circuit input and output values.

Inputs		Transistors State				outputs			
A	B	T1	T2	T3	T4	Y	Y^I	Y	Y^I
0	0	off	on	on	off	A	A^1	0	1
0	1	on	off	off	on	A^1	A	1	0
1	0	off	on	on	off	A	A^1	1-	0-
1	1	on	off	off	on	A^1	A	0-	1-

In Table2 to Table6, 0- and 1- represents weak 0 and weak 1 respectively, HiZ (--) indicates high impedance state. To get strong 1 and strong 0, and also to avoid high impedance state corrections and optimization mechanism are used. Section II explains corrections and optimization mechanism.

III. CORRECTION AND OPTIMIZATION MECHANISM

A. Introduction of Feedback Network

All circuits with complementary outputs have the ability to optionally determine the state of an output or amplify it through the use of another output and a suitable transistor. Transistors which are placed between the two outputs to influence the second output through activating the first one, are called feedback networks. This feedback network is placed between the two complementary outputs and causes the high impedance output states to be eliminated and replaced by the desired levels.

Also, it is possible to ensure full swing operation at the outputs. As different basic cell versions presented in this, required different feedback network. In Figure 7 four different feedback networks are presentd: Fp-CNTFET, Fn_CNTFET, Fc-CNTFET and Fnp-CNTFET.

Fp-CNTFET is a feedback network using two p-CNTFET transistors. Fn-CNTFET is a feedback network with two n-CNTFET transistors. Fc-CNTFET is a complementary feedback network and Fnp-CNTFET includes n-CNTFET and p-CNTFET transistors placed between the two complementary outputs Y and Y^1. The driving capability of feedback networks improved as V_{DD} and GND connections are used.

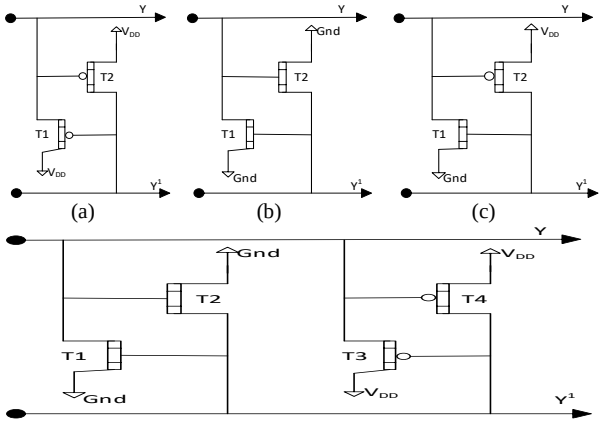

Figure 7: (a) Fp-CNTFET, (b) Fn-CNTFET, (c) Fc-CNTFET (d) Fnp-CNTFET feedback network.

B. Pull Up and Pull Down Networks

The use of pull up and pull down networks are used to eliminating the critical states of a circuit [1][2]. In Section 2 several basic cells were introduced. Studying the behaviour of these cells using their truth table shows that except for BC4 and BC5, all other cells are not complete XOR–XNOR circuits. In order to complete the behaviour of these cells high impedance states should be replaced by "0" or "1". One possible solution is to use pull up and pull down networks.

When facing output high impedance states, it is possible to use a pull up network to connect Y or Y^1 to the supply voltage. This results in replacing the high impedance state by logic "1". To replace a high impedance state with logic "0",

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a pull down network is used to connect the output to ground.

C. Bootstrap Technique

The gate voltage of transistor is changed by placing the boot transistor between input and the gate terminal of the transistor. The changed threshold voltage of the transistor is greater than or equal to the threshold voltage of (V_T) of transistor, then the transistor output will not be degraded and there is no voltage drop due to transistor's threshold voltages. Empirical results and evaluation of the circuit discloses that, boot strapping and main transistors should be of the similar type in order to provide capacitive property and for the boot phenomenon to occur.

D. Output Inverters

To ensure full swing operation at the outputs, inverters are used at the output. Using this mechanism for the basic cells introduced in section 2 eliminated the non full swing operation but can't replace high impedance states.

IV. INTRODUCTION TO CNTFET BALANCED XOR/XNOR CIRCUITS BASED ON PASS TRANSISTORS

In Section 2 five basic cells were introduced. These cells are having high impedance state and producing non-full swing outputs which refers to the unbalanced operation. The designing of a balanced XOR/XNOR circuits involve two steps one is by eliminating high impedance output state and other is to clamp the non full swing output. To fix this issue Correction mechanisms are employed. Considering the above limitations, it appears that in most cases, more than one correction mechanism is needed for basic cells, requiring a combination of correction mechanisms to optimize the circuit.

A. Class A XOR/XNOR Circuits using CNTFET

In this section, feedback networks are used in basic cell to construct balanced XOR/XNOR circuits to produce balanced output signals. The proper feedback network is selected for each basic cell to avoid high impedance output state and to get full swing. The constructed balanced XOR/XNOR circuits are called as class A circuits with the names from X1 to X5. The class A circuits from X1 to X5 are shown in Figure 8(a) to 8(e). X1 to X5 are presented with proper correction mechanism which eliminates high impedance output and producing full swing output.

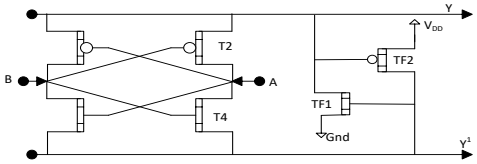

Figure 8(a): X1 Circuit

Table7: X1 circuit input and output values

Inputs		Outputs							
		Without Correction mechanism				Correction mechanism			
A	B	Y	Y^1	Y	Y^1	Y	Y^1	Y	Y^1
0	0	A, B	--	0-	HiZ	A, B	1	0	1
0	1	B	A	1	0	B	A	1	0
1	0	A	B	1	0	A	B	1	0
1	1	--	A B	HiZ	1-	0	A, B	0	1

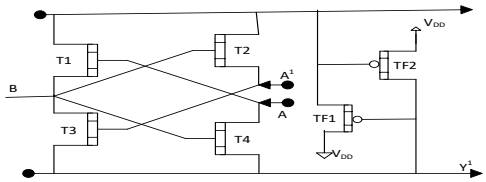

Figure 8(b): X2 Circuit

Table8: X2 circuit input and output values

Inputs		Outputs							
		Without Correction mechanism				Correction mechanism			
A	B	Y	Y^1	Y	Y^1	Y	Y^1	Y	Y^1
0	0	B	--	0	HiZ	B	1	0	1
0	1	A^1, B	A	1-	0	A^1, B	A	1	0
1	0	--	B	HiZ	0	1	B	1	0
1	1	A^1	A, B	0	1-	A^1	A, B	0	1

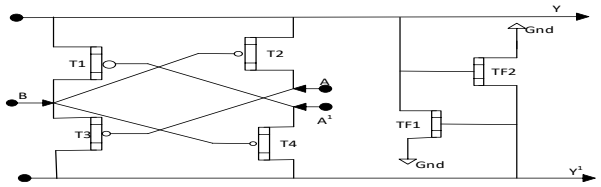

Figure 8(c): X3 Circuit

Table9: X3 circuit input and output values

Inputs		Outputs							
		Without Correction mechanism				Correction mechanism			
A	B	Y	Y^1	Y	Y^1	Y	Y^1	Y	Y^1
0	0	A, B	A^1	0-	1	A, B	A^1	0	1
0	1	B	--	1	HiZ	B	0	1	0
1	0	A	A^1, B	1	0-	A	A^1, B	1	0
1	1	--	B	HiZ	1	0	B	0	1

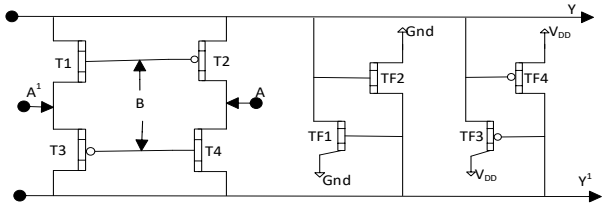

Figure 8(d) : X4 Circuit

Table10: X4 circuit input and output values

Inputs		Outputs							
		Without Correction mechanism				Correction mechanism			
A	B	Y	Y^1	Y	Y^1	Y	Y^1	Y	Y^1
0	0	A	A^1	0-	1	A	A^1	0	1
0	1	A^1	A	1-	0	A^1	A	1	0
1	0	A	A^1	1	0-	A	A^1	1	0
1	1	A^1	A	0	1-	A^1	A	0	1

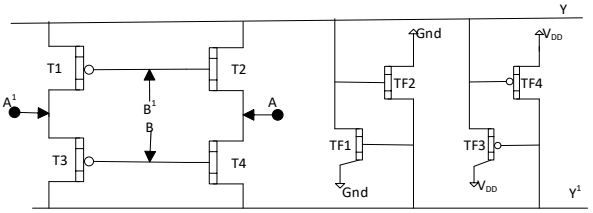

Figure 8(e): X5 Circuit

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Table 11: X5 circuit input and output values

Inputs		Outputs							
		Without Correction mechanism				Correction mechanism			
A	B	Y	Y^1	Y	Y^1	Y	Y^1	Y	Y^1
0	0	A	A^1	0	1	A	A^1	0	1
0	1	A^1	A	1	0	A^1	A	1	0
1	0	A	A^1	1-	0-	A	A^1	1	0
1	1	A^1	A	0-	1-	A^1	A	0	1

B. Class B XOR/XNOR Circuits using CNTFET

In this section, pull up and pull down networks are employed in basic cells to eliminate critical states and feedback networks are employed to get balanced output. The pull up, pull down and feedback networks are used simultaneously. The constructed balanced XOR/XNOR circuits are grouped as class B circuits with names X6 through X16. Figure 9(a) to Fig 9(k) represents class B X6 to X16 circuits.

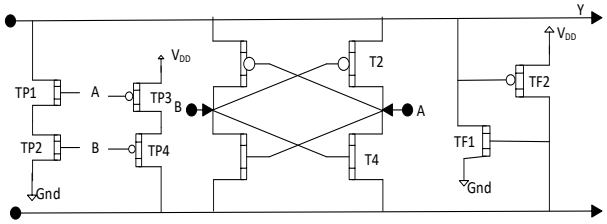

Figure 9(a): X6 Circuit

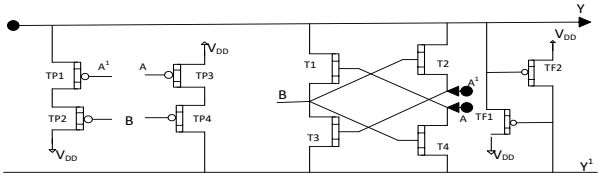

Figure 9(b): X7 Circuit

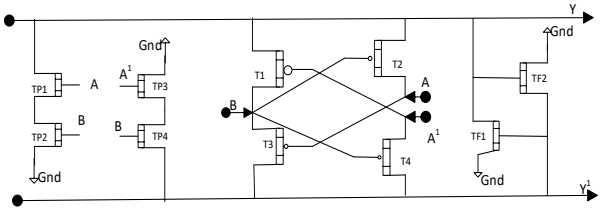

Figure 9(c): X8 Circuit

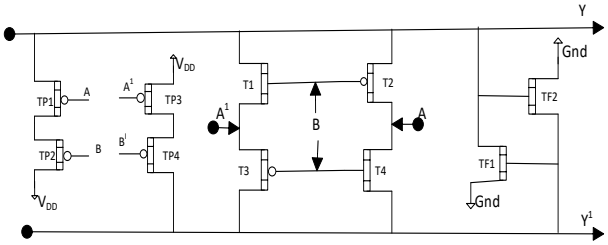

Figure 9(d): X9 Circuit

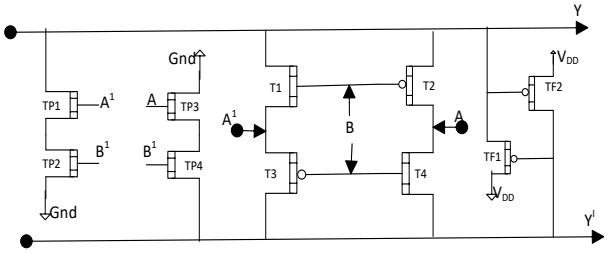

Figure 9(e): X10 Circuit

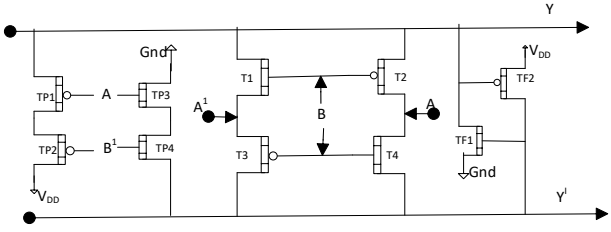

Figure 9(f): X11 Circuit

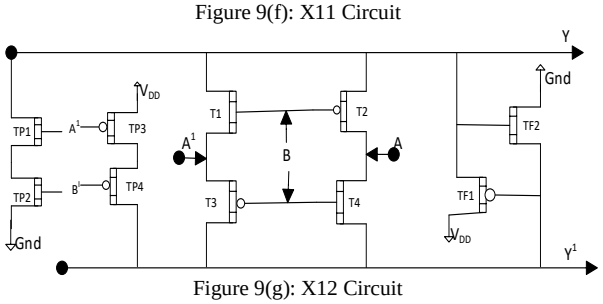

Figure 9(g): X12 Circuit

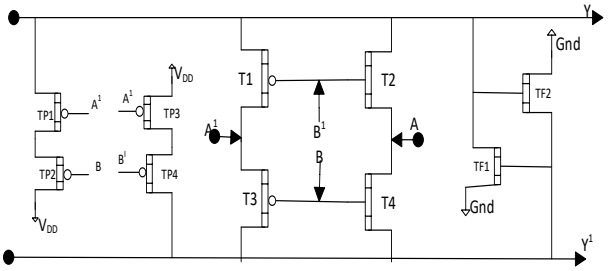

Figure 9(h): X13 Circuit

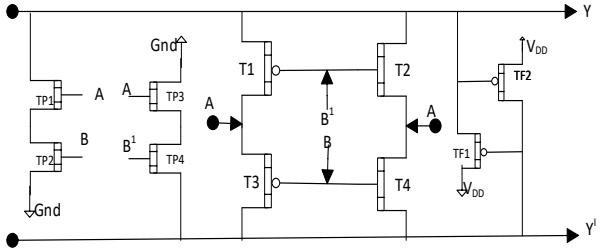

Figure 9(i): X14 Circuit

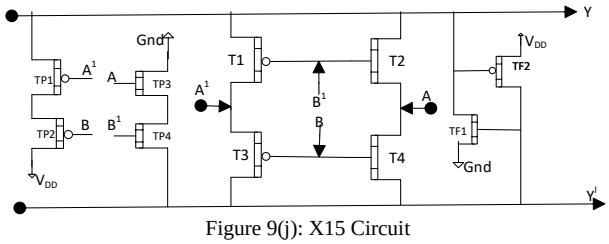

Figure 9(j): X15 Circuit

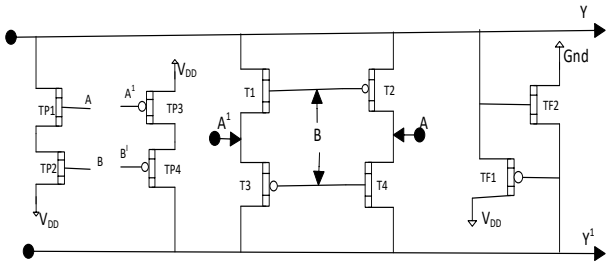

Figure 9(k): X16 Circuit

C. Class C XOR/XNOR Circuits using CNTFET

Class C includes XOR–XNOR circuits using the bootstrap technique. In both circuits two p-CNTFET and two n-CNTFET transistors are connected between the input and the gate terminal of the main transistor to obtain balanced output. The gate of the bootstrap p-CNTFET transistors is always connected to GND. Meanwhile the n-CNTFET transistors are always connected to V_{DD}. Figure 10(a) and Figure 10(b) shows X17 and X18 circuits.

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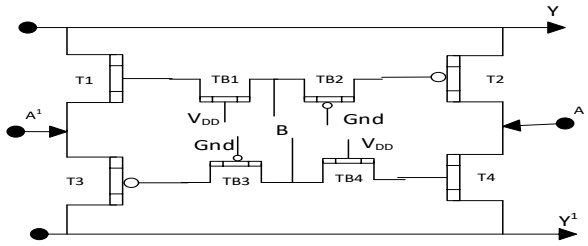

Figure 10(a): X17 Circuit

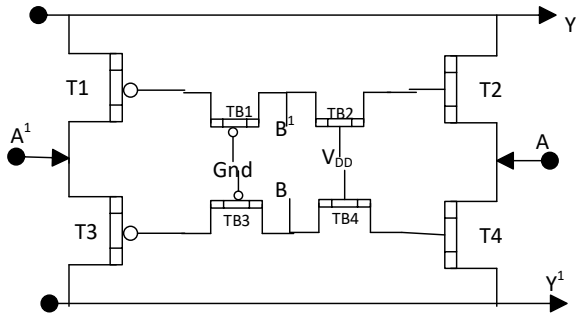

Figure 10(b): X18 Circuit

D. Class D XOR/XNOR Circuits using CNTFET

In class D circuits bootstrap technique has been employed to obtain balanced output. Pull up and pull down networks are employed to avoid high impedance output state to the basic cells BC1, BC2 and BC3 since they all suffer from unbalanced output as well as high impedance state at the output. Circuits X19, X20 and X21 in class D are upgraded versions of BC1, BC2 and BC3 respectively. Figure 11(a) to Figure 11(c) shows the circuit diagrams from X19 to X21.

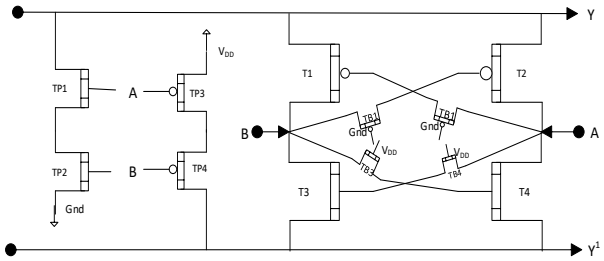

Figure 11(a): X19 Circuit

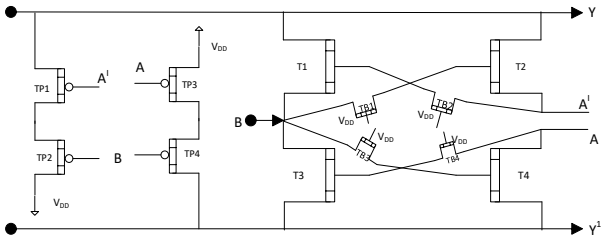

Figure 11(b): X20 Circuit

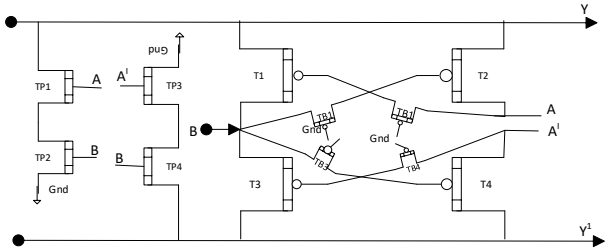

Figure 11(c): X21 Circuit

E. Class E XOR/XNOR Circuits using CNTFET

In class E circuits bootstrap technique has been employed to provide balanced output and to avoid high impedance states at the outputs by using feedback networks. Circuits X22, X23 and X24 in class E networks are based on BC1, BC2 and BC3 respectively. Figure 12(a) to Figure 12(c) shows the circuit diagrams of X22 to X24.

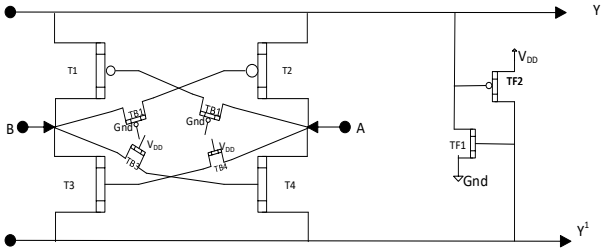

Figure 12(a): X22 Circuit

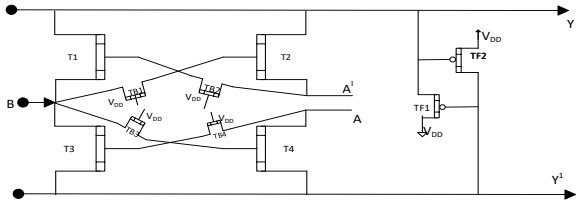

Figure 12(b): X23 Circuit

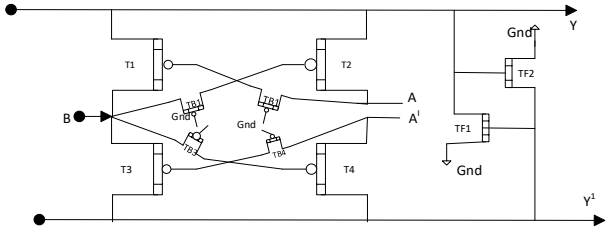

Figure 12(c): X24 Circuit

F. Class F XOR/XNOR Circuits using CNTFET

Class F includes circuits X25 and X26 which are built using BC4 and BC5 respectively. In these circuits output inverters are used at Y and Y^1 to provide signal level restoration. Figure 13(a) and Figure 13(b) shows the circuit diagrams of X25 and X26.

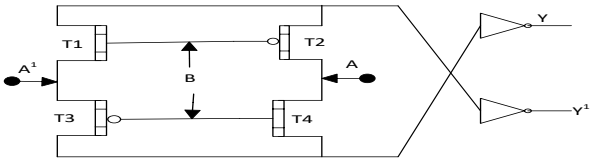

Figure 13(a): X25 Circuit

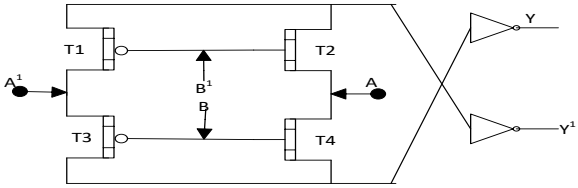

Figure 13(b): X26 Circuit

G. Class G XOR/XNOR Circuits using CNTFET

Class G includes circuits X27, X28 and X29 which are constructed by removing the bootstrapping transistors from X19, X20 and X21 respectively.

To provide full swing at the output, inverters are used at outputs. Figure 14(a) to Figure 14(c) shows the circuit diagram of X27 to X29.

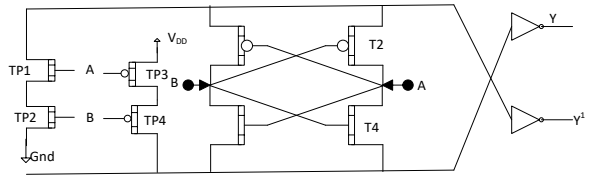

Figure 14(a): X27 Circuit

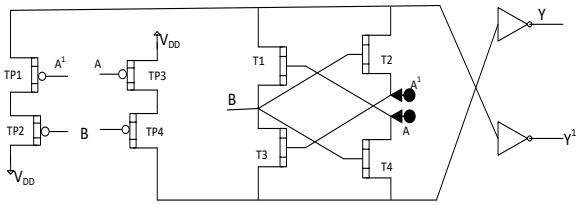

Figure 14(b): X28 Circuit

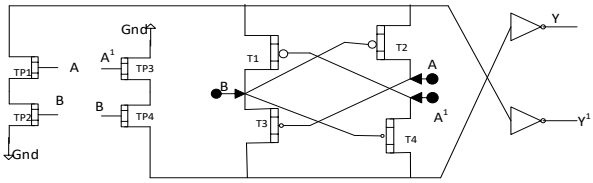

Figure 14(c): X29 Circuit

H. Class H XOR/XNOR Circuits using CNTFET

Class H includes X30, X31 and X32 which are constructed by X22, X23 and X24 by removing the bootstrapping transistors. To provide full swing at output, output inverters are used. Figure 15(a) to Figure 15(c) shows the circuit diagram of X30 to X32.

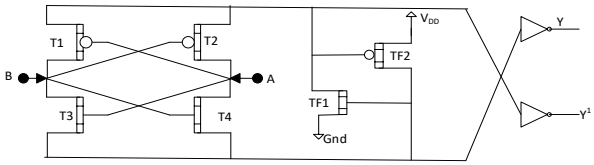

Figure 15(a): X30 Circuit

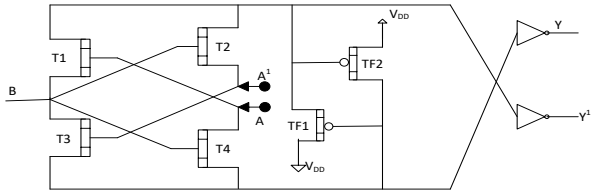

Figure 15(b): X31 Circuit

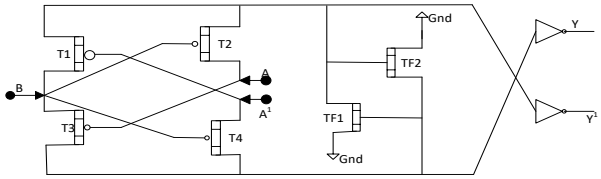

Figure 15(c): X32 Circuit

V. SIMULATION RESULT AND ANALYSIS

The execution of the balanced XOR/XNOR circuits are analyzed in terms of delay, power consumption and PDP using CNTFET. All 32 circuits are designed using cadence virtuoso and are simulated using spectre model.

Table 12: Area, Power dissipation and PDP of proposed Circuits

Class	Name	No. of transistors	Power dissipation in nw	Delay in ns	PDP in femto
A	X1	6	104.8	11.22	1.17586
	X2	8	301.9	11.47	3.46279
	X3	8	55.03	11.06	0.6086
	X4	10	268.4	11.31	3.0356
	X5	10	300.6	11.51	3.46
B	X6	10	121	11.24	1.36
	X7	12	119.5	11.05	1.32
	X8	12	66.6	11.11	0.74
	X9	14	90.69	11.21	1.017
	X10	14	105.8	11.03	1.167
	X11	14	143.7	11.19	1.608
	X12	14	196.7	11.03	2.17
	X13	14	94.25	11.16	1.052
	X14	14	120	11.14	1.337
	X15	14	141.8	11.14	1.58
	X16	14	127.5	11.14	1.42
C	X17	10	0.000123	0.000932	1.15E-7
	X18	12	0.003605	0.000603	2.174E-6
D	X19	12	16.67	11.06	0.1844
	X20	14	49.86	5.939	0.296
	X21	14	59.2	11.06	0.6548
E	X22	10	125.7	11.43	1.437
	X23	12	666.3	11.07	7.376
	X24	12	56.08	11.07	0.621
F	X25	10	66.55	11.39	0.758
	X26	12	64.44	11.14	0.718
G	X27	12	24.03	11.09	0.2665
	X28	14	63.73	11.09	0.7068
	X29	14	64.25	60.23	3.87
H	X30	10	121.7	11.27	1.3716
	X31	12	358.5	11.5	4.123
	X32	12	30.07	11.09	0.333

VI. CONCLUSION

As compared to the simulation result of the balanced XOR/XNOR circuits, the X19, X24, X25, X26, X27 and X32 circuits have less PDP and less no. of transistors. Hence, they are all best suitable to use in digital circuit design as designer requires less power consumption, delay and area. In class C X17 and X18 circuits give less PDP compared to other circuits but level degradation present in the output, that leads to further complication if it is used in digital circuits. In comparison with the XOR/XNOR circuits power dissipation is 46.6E-9w and delay is 10.14E-9sec but no. of transistors are 14.

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