Low Power 32 x 32 – bit Reversible Vedic Multiplier

Ansiya Eshack, S. Krishnakumar

Abstract*: Recently, low-power consuming devices are gaining demand due to excessive use and requirement of hand-held & portable electronic gadgets. The quest for designing better options to lower the power consumption of a device is in high-swing. The paper proposes two 32 x 32 – bit multipliers. The first design is based only on the Urdhava Tiryakbhyam Sutra of Vedic Mathematics. The use of this sutra has created a multiplier with higher throughput and lesser power utilization than conventional 32 x 32 – bit multipliers. The second design incorporates the reversible logic into the first design, which further reduces the power consumption of the system. Thus bringing together Vedic sutra for multiplication and reversible gates has led to the development of a Reversible Vedic Multiplier which has both the advantages of high-speed and low-power consumption.

***Index Terms*: FPGA, High speed, Low power, Reversible Gates, Urdhava Tiryakbhyam Sutra, Vedic Multiplier.**

I. INTRODUCTION

Low power usage is a major requisite in electronic systems. The demand of such systems is inversely proportional to its power consumption. Increased throughput of the system is an added advantage and the market is in need for such systems. Multiplication is an unavoidable process for systems dealing in signal processing, acoustics, communication and wireless technology [1]. The greater the bit size of the input to the multiplier, the greater the delay in receiving the output. Many research works have been focused on reducing the power requirement and decreasing the delay in generating outputs of a multiplier [2]. To develop a system with greater speed and lower power consumption, it is thus required to optimize the multipliers [3]. It has been understood that Vedic multipliers produce faster response than standard multipliers. Also use of Reversible logic gates limits the use of power. These two techniques are employed together to design two 32 x 32 – bit multipliers, both of which consume low power and provide quick outputs. Vedic Mathematics, is well-known for its simplicity and mental calculation capability [4]. It is a collection of 16 different formulae, applicable to all areas of mathematics like arithmetic, geometry, calculus, algebra, trigonometry and conics [3], [5]. The Urdhava Tiryakbhyam (UT) sutra is the only formula in Vedic Mathematics, out of the 16, which is applicable for all general types of multiplication [6]. The use of this sutra allows parallel generation of partial products (PP) during multiplication. The final output is got faster due to this process and thus greatly improves the speed of the system [7].

Reversible logic is a key area attracting a lot of research in the past decades [8]. Circuits employing reversible gates are low power-consuming as they do not lose information during the logic implementation. A reversible gate is represented by 'n * n' which indicates it has 'n' inputs and 'n' outputs. There is a one to one mapping between the inputs and outputs of a reversible gate [9], [10]. Most notable reversible gates are Fredkin, Toffoli and Peres [11].

The paper presents two designs of 32 x 32 – bit multiplier. The first design applies the UT Sutra for performing the multiplication. Results show this design utilizes less power and has high speed. The second design makes use of Reversible logic gates along with the UT sutra. It employs 3 * 3 Toffoli gates for the logic execution. It is observed that this multiplier consumes lower power than the 1st design.

The rest of the paper is as follows: Section II deals with Vedic mathematics and the UT sutra. The reversible gates are described in Section III. The design and implementation of the two 32 x 32 – bit multipliers are explained in Section IV. Results and discussion are provided in Section V, and conclusion in Section VI.

II. VEDIC MATHEMATICS AND UT SUTRA

Vedic Mathematics is the contribution of Shri Bharati Krishna Tirthaji Maharaja and is based on the Vedas [3]. It contains sutras (formulae) which help solve mathematical problems a lot easier and faster than the conventional system of mathematics. His findings were published in a book called Vedic Mathematics. It has been observed that use of Vedic Mathematics to solve problems reduces the time taken for calculation, when compared with regular mathematics [6]. The advantage of this is the use of mental calculations and little or no use of pen and paper to reach the results.

The **UT sutra** is one of the 16 sutras in Vedic mathematics. This sutra meaning "Vertical and Crosswise" follows vertical and crosswise multiplication between the bits of the input [12]. It follows a pattern which can be represented by a line diagram. The line diagram of a multiplier having two 2 – bit inputs, 4 – bit inputs and 8 – bit inputs are shown in Fig. 1(a), (b) and (c).

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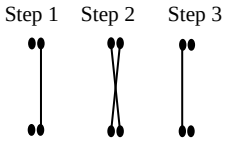

Fig. 1 (a) Line diagram of a 2 x 2 – bit multiplier using UT sutra

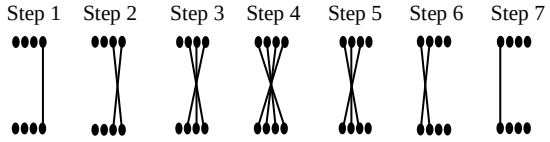

Fig. 1 (b) Line diagram of a 4 x 4 – bit multiplier using UT sutra

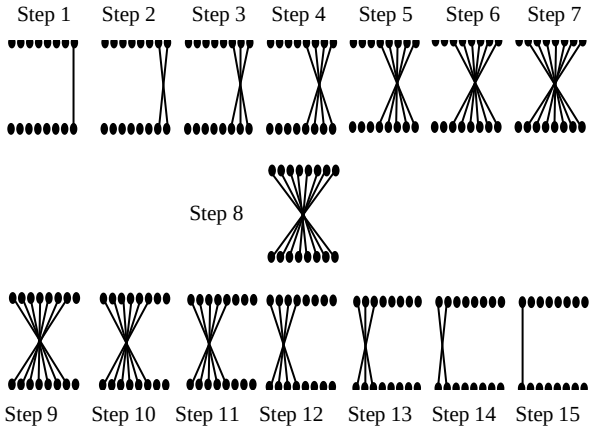

Fig. 1(c) Line diagram of an 8 x 8 – bit multiplier using UT sutra

The number of steps required during multiplication is one less than the total number of bits of the two inputs. For example, 2 x 2 bit multiplier has a total of 4 bits as inputs, and so it has 3 steps in the multiplication process. Similarly, a 4 x 4 bit multiplier and 8 x 8 bit multiplier have 8 bits and 16 bits as inputs, and so the number of steps required are 7 and 15 respectively. This same concept is used in higher order multipliers, and so it is understood that a 16 x 16 bit and 32 x 32 bit multipliers require 31 and 63 steps respectively.

Let's find the multiplication output of two 8 – bit binary numbers as an example. A total of 15 steps are required for this, which includes both vertical and cross wise multiplication. The products got in each step are called as PPs and, so the entire multiplication process generates 15 PPs. Let the numbers be 10111011 and 11011101.

10111011 x
11011101

$$1)PP_1 = \begin{matrix}1011101\\1101110\end{matrix}\begin{pmatrix}1\\1\end{pmatrix} = 1*1 = 1$$

$$2)PP_2 = \begin{matrix}101110\\110111\end{matrix}\begin{pmatrix}11\\01\end{pmatrix} = 1*1+0*1 = 1$$

$$3)PP_3 = \begin{matrix}10111\\11011\end{matrix}\begin{pmatrix}011\\101\end{pmatrix} = 1*1+1*0+0*1 = 1$$

$$4)PP_4 = \begin{matrix}1011\\1101\end{matrix}\begin{pmatrix}1011\\1101\end{pmatrix} = 1*1+0*0+1*1+1*1 = 11$$

$$5)PP_5 = \begin{matrix}101\\110\end{matrix}\begin{pmatrix}11011\\11101\end{pmatrix} = 1*1+1*0+0*1+1*1+1*1 = 11$$

$$6)PP_6 = \begin{matrix}10\\11\end{matrix}\begin{pmatrix}111011\\011101\end{pmatrix} = 1*1+1*0+1*1+0*1+1*1+1*0 = 11$$

$$7)PP_7 = \begin{matrix}1\\1\end{matrix}\begin{pmatrix}0111011\\1011101\end{pmatrix} = 0*1+1*0+1*1+1*1+0*1+1*0+1*1 = 11$$

$$8)PP_8 = \begin{pmatrix}10111011\\11011101\end{pmatrix} = 1*1+0*0+1*1+1*1+1*1+0*0+1*1+1*1 = 110$$

$$9)PP_9 = \begin{pmatrix}1011101\\1101110\end{pmatrix}\begin{matrix}1\\1\end{matrix} = 1*0+0*1+1*1+1*1+1*0+0*1+1*1 = 11$$

$$10)PP_{10} = \begin{pmatrix}101110\\110111\end{pmatrix}\begin{matrix}11\\01\end{matrix} = 1*1+0*1+1*1+1*0+1*1+0*1 = 11$$

$$11)PP_{11} = \begin{pmatrix}10111\\11011\end{pmatrix}\begin{matrix}011\\101\end{matrix} = 1*1+0*1+1*0+1*1+1*1 = 11$$

$$12)PP_{12} = \begin{pmatrix}1011\\1101\end{pmatrix}\begin{matrix}1011\\1101\end{matrix} = 1*1+0*0+1*1+1*1 = 11$$

$$13)PP_{13} = \begin{pmatrix}101\\110\end{pmatrix}\begin{matrix}11011\\11101\end{matrix} = 1*0+0*1+1*1 = 1$$

$$14)PP_{14} = \begin{pmatrix}10\\11\end{pmatrix}\begin{matrix}111011\\011101\end{matrix} = 1*1+0*1 = 1$$

$$15)PP_{15} = \begin{pmatrix}1\\1\end{pmatrix}\begin{matrix}0111011\\1011101\end{matrix} = 1*1 = 1$$

The carry of each step is added to the PP of the next step and thus the final output is got.

III. REVERSIBLE GATES

The traditional logic gates dissipate k T log (2) Joules of energy for every bit of information lost during the operation [13]. This power loss is very significant in the present scenario where large number of operations are performed in a small duration of time, and in a very small area. When computations are made lossless in terms of information, the energy loss can be eliminated. Reversible circuits built with only reversible gates have zero power dissipation, and therefore find great application in areas with limited power.

Reversible gates always have equal number of inputs and outputs [14]. Also, each output of these gates has a corresponding input. Reversible circuits are made by combining reversible gates and have no fan outs or loops. Depending on the application, some inputs in a reversible circuit are kept constant. At the output side also, some outputs are not used and termed as garbage outputs.

The Toffoli gate and the Peres gate are two 3*3 gates which are used for multiplication of two single bits. However, the Peres gate has a higher delay compared to Toffoli gate [15]. Due to this, the present work utilizes the Toffoli gate. The truth table and functional representation of a Toffoli gate is given in Fig. 2. When the input, Z, is kept constant at "0", the output R is the product of the two other inputs [16]. This is shown in Table I.

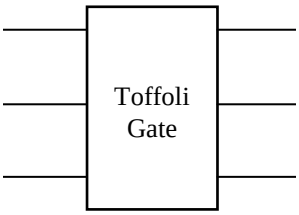

Fig. 2. Toffoli Gate

Table I. Truth table when input Z is "0"

Inputs			Output
X	Y	Z	R
0	0	0	0
0	1	0	0
1	0	0	0
1	1	0	1

IV. DESIGNED MULTIPLIERS

Two designs of 32 x 32 – bit multiplier are presented here. The first design uses the UT sutra while the second design includes the reversible logic gates, along with the UT sutra. Both the designs are modeled using Verilog hardware description language and implemented on the Virtex - 5 series of FPGA.

A. 32 x 32 – bit Vedic Multiplier

The two inputs to the multiplier are 32 bits and the output will be 64 bits. Let the inputs be $a_{32}a_{31}a_{30}$ …. $a_3a_2a_1$ and $b_{32}b_{31}b_{30}$ … $b_3b_2b_1$.

According to the UT sutra, there shall be 63 steps containing vertical and cross-wise multiplications resulting in partial products which can be added together to get the final output. The first ten steps in the line diagram of a 32 x 32 bit multiplier is shown in Fig 3.

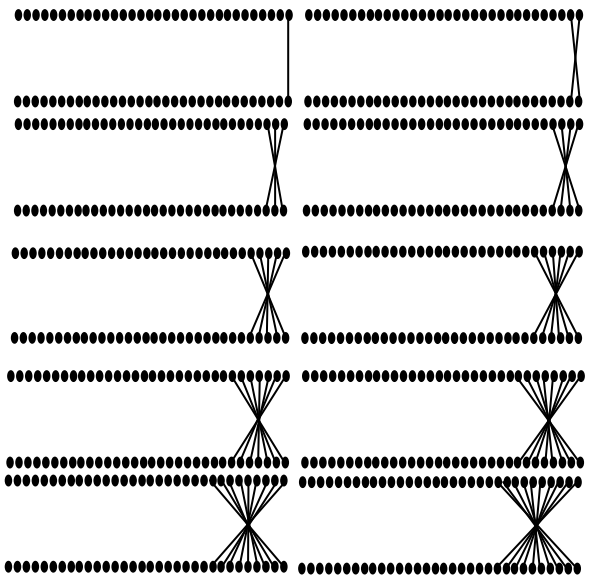

Fig. 3 Line diagram of a 32 x 32 – bit multiplier using UT sutra

The steps in Fig 3. can be written as:

$$1)PP_1 = \begin{matrix} a_{32}a_{31}a_{30}...a_3a_2 \\ b_{32}b_{31}b_{30}...b_3b_2 \end{matrix}\begin{pmatrix} a_1 \\ b_1 \end{pmatrix} = a_1 * b_1$$

$$2)PP_2 = \begin{matrix} a_{32}a_{31}a_{30}...a_3 \\ b_{32}b_{31}b_{30}...b_3 \end{matrix}\begin{pmatrix} a_2a_1 \\ b_2b_1 \end{pmatrix} = a_2 * b_1 + a_1 * b_2$$

$$3)PP_3 = \begin{matrix} a_{32}a_{31}a_{30}... \\ b_{32}b_{31}b_{30}... \end{matrix}\begin{pmatrix} a_3a_2a_1 \\ b_3b_2b_1 \end{pmatrix} = a_3 * b_1 + a_2 * b_2 + a_1 * b_3$$

…….

$$61)PP_{61} = \begin{pmatrix} a_{32}a_{31}a_{30} \\ b_{32}b_{31}b_{30} \end{pmatrix}\begin{matrix} ...a_3a_2a_1 \\ ...b_3b_2b_1 \end{matrix} = a_{32} * b_{30} + a_{31} * b_{31} + a_{30} * b_{32}$$

$$62)PP_{62} = \begin{pmatrix} a_{32}a_{31} \\ b_{32}b_{31} \end{pmatrix}\begin{matrix} a_{30}...a_3a_2a_1 \\ b_{30}...b_3b_2b_1 \end{matrix} = a_{32} * b_{31} + a_{31} * b_{32}$$

$$63)PP_{63} = \begin{pmatrix} a_{32} \\ b_{32} \end{pmatrix}\begin{matrix} a_{31}a_{30}...a_3a_2a_1 \\ b_{31}b_{30}...b_3b_2b_1 \end{matrix} = a_{32} * b_{32}$$

The PP of 1st step is taken as PP_1, that of 2nd step PP_2 and so on, then the final output is the concatenation of the PPs. Output = $PP_{63}PP_{62}PP_{61}$ … $PP_3PP_2PP_1$.

B. 32 x 32 – bit Reversible Vedic Multiplier

A 32 x 32 bit Vedic Multiplier (VM) is formed by four 16 x 16 bit Vedic multipliers. Each of the 16 x 16 bit VM is again formed by four 8 x 8 bit VMs, which in turn is formed by four 4 x 4 bit VMs. Finally, the 4 x 4 bit VM is formed by four 2 x 2 bit VMs. This is as shown in Fig 4.

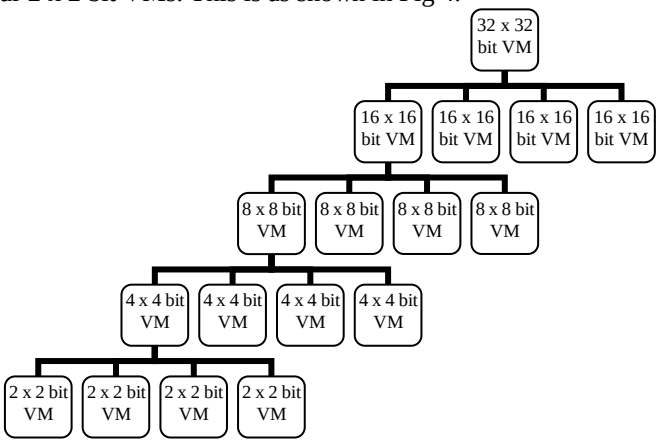

Fig. 4 Hierarchical break-up of 32 x 32 bit Vedic multiplier

The 2 x 2 bit VM has three steps for generating the final output.

$$1)PP_1 = \begin{matrix} a_2 \\ b_2 \end{matrix}\begin{pmatrix} a_1 \\ b_1 \end{pmatrix} = a_1 * b_1$$

$$2)PP_2 = \begin{pmatrix} a_2a_1 \\ b_2b_1 \end{pmatrix} = a_2 * b_1 + a_1 * b_2$$

$$3)PP_3 = \begin{pmatrix} a_2 \\ b_2 \end{pmatrix}\begin{matrix} a_1 \\ b_1 \end{matrix} = a_2 * b_2$$

Each of these three steps have single bit multiplication and these multiplications are performed using Toffoli reversible gates. This makes the 2 x 2 – bit VM reversible in nature.

The 32 x 32 – bit VM can now be termed as Reversible Vedic Multiplier (RVM) as the 2 x 2 – bit RVM forms its basic unit. The introduction of the reversible logic gates here has greatly reduced the power consumption of the multiplier.

V. RESULTS AND DISCUSSION

Both the designed VMs uses the parallel approach of UT sutra to generate the PPs. Thus the PPs are got in a pipelined manner making the multipliers faster than conventional multipliers. These multipliers can also be called Pipelined Vedic multipliers. Further the use of Toffoli reversible gates, in the second design, has made the multiplier utilize lower power than the first design. Table II shows comparison of the Look-up Tables (LUT) and slices of the FPGA used by the 1st VM design and 2nd RVM design. The number of LUTs and slices used by RVM has decreased by 21.2% and 21.6% respectively, when compared with the 1st design, and so it requires lesser power.

Table II. Device utilization comparison of both designs

Type of multiplier	LUTs	Slices
VM (1st design)	2814	1556
RVM (2nd design)	2216	1220

Fig 5. gives the comparison of the delay in output generation by both the designs. The 1st design, gives a delay of 24.84 ns while the 2nd design, shows delay of 24.56 ns. Thus it can be observed that the RVM has lower power consumption and better throughput, when compared with the VM.

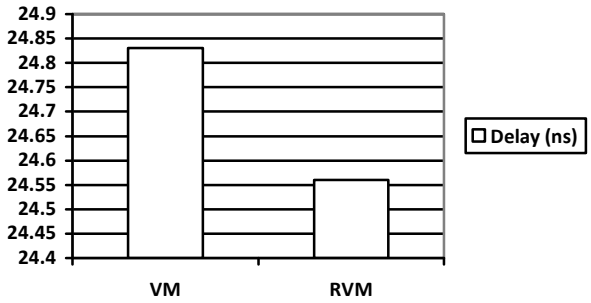

Fig. 5 Delay comparison between the designed 32 x 32 bit VMs

VI. CONCLUSION

In this paper, two models of 32 x 32 bit multipliers have been designed and implemented. Both the designs use the UT sutra of Vedic mathematics for multiplication of two 32 bit inputs, generating a 64 bit output. The 2nd design also incorporates the reversible logic, through the use of Toffoli reversible gates, along with the UT sutra for performing the multiplication. Although the 1st design gives low power consumption, it is observed that, introduction of the reversible logic gates has further reduced the power consumption of the multiplier. The 2nd design is thus more optimized in terms of power and has better throughput, when compared to the 1st design using only the UT sutra.

REFERENCES

1. A. P. Chavan, R. Verma and N. S. Bhat, "High Speed 32-bit Vedic Multiplier for DSP Applications, " *International Journal of Computer Applications*, vol. 135, no. 7, Feb. 2016, pp. 35-38
2. P. Mehta and D. Gawali, "Conventional versus Vedic mathematical method for Hardware implementation of a multiplier"*2009 International Conference on Advances in Computing, Control, and Telecommunication Technologies*, Trivandrum, Kerala, 2009, pp. 640-642.
3. L. Sriraman, K. S. Kumar and T. N. Prabakar, "Design and FPGA implementation of binary squarer using Vedic mathematics," *2013 Fourth International Conference on Computing, Communications and Networking Technologies (ICCCNT)*, Tiruchengode, 2013, pp. 1-5.
4. A. P. Nicholas, K. R. Williams and J. Pickles, *Vertically and Crosswise: Applications of the Vedic Mathematics Sutra*, Motilal Banarsidass Publishers, 2003, ch 1.
5. M. Ramalatha, K. D. Dayalan, P. Dharani and S. D. Priya, "High speed energy efficient ALU design using Vedic multiplication techniques," *2009 International Conference on Advances in Computational Tools for Engineering Applications*, Zouk Mosbeh, 2009, pp. 600-603.
6. A. E. Vijayan, A. John and D. Sen, "Efficient implementation of 8-bit vedic multipliers for image processing application," *2014 International Conference on Contemporary Computing and Informatics (IC3I)*, Mysore, 2014, pp. 544-552.
7. V. Kunchigi, L. Kulkarni and S. Kulkarni, "High speed and area efficient vedic multiplier," *2012 International Conference on Devices, Circuits and Systems (ICDCS)*, Coimbatore, 2012, pp. 360-364.
8. J. V. Suman, "Design and Performance Evaluation of Hybrid Vedic Multipliers, " *International Journal of Innovative Technology and Exploring Engineering*, vol. 8, issue. 8, June 2019, pp. 1622-1626
9. S. Prema, Ramanan S. V, R. Arun Sekar and R. Cristin, "High Performance Reversible Vedic Multiplier Using Cadence 45nm Technology," *International Journal of Innovative Technology and Exploring Engineering*, vol. 8, issue. 7, May 2019, pp. 47-52
10. A. K. Thakre, S. S. Chiwande and S. D. Chafale, "Design of low power multiplier using reversible logic gate," *2014 International Conference on Green Computing Communication and Electrical Engineering (ICGCCEE)*, Coimbatore, 2014, pp. 1-6.
11. N. Abdessaied and R. Drechsler, *Reversible and Quantum Circuits : Optimization and Complexity Analysis*, Springer International Publishing, 2016, ch. 2.
12. A. Eshack and S. Krishnakumar, "Implementation of Pipelined Low Power Vedic Multiplier," *2018 2nd International Conference on Trends in Electronics and Informatics (ICOEI)*, Tirunelveli, India, 2018, pp. 171-174.
13. F. Naderpour and A. Vafaei, "Reversible multipliers: Decreasing the depth of the circuit," *2008 International Conference on Electrical and Computer Engineering*, Dhaka, 2008, pp. 306-310.
14. K. Morita, "Reversible Computing Systems, Logic Circuits, and Cellular Automata," *2012 Third International Conference on Networking and Computing*, Okinawa, 2012, pp. 1-8.
15. U. Kumar, L. Sahu and U. Sharma, "Performance evaluation of reversible logic gates," *2016 International Conference on ICT in Business Industry & Government (ICTBIG)*, Indore, 2016, pp. 1-4.
16. A. Eshack and S. Krishnakumar, "Reversible Logic in Pipelined Low Power Vedic Multiplier," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 16, no. 3, Dec 2019 (to be published).

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