A 10-bit 150MS/s Pipelined ADC with 2.5bit Gain Stage for High Frequency Applications

G.Kirubakaran, D.Dineshkumar, R.Varun Prakash

Abstract*: This paper proposes a 10-bit pipelined Analog to Digital Converter (ADC) which incorporates various techniques for lesser power and higher performance. The proposed method reduces the computational burden while comparing to the modified Monte-Carlo (MC) method. Pipelined ADC has N number of stages, it has higher resolution and higher frequency of conversion while comparing to other ADCs. The proposed ADC employs five 2.5bit gain stages; instead of 1.5bit gain stages for high accuracy. This method is implemented in the Tanner Software with the Generic 250nm library at a maximum power supply of 5V. The maximum frequency attained is 150MHz; and the ADC exhibits a SNR of 61.96dB. It also attains a 10bits as effective number of bits at the maximum sampling rate.

***Index Terms*: Evolutionary algorithm, Monte-Carlo (MC), Pipelined ADC, 2.5bit gain stage, 10-bit ADC**

I. INTRODUCTION

Data converters has been significantly increased because of technology scaling in VLSI industries [5]. Technology scaling impacts the variability in process which results in random parameters [6]. The performance of converters would be affected because of the process variation; which is mainly due to the advancement of technologies. In high speed pipelined data converters, the performance of analog blocks needs more significance [7]. Based on the pipelined ADC concepts, we are capable of designing a pipelined ADC in a very short design time. Many researchers have proposed methods to design a high performance ADC. [8] has proposed a statistical ADC. The performance of the full ADC using a uniformly distributed analog input for finding the RMS error of the resulting code. This error is larger than the specified threshold, due to the probability of error in front end. [9] proposed a 14-bit pipelined ADC with SFDR of 100-dB. By applying a stage scaling algorithm at the architectural level and a device sharing technique at the circuit level, the ADC was optimized for low power application.

[10] proposed a 12-bit low power pipelined ADC with a SFDR of 82 dB using split-ADC Calibration. With the help of multiple stage gain and a precise calibration of non-linearity, the ADC attains fair results. [12] proposed a transistor level synthesis of pipelined ADC. The proposed tool is capable of synthesizing the pipelined ADC in less design time, approximately in minutes, and also obtain a great agreement between switch and behavioral level simulations. [7] proposed a simultaneous optimization of analog circuits. This approach is used to improve lifetime of the ADC. A blended approach is used for optimizing the fresh and lifetime yields at the same time. [2] proposed a yield-aware pareto front extraction. This algorithm minimizes the clock errors in the recovery path. [13] proposed a low power 13-bit pipelined ADC. It reduces power dissipation. [14] proposed a 10-bit low power pipelined ADC. It was provided with a 3.3V power supply and observed 0.6 LSB OF INL. [15] proposed a design of steering DAC. It was provided with transistor level synthesis. It elaborately defines the design points under reliability both for short and long time. [4] proposed an accurate and an efficient yield optimization technique.

The proposed approach is implemented on a 10-bit pipelined ADC, for greater accuracy and performance. In this method, optimization is done at system level. The performance parameters of pipelined ADC mainly depend on the sub-block ADC design, which affects the overall power and time for design [12]. The proposed ADC is based on a novel high performance algorithm. The ADC optimization hasn't been attained at the system level yet. ([1]-[4]).

II. PROPOSED WORK

A. Pipelined ADC

The pipelined ADC is a data converter with X steps. Here, each step is converted into a single bit. It consists of X stages which are in series with each other. Each stage contains a sample and hold circuit, a comparator, an amplifier and also a summer. The pipelined ADC is capable of attaining higher resolutions without sacrificing the speed. It also gives high throughput altogether. For each and every clock pulse, one conversion will take place. The residue of first stage will be carried to the second stage and so on. Similarly, each and every stage has some residue from previous stages. This improves the conversion time. The drawback is the initial delay incurred by the first clock cycle before the application of the first step. If there is an error in one stage, that will be carried to the next stage. Hence it will affect the accuracy. Care should be taken when considering several stages.

B. Proposed Pipelined ADC Architecture

The block diagram of the proposed 10-bit pipelined ADC was shown in Fig. 1. The architecture has a S/H block at the beginning, followed by four 2.5 gain stages and eventually a flash ADC. Sample and hold converts the analog signals into digital signals. The function of the S/H circuit is to take the samples and hold the samples until the ADC processes the information. In order to sample the input signal, the switch will be connected so that the capacitor gets charged or discharged so that the input voltage gets proportional to

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the voltage across the capacitor. In hold mode the switch gets disconnected and the capacitor gets discharged.

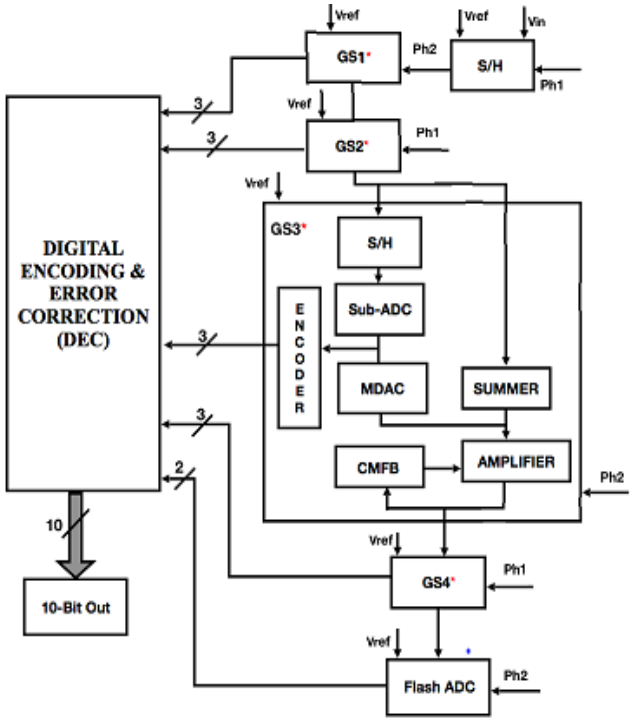

Figure 1. Simplified block diagram of pipelined ADC.

The gain stage consists of a sub-ADC block with 3-bit resolution shown in fig.2, and a multiplying DAC (abbreviated for simplicity as MDAC). The output of the multiplying DAC is the product of the reference voltage and the code (as 0s or 1s). DAC needs a fixed reference voltage but MDAC accepts different reference voltage. The full scale output of the MDAC is determined by Vref. The output is the current signal rather than voltage signal.

The sub-ADC consists of comparators and amplifiers. Fig. 2(a) shows the schematic of the 2.5 bit multiplying DAC (MDAC) with two stage cascade amplifier. The sampled input Vin is finally obtained by digital error correction block (DEC). The input voltage Vref and Vin is fed into the S/H circuit. The output thus obtained from the S/H circuit along with Vref is applied to the 2.5-bit gain stage1. Each gain stage has 2 effective bit (i.e., 2-2-2-2-2 configuration).

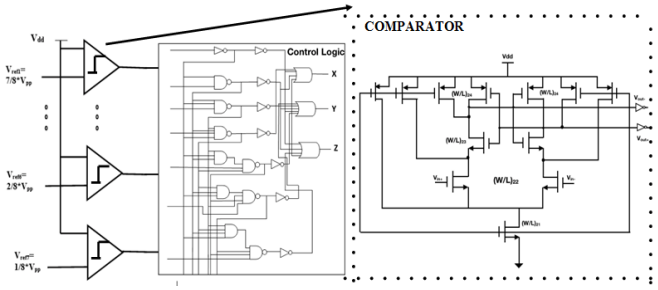

Figure 2. Sub ADC.

The output from the gain stage1 is of 3 bits and it is given to the gain stage2 as input. Each and every Gain stage consists of an S/H circuit, followed by MDAC, and a flash ADC; also a 2-bit encoder. The output of the sample and hold circuit is given to the flash ADC. Flash ADC is the fastest of all type of ADC. The reference voltage gets divided and each value is fed to the comparators. The reference voltage and the input voltage gets compared. The conversion time of flash ADC is 100ns or even lesser.

Hence, the output signal from the flash ADC is given to the 2-bit encoder and also to the MDAC. The encoder has 2n input lines and n output lines. We have used 4X2 encoder. The gain stage2 will give 3-bit output and it is fed to the gain stage3 along with Vref. It also generates 3-bit output and further it is given to the gain stage4. The output of the gain stage4 along with Vref is given to the flash ADC. The flash ADC will give 2-bit output. The output of 14 bit is fed to the digital encoding and error correction block (DEC). Finally, the output of the DEC block is 10 bit.

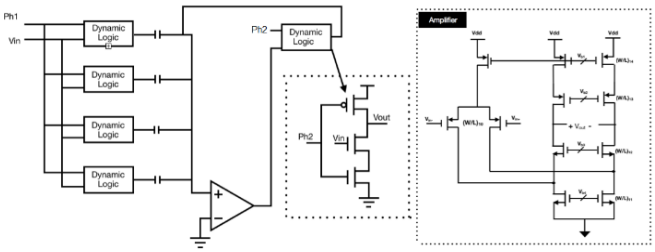

Figure 3. Multiplying DAC

III. RESULTS AND DISCUSSIONS

To implement the given ADC, the Tanner EDA tools have been utilized. The library chosen for the proposed architecture was Generic 250nm Standard Library which follows [16]. Fig.4 shows the 2.5-bit Multiplying DAC implemented in the Tanner S-Edit tool. Here, we use the dynamic CMOS logic for switches, whereas phase 1 and phase 2 are the two non-overlapping clock pulses. A DC supply of 5V is used across the devices used in the architecture. The output hence taken from the amplifier is fed back as the input to the input through the dynamic logic using the phase 2 clock. The characteristics of the MDAC is shown in fig.5. By using MDAC, the digital output is converted into an intermediate analog output.

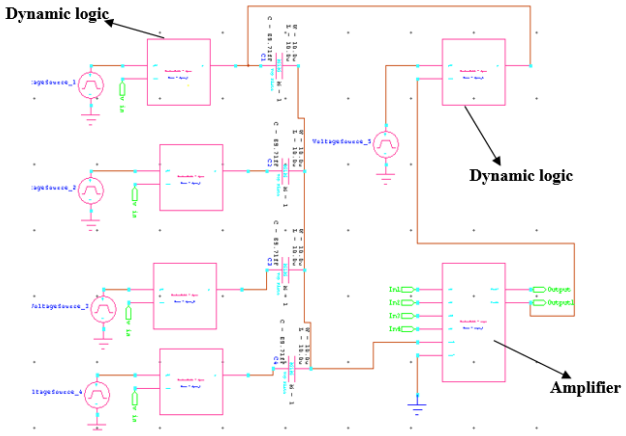

Figure 4. Schematic of an MDAC

The CMOS schematic of Sub-ADC is shown in fig.6. The comparators in the sub-ADC have two inputs; one of which is the reference voltage of 5V and the other inputs are the scaled version of input.

The output of each comparator is given to the control logic which has 6 inputs. The Sub-ADC output is shown in the fig.7. For various inputs, the transient analysis has been taken.

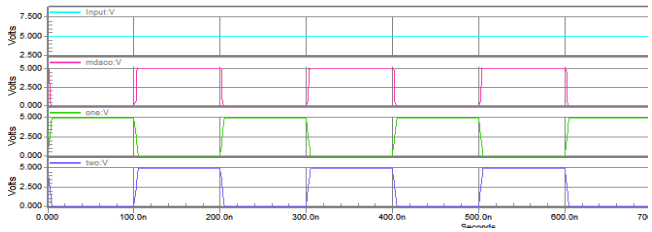

Figure.5 Transient analysis of an MDAC

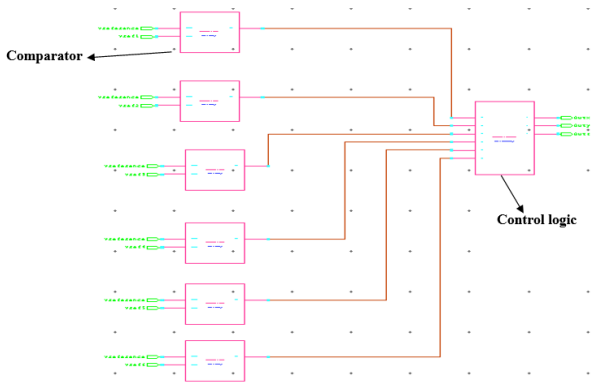

Figure.6 Schematic of the Sub-ADC.

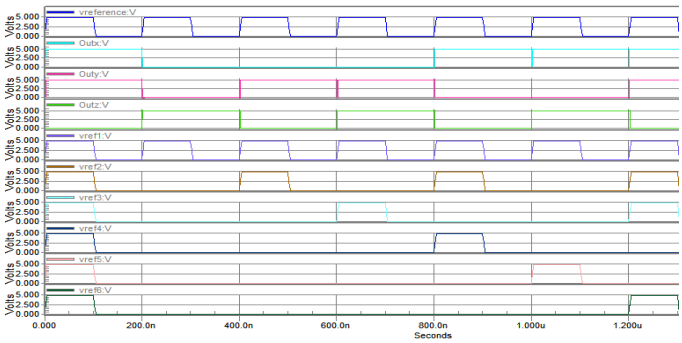

Figure.7 Transient analysis of the Sub ADC.

The gain stage consists of both MDAC and Sub-ADC. The CMOS schematic of a single 2.5-bit gain stage is shown fig.8. The transient analysis for a single gain stage is shown in fig.9.

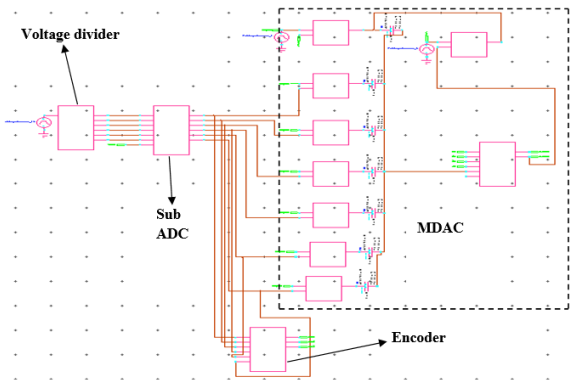

Figure.8 Schematic of a single gain stage.

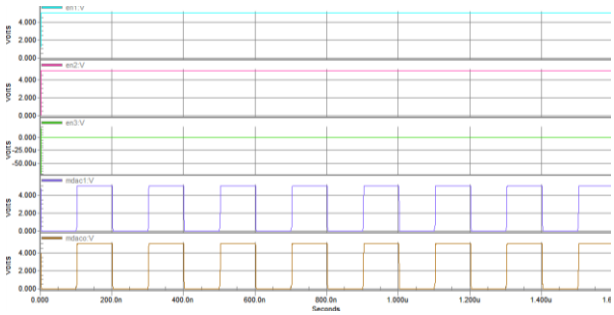

Figure.9 Transient analysis of a single gain stage.

The overall schematic of proposed pipelined ADC is shown in fig.10. The schematic consists of 4 gain stages connected in series with each other. Each gain stages gives 3-bit output; thus cumulatively, all the gain stages produce 12 bits and another 2 bits are extracted from the flash ADC. And now the 14-bit digital code is sent to the time alignment and error correction block to get converted into a 10-bit digital output. The transient analysis of the proposed pipelined ADC is shown in fig.11.

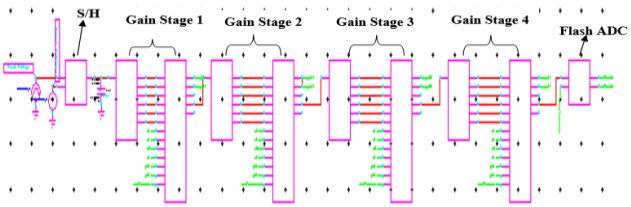

Figure.10 Schematic of the proposed pipelined ADC.

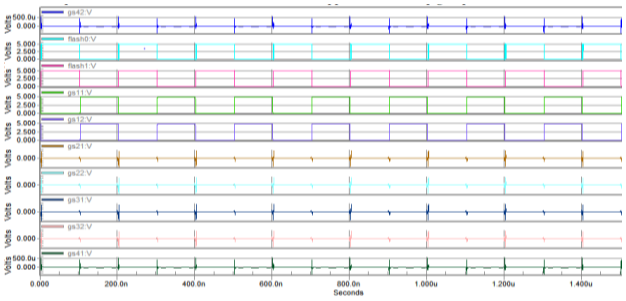

Figure.11 Transient analysis of pipelined ADC.

IV. COMPARISON OF RESULTS

The Table 1 shows the performance comparisons of the proposed ADC with the previous ones. As the technology node we work upon is larger, it impacts the DNL and INL of the device. Though, the lower range of DNL of the proposed work and the work of [11] are comparable. The maximum frequency attainable is 150MHZ which can be used for various high frequency applications such as medical imaging, WLAN, low light photography etc.; The Signal to Noise Ratio (SNR) attained by our ADC is better than the work proposed by [11], which is superior considering the technology node we have opted. Comparing the previous works, the proposed work exhibits an Effective Number of Bits of 10 bits out of its 10-bit resolution, which is again a torchbearer of our

work. The Spurious Free Dynamic Range (SFDR) of the proposed ADC is also relatively comparable to other works which ensures that our ADC is capable of differentiating wide range of analog inputs. The SNR of the proposed work is nearly approaching the SFDR and SNR of the work proposed in [10]

Table 1. Performance Comparison of Various Works with the Proposed Work

Performance Parameters	[10]	[11]	Proposed Work
Technology Node	40nm	130nm	250nm
DNL	+0.16 to +0.21LSB	+0.83 to -0.47 LSB	+1.3 to +0.36LSB
INL	+1.4 to +1.23LSB	+ 1.05 to 0.7 LSB	+1.93 to +0.5LSB
Resolution	12 bit	10 bit	10 bit
Supply	1V	1.2V	5V
Maximum Frequency	195MHz	200MHz	150MHz
SNR	64.8dB	56.5dB	61.96dB
SFDR	82dB	71.8dB	65.48dB
ENOB	10.5bits	9.1bits	10bits

V. CONCLUSION

This paper presented a design of an energy efficient and high performance ADC. This work is implemented on a 10-bit pipelined ADC in a 0.13µm CMOS process and the frequency is of 150MHz.The ADC is a uni-polar ADC and the input range is of 0V to 5V. The resolution of the pipelined ADC is 10 bit. Since it is a 10-bit ADC, 210 we get 1024 combinations. For a 10-bit ADC the resolution will be 4.88mV. To calculate the Differential Non-Linearity (DNL) of the ADC, we have achieved the LSB as 977µV/bits. The DNL is achieved as +1.3LSB to +0.36LSB. The Integral Non-Linearity (INL) is achieved as +1.93LSB to +0.50LSB. The conversion time of the ADC is 6.66ns. The Signal to Noise Ratio (SNR) is achieved as 61.96dB and the Effective Number of Bits (ENOB) is measured as 10 bits.

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