Implementation of Low Power Memory on FPGA

Kshitij Wahurwagh, Shruti Danve

Abstract*: Clock gating is a prominent and an efficacious methodology adopted to decrease the dynamic power (clock power) utilization in complementary metal oxide semiconductor (CMOS) based circuits. The sole intent of gating a clock signal is to minimize its switching activity and thereby reduce significant amount of power utilization of the clock signal. Memories or storage elements are the integral part of the complex designs used in the modern day devices enabling storage of exhaustive and crucial values being processed. In this paper, we present the design and implementation of Random Access Memory (RAM) with reduced power consumption using clock gating technique on a Field Programmable Gate Array (FPGA). These memory elements can be either of synchronous or asynchronous nature. The memories discussed in the proposed work are synchronous in nature and hence reading and writing operations take place on the positive or rising edge of the clock. A gating logic is applied to lessen the superfluous transitions of the clock signal propagating along the clock network of the circuit. The target device (FPGA) for this work is Xilinx Spartan 6 and the design tool is Xilinx ISE 14.7 with the memories being modelled in Verilog HDL and simulation outputs shown in ISim.

Index Terms*: Clock gating, dynamic power, power consumption, Random Access Memory (RAM.)

I. INTRODUCTION

Modern portable multimedia and electronic gadgets which are indispensible part of the contemporary lifestyle, have witnessed an exponential growth lately. Battery being the source of power for these devices, longer battery life has become a crucial aspect in the design of these gadgets. Consequently low power designs have drawn a lot of interest from the researchers to aid the problem of heavy power consumption of these circuits. In majority of such products, a notable amount of the entire circuit is occupied by memory or storage elements. Such memories are required for the temporary storage of signal values which may require further processing or for the purpose of displaying. Various types of memories, each having its dedicated function, associated with the circuits are read only memory ROM (non volatile), Static RAM, Dynamic RAM, and flash memory. Most common circuits today make use of control logic based static random access memory (SRAM) to implement the delay buffers [4]. In the proposed implementation, we are using dual port RAM and single port RAM to illustrate the power consumption reduction using clock gating technique.

The power dissipation of a CMOS circuit can be broadly attributed to two sources: Static power (P_{static}) and Dynamic power ($P_{dynamic}$). The aggregate power consumption of the circuit is a result of the sum of this static and dynamic power. Static power contributes to the overall power usage even when a circuit is not switching [11]. Subthreshold, gate, junction leakage currents and contention currents are the sources which contribute to the circuit's static current and power. [11] The transitional activities at the input and output nodes of the circuit are responsible for the dynamic power consumption. The dynamic power required for the charging and discharging of the output node capacitances is termed as the capacitive load power (P_{cap}). Transient power ($P_{transient}$) is required to change the state of signal form high (1) to low (0) or from low (0) to high (1). The aggregate dynamic power of a CMOS circuit can be expressed as the sum of its transient power ($P_{transient}$) and the power consumed by its capacitive loads (P_{cap}).

$$P_{total} = P_{static} + P_{dynamic} \quad (1)$$

$$P_{dynamic} = P_{cap} + P_{transient} \quad (2)$$

$$P_{dynamic} = \alpha (C_L + C) V_{dd}^2 f \quad (3)$$

Where C is the internal capacitance of the gate; C_L is the load capacitance; α is the activity factor (switching activity) and f is the clock frequency. The probability of a circuit node switching its state from one to another (0 to 1 and vice versa) is termed as its activity factor (α). The activity factor of a clock signal is α = 1 due to the two state transitions occurring every cycle (rising and falling). Most data transition only once each cycle and hence has a maximum activity factor of 0.5 [11]. So, in this manner if we reduce the switching activity of the clock, a significant amount of power consumption can be reduced, which is feasible with the use of clock gating technique.

II. CLOCK GATING

Clock gating proves to be a simple and potent technique to implement at the Register Transfer Level (RTL) which results in substantial decrease in the utilization of clock power, when the objective of the front end design is to minimize the overall power dissipation of the circuit. Its objective is to attenuate the propagation of undesired clock signal transitions to the circuit without altering the functionality. Charging and discharging of the capacitors being the source of dynamic power dissipation, a drop in the signal transitions, switching activities at the node without affecting the functionality of the circuit will result in a significantly reduced power consumption of the circuit. These switching activities are mitigated by suppressing the

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flow of clock signal to the idle blocks of the circuit and consequently saving power by not charging or discharging the capacitive loads [5]. The effect of clock gating technique is more pronounced when applied to the registers which store the same values for multiple clock cycles. The major obstacles in using the clock gating technique are to find the optimal place to deploy it and developing a logic which switches the clock on and off at appropriate times [1]. The most appropriate stage to deploy the clock gating logic is at the Register Transfer level which exhibits a significant impact of the implementation and also gives accurate power estimation of the circuit [1],[12].

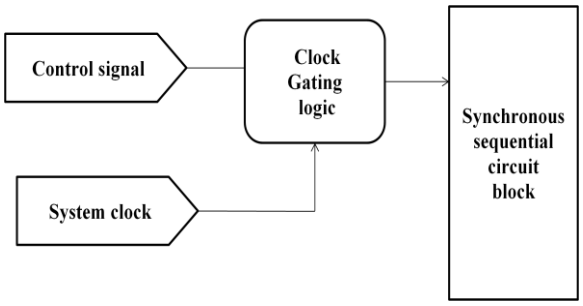

Figure 1: Clock gating logic

Fig.1 represents the principle behind the gating technique in the sense that some logic is inserted between the sequential block and the system clock so that the new clock (gated clock) reaching the module reduces the switching activity of the sequential module while preserving the functionality of the circuit.

There are several methods or ways in which a clock gating technique can be implemented a particular circuit. They are listed below and discussed in the following subsections.

1) Latch less clock gating (AND gate based)
2) Latch based clock gating
3) Multiplexer based clock gating etc.

A) Latch Less Clock Gating (AND Gate)

Fig.2 shows the concept of clock gating using a simple 2-input AND gate. This technique belongs to the latch less clock gating category. In this AND gate method proposed in [1], the flow of clock signal to the logic block is principally controlled by an enable or control signal. The AND gating approach proposed by authors in paper [1] suggests the insertion of a 2-input AND gate between the sequential module and the system clock. One of the inputs to the gate is a system clock and the other input is a control/enable signal to regulate the output of the AND gate which is given to the login block or at the clock input of the circuit.

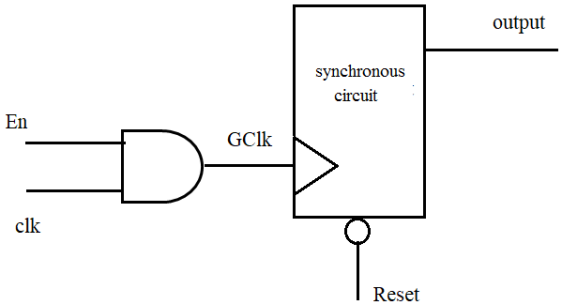

Figure 2: clock gating using AND gate

B) Latch Based Clock Gating

The clock gating technique incorporating a latch as proposed by the authors in [1] makes use of a latch to hold the state of the control signal from the active clock edge until before the next active clock edge. The latch being level sensitive requires the enable or control signal to be high only around the active edge of the clock to facilitate the hold and store of control signal's state throughout the clock pulse, similar to the case in conventional non gated design [7]. Fig.3 shows clock gating logic incorporating a latch.

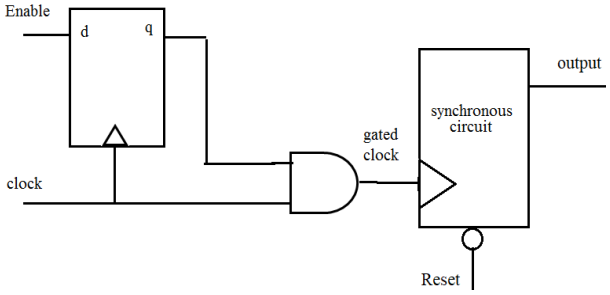

Figure 3: AND Gate Clock Gating Using A Latch

C) Multiplexer (MUX) Based Clock Gating

Fig.4 shows the concept of clock gating with the use of a simple 2 to 1 multiplexer. Multiplexer based clock gating approach as proposed in [7], [1], makes use of an enable signal controlled multiplexer to regulate the closing and opening of a feedback loop around a D-type flip-flop. The drawback associated with this multiplexer (MUX) based gating is greater power dissipation in comparison to other gating techniques [1].

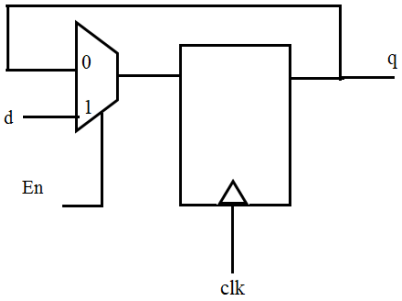

Figure 4: Multiplexer based clock gating

III. IMPLEMENTATION

This section discusses and presents the Register Transfer level (RTL) implementation of the RAM both with and without the employment of clock gating. Here, we are considering RAM of size 64*8 bytes for both single port and dual port implementations. These RAM implementations are simulated and verified in ISim simulator. Fig. 5 shows the implementation of single port RAM without clock gating. First input is 6-bit wide address bus which corresponds to the depth of the RAM (number of memory locations). Next input is 8-bit input data (d_in) that is required to be stored at a particular memory location. The width of the data input determines the word size of the memory (number of bits that can be stored in each memory location). The clock (clk) signal enables synchronous operations allowing both read and write operations to be executed on the positive edge of the clock. Another input associated with RAM is write_en, which exclusively controls

the writing of data onto the memory location. The output port is d_out from which the contents of the memory will be read on the positive edge of the clock. Fig. 6 and Fig. 7 illustrate the detailed register transfer level (RTL) implementaion and the simulation output of the single port RAM, respectively.

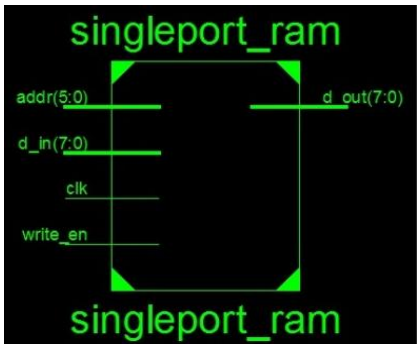

Figure 5: RTL schematic of single-port RAM

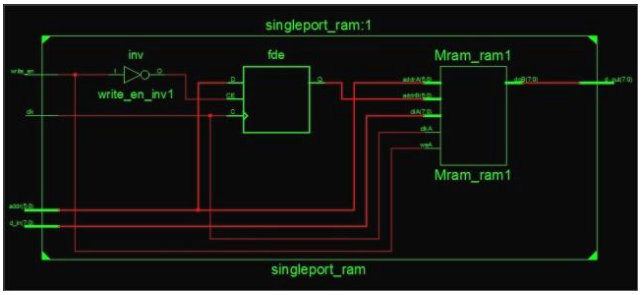

Figure 6: Detailed RTL implementation of single-port RAM

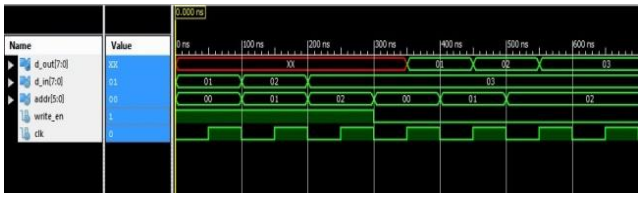

Figure 7: Simulation output of the single-port RAM

The dual port RAM has two ports from which both read and write operations are carried out simultaneously. The two input ports for writing the data in the memory are 8 bits wide. The address bus for both the ports is 6 bits wide. The two output ports are 8 bits wide and the clock and two write enable signals are other inputs for the dual port implementation. Fig. 8 shows the RTL implementation of dual port RAM.

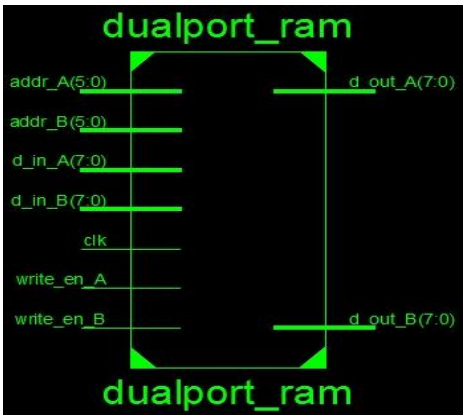

Figure 8: RTL schematic of dual port RAM

The read and write operations for both the ports take place on the rising edge of the clock signal based on the value of write enable signal. The Figs. 9 and 10 show the simulation output and the detailed RTL schematic of the dual-port RAM, respectively.

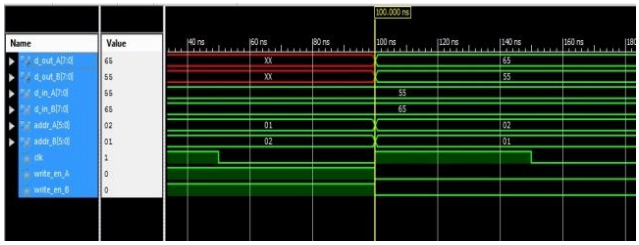

Figure 9:Simulation output of dual port RAM

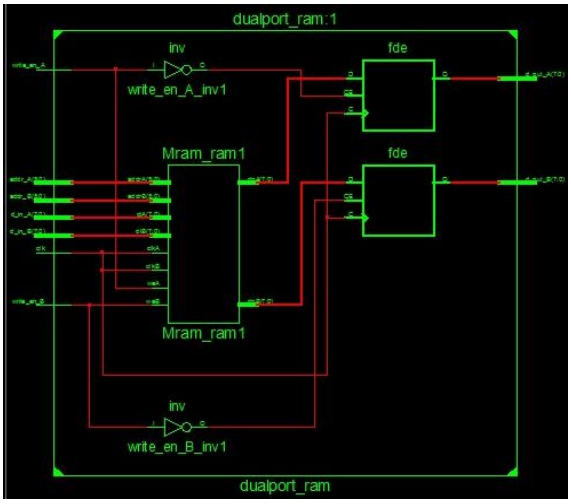

Figure 10: Detailed RTL schematic of dual port RAM

The clock gating technique that we have applied in the memory implementations is latch less AND gate based. This method as discussed previously incorporates an additional control signal to regulate the flow of the clock signal to the circuit. Fig 11 and Fig. 12 show detailed RTL implementation of both single and dual port RAMs with the application of clock gating.

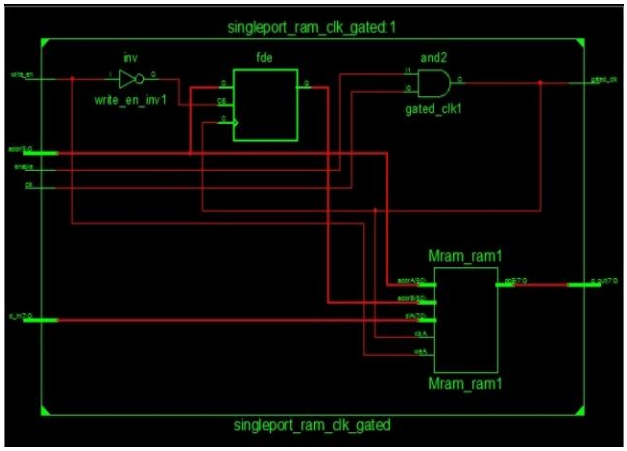

Figure 11: RTL implementation of single port RAM with clock gating

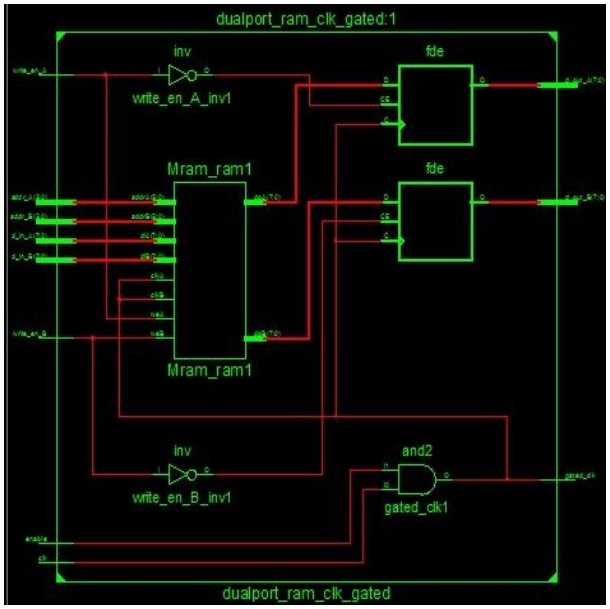

Figure 12: RTL implementation of dual port RAM with clock gating

IV. RESULTS

The difference in the observed power consumption between the two implementations of the memory (with and without clock gating) is presented the figures below. The comparative analysis of the power utilization of the RAMs for different clock frequencies is also presented in Table 1.

Name	Power (W)	Frequency (MHz)	Buffer
Clocks			
clk_BUFGP/IBUFG	0.00167	100.0	NA
clk_BUFGP/BUFG	0.00135	100.0	BUFG
clk_BUFGP/IBUFG	0.00003	100.0	IOB
clk_BUFGP	0.00029	100.0	BUFG
Total	0.00167		
Total By Clock Domain Power (W)	0.00167		

Figure 13(a): Clock power for non gated single-port RAM

Name	Power (W)	Frequency (MHz)	Buffer
Clocks			
gated_clk_OBUF	0.00030	100.0	NA
gated_clk_OBUF	0.00030	100.0	LUT6
Total	0.00030		
Total By Clock Domain Power (W)	0.00030		

Figure 13(b): Clock power for gated single-port RAM

The power consumption estimation is given by the Xilinx XPower Analyzer. The clock frequency for both the RAMs is considered to be 100 MHz. The figures 13(a), 13(b) and 14(a), 14(b) show the clock power consumption with and without clock gating for both single-port and dual-port RAMs, respectively. The clock power consumption for single port RAM has reduced from 0.00167W to 0.00030W and for dual port RAM has reduced from 0.00156W to 0.00037W after the application of clock gating. Clock power consumption for both RAMs with clock frequency 500 MHz is shown in the Table 1.

Name	Power (W)	Frequency (MHz)	Buffer
Clocks			
clk_BUFGP/IBUFG	0.00156	100.0	NA
clk_BUFGP/BUFG	0.00135	100.0	BUFG
clk_BUFGP/IBUFG	0.00003	100.0	IOB
clk_BUFGP	0.00017	100.0	BUFG
Total	0.00156		
Total By Clock Domain Power (W)	0.00156		

Figure 14(a): Clock power for non gated dual-port RAM

Name	Power (W)	Frequency (MHz)	Buffer
Clocks			
gated_clk_OBUF	0.00037	100.0	NA
gated_clk_OBUF	0.00037	100.0	LUT6
Total	0.00037		
Total By Clock Domain Power (W)	0.00037		

Figure 14(b) : Clock power for gated dual-port RAM

Table I: Comparative analysis of clock power of RAM

Power consumption (in Watts)				
Frequency	100 MHz	% power reduction	500 MHz	% power reduction
Single-port (non clock gated)	0.00167	82.03	0.00656	77.28
Single-port (clock gated)	0.00030		0.00149	
Dual-port (non clock gated)	0.00156	76.28	0.00599	69.44
Dual-port (clock gated)	0.00037		0.00183	

V. CONCLUSION

Clock signal in case of conventional non clock gated designs accounts for substantial amount of overall power dissipation of the device. An efficient low power memory implementation has been presented with the deployment of clock gating technique. The clock gating technique applied at the RTL design of the memory has resulted in a significant reduction in the dynamic power consumption. The clocking power for the single port RAM has decreased from 1.67mW to 0.3mW and for dual port memory has reduced from 1.56mW to 0.37mW operating at a frequency of 100MHz. The clock power has reduced by 82.03 % and 76.28% for both single port and dual port RAM, respectively, for 100MHz clock frequency. Thus from results it is evident that clock gating methodology reduces appreciable amount the clock power and consequently the overall power of CMOS circuits and hence can be proactively deployed on larger circuits to significantly reduce the overall power consumption of that circuit.

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