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# Implementation and Utilization of LBIST for 16-bit ALU

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***Abstract*: This paper refers to implementation of Low Power Built-In-Self-Test (LBIST) and its utilization for testing of 16 bit ALU core. Low Power Test Pattern (LP) Generator is programmable and able to produce pseudorandom test patterns. The programmability feature brings in selectiveness in toggling levels of test patterns. This helps to increase the error coverage gradient. This low power pattern generator consists of a pseudo random pattern generator (PSPR) which can be a linear feedback shift register or ring generator. The test pattern generator allows the production of binary sequences by devices with that selected toggling rate is defined as 'Preselected toggling' (PRESTO) activity. In this methodology, controls for operation of generator are selected automatically. Selection of all the controls is made simple and accurate for the tuning. Using this method fault coverage of test pattern generator can be improved as well as pattern count ratio gets improved. The proposed low power test compression method helps to get predictable test patterns. Here preselected toggling based logic BIST is used to get flexible and accurate test patterns hence high quality testing is achieved here with integration of PRESTO and LBIST method.***

***Keywords:** fault coverage, low power BIST, pattern Generator, PRESTO, PSPR*

## I. INTRODUCTION

Adding testability feature to hardware product design DFT (Deign for testability) is used which consist of IC design techniques. For development of reliable and high quality semiconductor products, manufacturing tests DFT is used. It includes low power test pattern generation as well as test compression methods. The Test pattern generator, which comes with preselected toggling level, is proposed to compress the test patterns and hence it helps to reduce the power consumption of the system. Using the PRESTO generator scan chains can be loaded with test patterns of low transition count. This process can effectively reduce the total power consumption. Using PRESTO generator totally automatic selection can be enabled which will help to achieve desired or user defined toggling rates for the test patterns. BIST (Built In Self-Test) is a method of self-testing. This self-testing can be achieved by providing the design of extra hardware features and software features to the integrated circuit. BIST can perform the testing of their function using its own circuit so that there will be no dependency for external testing devices called Automatic Test Equipment (ATE).

DFT or Design for test includes BIST technique. Using Built in self-test testing of chip is done with high speed, more effectively. Also this method is economical and easier. The BIST technology can be applied to any kind of circuit. Hence implementation of BIST technique changes with circuit to which BIST technique is applied. For example consider a DRAM. BIST technique for it consists of addition of extra circuit for the purpose of pattern generation, mode selection, timing and go or no go diagnostic tests.

BIST is used to perform certain special tests which include extra circuit for on chip testing which is able to remove the necessity to have a high end testing equipment. Critical circuits can be tested with BIST even if they don't have direct connection to the external pins. For example, embedded memories used by various devices internally. For the fast operating chips esters are not sufficient for effective testing in such cases BIST is the best solution for the fastest chips.

BIST technology has following advantages:

1. Its cost is less. Hence economical method as it reduces the need of automatic testing equipment.
2. Less test time as parallel testing can be performed for many circuits.
3. Excellent fault coverage, by adding extra test structures in the circuit on the chip.
4. BIST provide easy client support.
5. BIST has capability to perform testing outside the testing environment. BIST allows customer to test their chips before mounting as well as when the chips are present in the application boards.

Memory and logic part of system can be checked with BIST technology. Fault coverage, hardware overhead and test set size and performance overhead are the 4 parameters to be considered while designing BIST circuit. The number of faults detected by the test patterns is known as fault coverage of the test pattern generator. Hardware overhead of system is the additional hardware required for BIST implementation. Test set size should be larger to achieve high fault coverage. Performance overhead is the effect of BIST on the performance of the circuit. BIST causes less maintenance and testing price.

The main aim of paper is to reducing switching of test pattern generator during the scan chain loading process by using the preselected toggling level (PRESTO). The architecture of test pattern generator allows configuration of the scan chains which can be driven by a pseudo random test pattern generator by a constant value which is always set to fix value forgiven period of time. Transition count is kept low for pattern counts. Scan chains are loaded which helps to reduce the power consumption.

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This test pattern generator also enables total automatic selection of its controls so that the final test patterns will have preferred features and toggling rate as specified by the user. Pseudo Random Pattern Generator with toggling level defined beforehand is proposed here. Basic functionality of PRESTO can be modified for additional features as fully operational version of PRESTO and low power de-compressor.

## II. LITERATURE SURVEY

Author proposed a fresh design way of pattern generator. This methodology is usually worked out in connection with on-chip BIST. The design generator includes two elements: a GLFSR earlier suggested as a PSPR and combinational logic combined together to map the results of the PSPR. Using minimum test patterns with only small area overhead, this combinational logic block, intended for a particular COT, can be designed to accomplish nearly 100% single stuck-at fault coverage[1]. Author presented a new low power BIST, TPG method. The method uses window block to monitor transitions and a MUX. Transitions of random patterns generated by LFSR satisfy pseudorandom Gaussian distribution. Transitions of patterns are repressed using k values obtained by distribution of TMW. This method is able to reduce scan transitions upto 60% [2]. Author proposed a hybrid BIST method. This hybrid BIST method is designed to extract the sequence which occurs frequently from the deterministic test patterns. These sequences which are extracted are stored on the chip. Technique used for sequence extraction is cluster analysis. Encoding of deterministic patterns is performed by considering the stored sequences. The hybrid method mostly requires less storage on the chip as well as test data volume is less as compared to other BIST techniques. These conclusions are obtained by conducting experiments on ISCAS-89 benchmark circuit [3]. Author presented architecture for scan based mixed mode BIST. Storage requirements of deterministic patterns relies on 2D compression method, it combines advantages of vertical and horizontal compression techniques. Experimental result shows reduced storage space [4]. Author presented a technique for compression of test vectors which is lossless technique. This method integrates reseeding of linear feedback shift register with statistical coding in a great way. Linear equations solved to encode the test vectors by LFSR seeds. The space got by solving linear equations might be very large. The use of this solution with large space is made to find out the seeds. These seeds can be encoded efficiently by using the statistical codes. Author described both the architectures to implement reseeding of LFSR, with the seed compression technique [5]. Author presented new type of linear feedback shift register (LFSR). It is designed in such a way that it reduces the transition count at input by up to 25% at the CUT, for this purpose it uses technique called bit-swapping. Experiment is conducted on ISCAS'85 and 89 benchmark circuit. An experimental result shows that there is up to 4% of power reduction while test is performed. To achieve power reduction, the proposed technique can be very well combined with the methods proven to be good in power utilization. [6]. A new technique called Random single input change (RSIC) test generation is proposed by Girard. It gives high level of defect coverage for low power BIST. Parallel implementation of BIST is implemented and analyzed for RSIC generator [13]. Author described different functional models of Different fault modeling methods of RM and flash memories are proposed. BIST techniques are explained to reduce the fault [15]. Low power test method is proposed which is compatible for both BIST and test compression. Power reductions can be obtained by using micro-controller which allows lowering toggling rates while injecting data into scan chains, it causes low switching activity. Power dissipation and voltage drop can be reduced [8]. Systems fortified with scan based BIST like STUMPS are analyzed. Highest power consuming nodes and modules are identified. Designs are modified in terms of some gating logic for masking the scan path activity during shifting for consumption [9]. Deterministic logic BIST (DLBIST) method is proposed by author. The DLBIST method integrates pseudo LBIST and external testing performed in deterministic way. In terms of computation, DLBIST is having linear complexity. It has binary decision diagram based memory algorithms. These tests are performed and observed on industrial designs having up to 2M gates [10]. Hybrid weighted approach is formed for test data compression scheme which combines external testing and Built In Logic Test. This method is built on pseudorandom testing. Two methods are given to store the weights efficiently [19].

## III. IMPLEMENTATION OF PRESTOGENERATOR

It consists of n-bit PSPR, which can be a linear feedback shift register or ring generator. The output of PSPR is connected to n-bit hold latches and is controlled by n–bit toggle control register. Output of hold latches is provided to the phase shifter. As long as input of hold latch is enabled, data passes through it i.e. toggle state and when input of hold latch is disabled, data is captured and saved in it. Hence it provides constant value to phase-shifter. This state is hold state. The output of a block phase shifter is acquired by performing XOR operation on the outputs of three different hold latches so that all scan chains stay in low power mode because phase shifter output is driven by only disabled hold latches. Its contents are '0' and '1'. When its value is '1', data is transparent to arrive from PSPR. Its fraction determines the scan switching activity. Reloading of control register is performed once per pattern. Content of extra shift register are used for reloading. Shift registers are inserted with enable signals. These enable signals are created using original pseudo random pattern generator with weights which are programmable. The weight value is determined by four AND gate output. Programmable weights are used to produce probabilistic output. AND gates decide probability of producing '1'. It is 0.5, 0.25, 0.125, 0.625 respectively. OR gate allows selecting probabilities beyond simple powers of 2. Switching register is a 4 bit register used to select level of switching which is user defined. Switching register activates AND gates and selects level of switching. Switching code '0000' is used to turn off the LP functionality. It is detected by 4-input NOR gate provided in the system. While working in weighted random mode, it is made sure that content of control register are statically stable. It is ensured by switching level selector. Stability is checked by considering the amount of 1's it is having. Hence the number of scan chains staying in low power mode will roughly be the same.

The set low power toggling chain will be changing from one test pattern to another. Certain level of toggling will be corresponding to the scan chains. The available toggling granularity may reduce this solution too bristly to be always acceptable, with only 15 different switching codes.

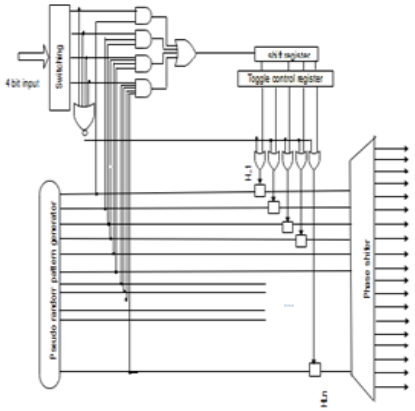


**Fig 1. Block diagram of PRESTO generator**

Switching codes decides probability to inject "1" into shift register. Switching codes and their corresponding probability to inject "1" is given in table number 1 as below.
Algorithm for selecting switching code:

1. For switching code k (k=1,2,3,4….15 ), probability of injecting "1"s in shift register is Pk. P1=0.5, P2=0.25
2. Duration of hold duty cycle is given by hk: hk=tk=1/Pk
3. Number of '1's in control register is given by nk. nk=Pk*n
   Where, n is the size of PRPG.
4. Find an average number of scan chains (ak): 1000 n-bit random combinations having exactly nk, is generated to obtain the number of active scan chains in each case and ak is averaged over 1000 samples.
5. Desired level of toggling is T %. Resultant number of active scan chains: A=(T*S/50)

Where, S is total number of scan chains.
Determine how many extra scan chains should be inactivated.

$$dk=ak-A$$

Let 'L' be the scan chain length. The value dk is converted into no of corresponding cells in active scan chains.

$$dk*L=(ak-A)*L=ak*hk*r$$
$$(hk+tk)*r=L$$
$$r=hk/tk$$
$$r=(ak/A)-1$$

r=number of hold duty cycle.
Ratio r is calculated for each hk and tk value. It is used to find the best matching value between actual r and theoretical value of expression (ak/A)-1.
The hold and toggle codes and their switching values produce a ratio r. The selection of PRESTO parameters is done based on smallest deviation of r from its theoretical value.

Table- I: Switching codes

| Switching code (hex value ) | Switching code | Probability to inject "1" into shift register |
|---|---|---|
| 1 | 0001 | 0.5 |
| 2 | 0010 | 0.25 |
| 3 | 0011 | 0.625 |
| 4 | 0100 | 0.125 |
| 5 | 0101 | 0.5625 |
| 6 | 0110 | 0.34375 |
| 7 | 0111 | 0.671875 |
| 8 | 1000 | 0.0625 |
| 9 | 1001 | 0.53125 |
| A | 1010 | 0.296825 |
| B | 1011 | 0.6484375 |
| C | 1100 | 0.1796875 |
| D | 1101 | 0.58984375 |
| E | 1110 | 0.38476563 |
| F | 1111 | 0.69238281 |

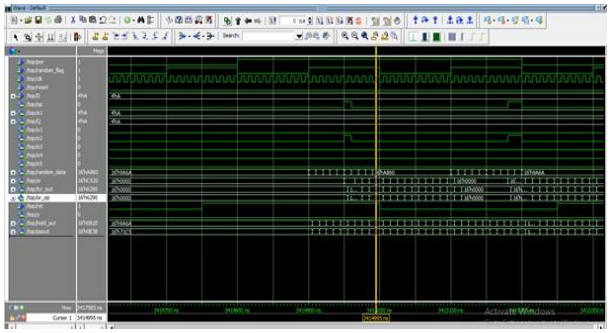

**Fig.2. Simulation results of PRESTO generator**

### *A. Fully operational version of PRESTO*

Higher flexibility can be achieved informing low toggling test patterns by modifying the basic PRESTO architecture. Here shifting period of every test pattern is divided into alternating hold and toggle interval. Tflip-flop is used to move the generator back and forth between two states. If it is 0, It remains in hold state and if it is 1, it is in toggle mode. When T flip flop is having value 1 (i.e. toggle mode), the hold latches are enabled in this state by the control register. Hence test data can be passed from PRPG to the scan chains. Two additional 4 bit registers are used to keep parameters of hold and toggle mode which decides for how much period generator stays in either hold mode or toggle mode. The T flip flop is used to control four multiplexers having 2 inputs each. These multiplexers transfers data from toggle and hold registers. T flip flop selects the control data source that is used in the next pattern to change the generator's function or operation. The input multiplexer observes the toggle register when it is in toggle mode. As the status of weighted logic becomes '1', the flip flop toggles which causes freezing of all hold latches in the previous recorded state. This state continues until weighted logic becomes '1' again. When to terminate or end the hold mode of generator is depend on content of hold register.

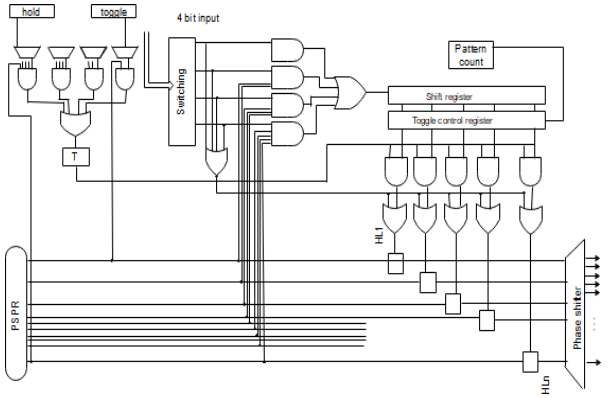


**Fig 3. Block diagram of fully operational version of presto**

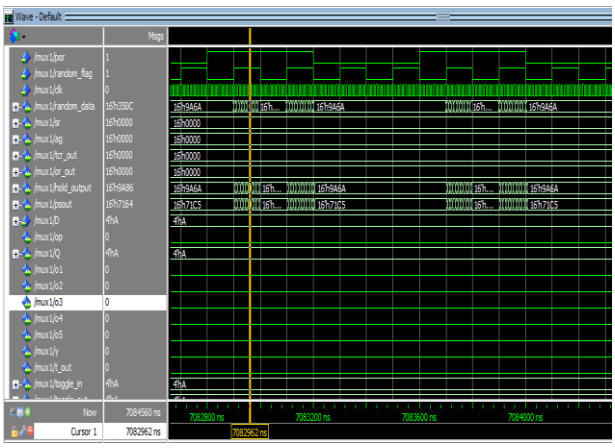

**Fig.4. Simulation results for fully operational version of PRESTO**

*B. LP decompressor*

To achieve test data decompression while conserving unique functionality of the circuit, architecture is modified as shown in the block diagram of LP decompressor. Disabling weighted logic blocks is the basic principal of decompressor. The multiplexer is kept in front of the shift register hence; toggle register's contents can be selected in deterministic manner Toggle and hold register perform preset operation of 4 bit binary down counter which causes determination of duration of toggle and hold phase. Initialization of down counter and T flip-flop is done for every test pattern. The mode of operation of decompressor is depends on the initial value of the Tflip-flop. Primary value of counter is referred as an offset. This offset value determines that mode's duration. Functionality of T flip-flops is same as the low power pseudo random pattern generator.

The external ATE channels which are feeding to the original PRPG are allowed to form a continuous flow of test data decompression sequences in order to achieve dynamic LFS reseeding. The size of pseudo random pattern generator is given. Values of number of scan chains, toggle register, hold register, switching code, the offset and size of phase shifter are given. Based on these values LP decompressor produces deterministic test patterns having toggling level as specified by the user for the corresponding scan chains to remain balanced. The decompression operation is tightly coupled with compression architecture.

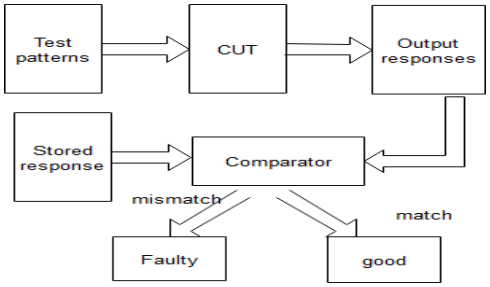


**Fig 5.block diagram of LP decompressor**

*C. Details of Circuit Under Test (CUT)*

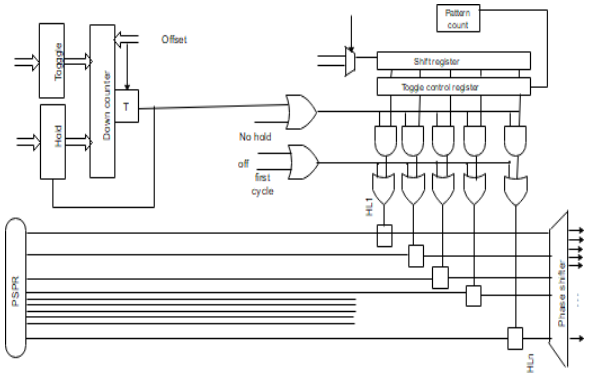


**Fig.6. Circuit under test**

The purpose of test is to detect the Circuit Under Test (CUT) as faulty or fault free. Test signals are applied to the inputs of CUT. Response of output is observed and compared with true responses. There should not be the mismatch between observed response and the stored correct response for the good or fault free circuit. Figure 6 shows the fault detection method. Circuit under test is the 16 bit ALU performing arithmetical and logical operations. It has two 16 bit data inputs and one 4 bit operation selection input and two outputs i.e. carry flag and ALU output. The patterns obtained from preselected toggling generator are given to the ALU circuit as input. Results generated are compared with stored results. Figure 7 shows block diagram of 16 bit ALU. A and B are 16 bit inputs and Result and carry are outputs. 4 bit select input is given to select the operation to be performed by ALU.

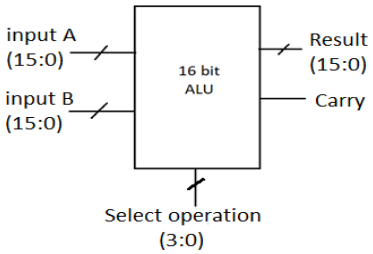


**Fig.7. CUT – 16 bit ALU**

Table-II: ALU select and operation

| ALU select | Operation |
|---|---|
| 0 | Addition |
| 1 | Subtraction |
| 10 | Multiplication |
| 11 | Division |
| 100 | Logical shift left |
| 101 | Logical shift right |
| 110 | Rotate left |
| 111 | Rotate right |
| 1000 | Logical and |
| 1001 | Logical or |
| 1010 | Logical xor |
| 1011 | Logical nor |
| 1100 | Logical nand |
| 1101 | Logical xnor |
| 1110 | Greater comparison |
| 1111 | Equal comparison |

## IV. SIMULATION OF CUT AND PRTPG INTERFACING

16 bit ALU is tested with 16 bit PRESTO Generator. The simulation results are as shown in the Fig. 8. The 16 bit PSPR is interfaced with 16 bit ALU. The test patterns are applied as input to CUT. Results of ALU are compared with stored results to decide whether circuit is faulty or a good one.

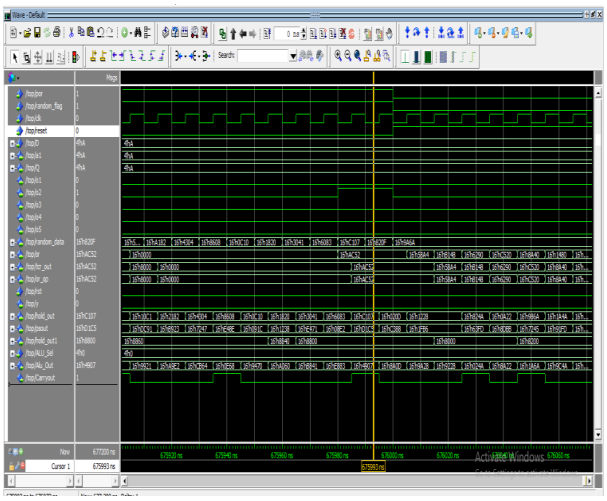

**Fig 8.testing 16 bit ALU with PRESTO circuit**

## V. CONCLUSION AND FUTURE SCOPE

PRESTO is the low power pseudo random test pattern generator. This can produce pseudorandom test patterns with scan shift-in switching activity accurately selected through programming. It includes low power test pattern generation as well as test compression methods. Test pattern generator with preselected toggling level is proposed to compress the test patterns and hence to reduce the power consumption. Patterns having low transition count are loaded by the PRESTO generator to the scan chains. It helps to reduce the power dissipation. These features can be used to control generators, so that the resulting test vectors can produce the desired error coverage faster than conventional pseudorandom patterns while still reducing the rate of displacement to the desired level, or can offer a higher coverage rate if run for comparable time of test. The pattern generator can be tested with sequential and combinational circuits.

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