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Implementation of Low density Parity Check system using Probabilistic Gradient Descent Bit Flipping Decoder

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Abstract— This paper represents the concept of hard decision decoder in which PGDBF is suitable decoder for the basic model of hard-choice decoder as long as low-density parity check code (LDPC) which is increase the error correction. This design introduced dynamic architecture which reduce the capability of random disarrangement of the PGDBF. The design is working on the Short Random Sequence (SRS) that is replica cover on the PGDBF decoding guidelines. In each iteration flipping number of bits these are focusing on improvement in performance and decoding delay. The best SRS is essential to manage the well-known decoding achievement of PGDBF, we introduced two kind of access with same hardware categories, but various LDPC codes are perform different behaviors. In this design we are modifying small hardware decoding unit for obtaining a good decoding explanation for present and further purpose.

Keywords— Gradient-Descent bit flipping, low-density parity-checker, Irregular generator.

I. INTRODUCTION

In the recent years low density parity check performed crucial role in increasing the performance in decoding. The main focus is to improve the error correction or minimise the hardware in decoder. [1] implemented soft-decision iteration decoding with various algorithms which offers better error performance in refer to theoretical coding , but calculation rate is very high. Other way of hard-decision decoders are less-complexity solution. Compared to soft decision iteration decoders hard decision decoders are considered to be performance less with low complexity. One of the decoders such as bit-flipping or A Posterior probability (APP) uses the notes of tenner chart for internal and external data exchange [2], [3].

One of the key algorithms bit flipping reduces the hardware resources without compromising the performance with respect to the other algorithms. Keeping the complexity of the hard ware less number of decoders have introduced. Those are weighted bit flipping, gradient descent bit flipping (GDBF). Comparatively all decoders uses the same theory of passing single bit of data between variable node (EN) and check node (DN).

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Each bit-flipping consist of an energy function or inversion function which performs the bit reversal varies in each decoders. Example In serial bit flipping decoders a single bit is inverted at a time. The energy function for the WBF decoders [4, [6], [7] is design based on DN values and channel output values for the AWGL. Different BF uses different modes based up on the changes acquires different error correction and speeds which very important on performance of LDPC decoders.

Mr. Wadayama [5] proposed one type of PGDBF algorithm. This is collected from the modest system the main aim of this system is gathering nearest matching bits in order to change this bits to elaborate the previous operation. Gradient Descent Bit-Flipping algorithm display the error correcting efficiency is admirable to well-known Bit-flipping algorithms. The experts recommended to integrate a Probalistic aspect in flipping, motivated from PGDBF [2]. But bits are satisfying the gradient action. The alternate selective fraction P0 of them are flipped. This change in algorithm made drastic development in the performance without effecting the error correcting efficiency following soft-Decision data flow Decoders [8].

This work introduced a dynamic hardware (HW) application of the PGDBF decoder which proportionality reduces hardware resources required to implement the alternatively disarrangement of the PGDBF. Binary symmetric channels (BSC) were used over regular LDPC codes so our work is to restrict the decoders those are helping to regular LDPC codes. Recently many cellular standards using irregular LDPC codes, but ordinary LDPC codes are attractive for functional operations; those are fiber-optics communication, satellite communication and storage mediums like pen drives, memory cards [11].

II. CHARACTERIZATION AND INVESTGATION OF THE PGDBF

Parity-check matrix is also called as LDPC code .parity check matrix S size of (P, Q), where P > Q. By represent code word as a vector A = $(a_1, a_2, \ldots a_Q) \in \{0,1\}^Q$ which gratify $Sx^T = 0$. We signify by B = $(b_1, b_2, \ldots b_Q) \in \{0,1\}^Q$ with the help of strengthen possibility α the output bits of binary symmetric channel of the translate code word x has modified.. The graphical chart of a Low Density Parity Check code is a two –part chart called Tenner chart made out of two sorts of hubs, the BNs B_q, q= 1, . . . , Q and the DNs c_Q, q = 1, . . . , P. In the Tanner chart, an e_q is associated with a DN c_p if S (p, q) = 1.

Let us additionally mean $Q\ (e_n)$ the arrangement of DNs associated with e_q, with an association degree d_{e_q}= |$Q\ (e_q)$|, and indicate Q (D_p) the arrangement of ENs associated with the DN D_p, with an association degree d_{c_m}= |$N\ \ (c_m)$|At the point when,

All LDPC codes are general codes; all these network degrees are equivalent for all the nodes. i.e., d_{d_p} =d_d , ∀m and d_{e_q}= d_e, ∀n. in this design we are mainly focus on general Quasi-Cyclic LDPC codes. The Quasi-Cyclic LDPC codes is getting from special representation of a little base network S_B is increased by restoration each vertex in S_B by a circulate change of fundamental corner to corner Z × Z network, so as to get the absolute LDPC structure S. In most of the practical applications we are suggested to QC_LDPC codes because of their extraordinary user and hardware friendly type, a few models [14] [15].Even though we are applying on irregular LDPC codes ,the regular LDPC codes are also suitable for regular bit flipping decoders, in this design to standard d_e = 3 and d_e = 4 LDPC codes.

For each and every decoding iteration, variable node value will be changed based on iterative update method this is defined as BF decoder. In j[th] iteration the value of En is $E_n^{(J)}$. The binary value of DN d_q $is\ D_p^{(k)}$ at j-th iteration, it denotes whether the m[th] parity check condition is accurate or not. Once the total looping's It_{max} is attained Bit-flipping process is stopped when each and every DN values are fulfilled. The DN computation in BF calculations can be expressed as

$$c_m^{(k)} = \underset{v_{n\epsilon N(c_m)}}{\oplus} v_n^{(k)} \qquad (1)$$

XOR (exclusive-OR) indicates bitwise operation. The iteration (N-th) En in the valuation of sin would become a guideline for the use of information Satisfiability renewed in the near DN N (e_q) there is, or modify the estimation $e_q^{(J)}$. the base of GDBF estimation is to say, the work is the conversion of the vital faculty or ability is said to be characterized to the DN so complement one another, to decide what to use, and honour, $e_q^{(J)}$. Might not be, or to be able to be changed. The first is planned for GDBF AWGN Channel [5].

And we needed to have a vitality as in (2), in which the timber γn prospect ratio (PR) AWGN got from the channel mode.

$$\Lambda_{v_n}^{(k)} = \left(1 - 2v_n^{(k)}\right)\gamma_n + \sum_{c_m \epsilon N(v_n)} (1 - 2c_m^{(k)}) \qquad (2)$$

The GDBF on the AWGN medium, the vitality work is genuine esteemed, comparing with the least reliability to corresponding bit. Both modes are designed for the bifurcation rule to emphasize k: either a solitary piece that has the least vitality activity is rotated or a bits collection that have a lesser vitality work than a predefined edge are rotated. The BSC channel, vitality capacity can be adjusted on condition of attendance.

$$E_{v_n}^{(k)} = v_n^{(k)} \oplus y_n + \sum_{c_m \epsilon N(v_n)} c_m^{(k)} \qquad (3)$$

In this situation, the vitality work is number esteemed, changes from 0 to (d_{e_q} + 1), and the bits which have the most extreme esteem $E_{max}^{(J)} = max_q(E_{e_q}^{(J)})$are flipped. Because of the whole number portrayal of the vitality work, numerous bits are likely to have the most extreme vitality, prompting the various flips mode.

Give us a chance to utilize a pointer variable to demonstrate the DNs which have the greatest vitality at cycle J, i.e., $I_q^{(J)} = 1$on the off chance that $E_{e_q}^{(J)} = E_{max}^{(J)}$ and $I_q^{(J)} = 0$ generally. But frankly to say all flipped Bits are shows negative impact on GDBF.

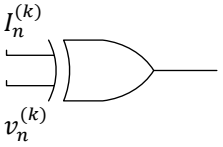

Fig: 1 GDBF

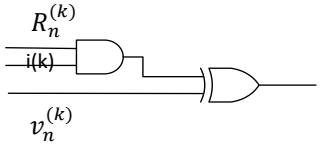

Fig: 2 PGDBF

:$I_n^{(k)}$=1 if $E_n^{(k)} = E_{max}^{(k)}$ Else $I_n^{(k)} = 0$

$I_n^{(k)}$=1 if $E_n^{(k)} = E_{max}^{(k)}$ Else $I_n^{(k)} = 0$

$R_n^{(k)} = 1\ with\ probability\ of\ po$

PGDBF algorithm shown below

Initializing J=0, $e_q^{(0)} \leftarrow b_q,\ q = 1, \ldots\ldots, Q.$

Z= S $v^{(0)^T}$ mod 2

While z≠ 0 $and\ J\ \leq It_{max}$ do

Make $R_q^{(J)}$,q=1,…… Q, fromβ (p0).

Compute $E_{e_q}^{(J)}, q = 1, \ldots, Q$ $E_{max}^{(J)} = max_q(E_{e_q}^{(J)})$

For q=1… Q. do

If $E_{e_q}^{(J)} = E_{max}^{(J)}$ and $R_n^{(J)} = 1$ then

$$e_q^{(J+1)} = e_q^{(J)} \oplus 1$$

End if

End for

Z= S $e^{(J+1)^T}$mod 2

J=j+1

End while

Output: $e^{(J)}$

The PGDBF calculation is shown in Algorithm 1

To evade this encounter , the experts planned the PGDBF calculation, where rather than flipping every one of the bits with greatest vitality work admire, just modified all irregular part of bits .For every pre-specify value $p_q^{(J)}$ An irregular division is fixed this is totally different for each DN and every emphasis. For all iterations and DNs the value of $p_q^{(J)}$ is constant, represent Po ∈ [0, 1].We indicate the irregular sign (RS) succession at the J-th emphasis by $R^{(J)}$ = $\{R_q^{(J)}\ |1 \leq q \leq Q\}$ in which the arbitrary sign $R_q^{(J)}$is activated correspondingly to DN n[th]. Above figures indicates the variation between GDBF and PGDBF . When XOR is equal to one (=1), value of DN $d_q^{(j)}$ at iteration j modified, this entire thing can be done in GDBF. If $I_q^{(J)}$ = 1 and $R_q^{(j)}$ = 1 both are fulfilled the value of VN $d_q^{(j)}$is modified.

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III. ARCHITECTURE OF THE PROPOSED SYSTEM

A. PGDBF ARCITECTURE

The Universal design of the PGDBF decoder is shown in Fig 3. In this design we are adding one additional block .this block generate the random Signal $R^{(j)}$. First we are discussing about decoders in this design how those decoders are represent in algorithm 1 working based on PGDBF decoder. We concentrate in this design on the BSC channel, both the registers exhibits to two back to back D-Flip Flops are stock the noisy code word y and the predicted code word at the present cycle $e^{(j)}$. And talking about the decoder, the signal init generate the replica of y into$v^{(o)}$. The Connection Network Units figure out the equality of their nearby bits in $e^{(j)}$, after a initial connection network unit run properly. The DN values are driven by second connection to the energy computation blocks to every EN. The greatest pointer module is made out of a most extreme discoverer segment and comparators which

Yields $I_q^{(j)} = 1$ at whatever point the comparing vitality is equivalent to the most extreme, and $I_n^{(k)} = 0$ generally. Pointer value $I_q^{(j)}$ are grow-rapidly to the AND gate inputs, and joined with the RS succession. This AND gate inputs are mainly indicates the difference between PGDBF and GDBF. All bits with $I_q^{(j)} = 1$ are flipped in the GDBF decoder. Just the bits with $I_q^{(j)} = 1$ and $R_q^{(j)} = 1$ are modified in the PGDBF decoder.

In each and every cycle syndrome check block repeatedly conduct an OR task on the DNs values to verify whether the center of the middle grouping $d^{(j)}$ is a code word, if so the extracting process is stopped. Other case when the extract ended is the point at which no code word $d^{(j)}$been found, and a predestination most extreme number of emphases It_{max} has been come to, in which situation a disappointment interpreting is registered. In which all parts in the design of decoder are combinational circuits with the exception of the registers $d^{(j)}$ and y. accordingly, updated qualities of the bits in $d^{(j)}$ are refreshed after each and every cycle.

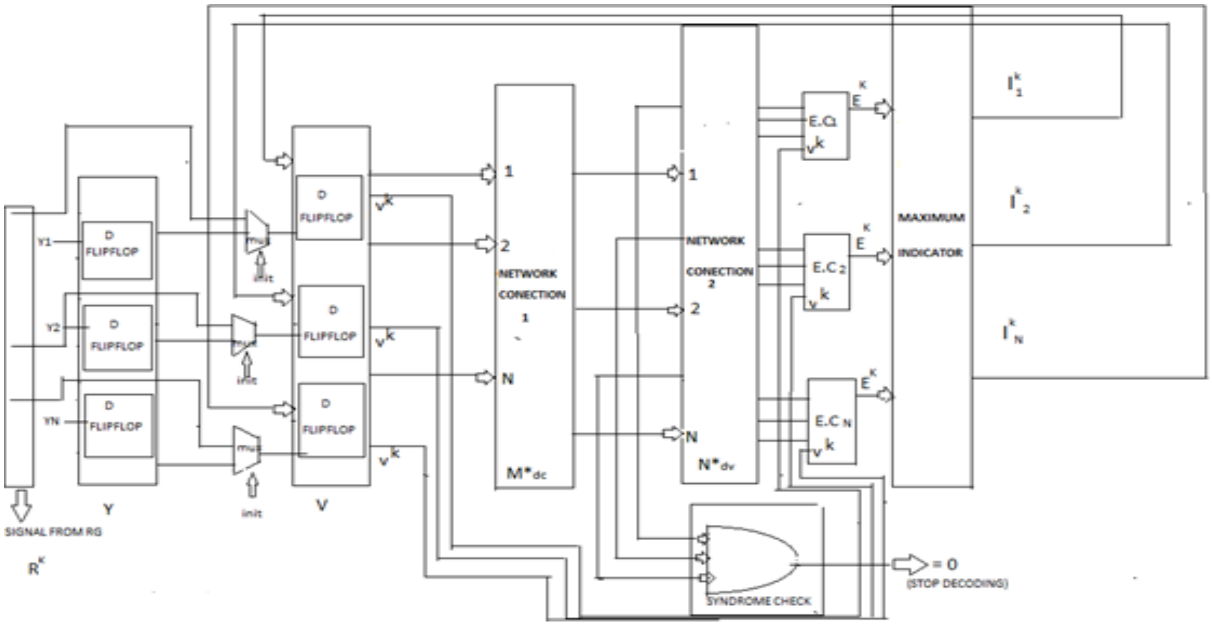

Fig.3 The Global architecture of PGDBF

B. MAXIMUM INDICATOR OPTIMIZATION

The main block from which the output is considered is maximum indicator block of PGDBF, this handles the Global design critical path in fig.3 and it caps the throughput of the decoding and reachable working recurrence. The experts conformed the extensive usage of find the most extreme incentive out of a random rundown of N numbers is dependably an Exchange off between calculation
cost and region/vitality utilization. Since our objective isn't just to get a streamlined decoder concerning different targets, counting equipment cost minimization, and in this design we are focused on only minimization of the critical path in the maximum indicator block with no focus on cost of hardware equipment. Above implies of not considering Traditional Binary Tree method which reduces the area and power consumption and considering Leading-Zero Counting Topology which increases the decoding speed. Proposed approach does not consider looping (k).

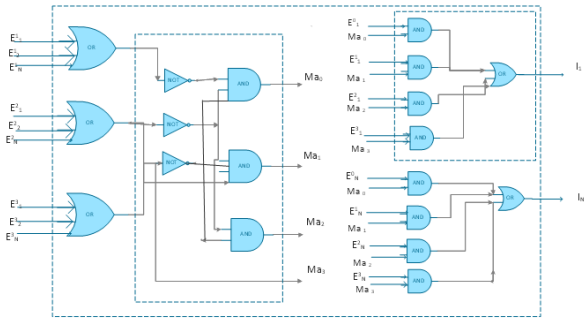

Fig 4 Maximum indicator block

IV. DISCUSSION AND RESULTS

My design is simulate using Xilinx ISE 14.5 minimizes the decoding speed the displayed resulted output (fig 5) of PGDBF with modified maximum indicator (MI) with the traditional binary tree method (TBT) to focus on the method which leading to zero counting topology (LCT).

Fig 5: Simulation output

V. CONCLUSION

We implement the PGDBF algorithm with effective hardware application as an alternative for hard decision model iterative decoder with achievement of subsequent MS decoder. Our main intention in this design is to reduce the resources needed to plan for irregular disorders of the PFDBF and minimize operation of MI block. The main block is completely based on short random sequence (SRS) that is replica apply on PGDBF modified guidelines. We are planned for implementing another two methods to initialize the Random Signal (RS) those methods are LFSR task and IVRG task, we are using same hardware for both the tasks but works on different behaviors on deferent LDPC codes. We significantly improved the decoding throughput of the Bit-flipping decoders with contraction of maximum indicator block with LCT in order to shorten the crucial way. Compare to other design this design is very faster, consumes less chip area and very low cost.

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