Design an All Digital PLL with Ripple Reduction Technique

Rajni Singla, Rekha Yadav

Abstract: ***The article describes about the design and implementation of advance version of Phase Lock Loop (PLL) is All Digital PLL. Research work is on ADPLL where parameter ripple is reduced by applying the technique of ripple reduction technique. Ripple reduction technique reduces the use of Kth counter, Kth counter comes under consideration when enable is ON. Phase locked loops are most widely used in communication system. Most of the PLL's that are used currently are hybrid type PLL's where all the blocks are assumed to be digital. The circuit design of ADPLL consists of Digital Controlled Oscillator (DCO), loop filter and Phase Frequency detector (PFD). Here phase detector used is Ex-or gate, for loop filter, Kth counter is used and Increment/Decrement circuit is used as DCO. Divide-by-N counter is used for feedback system. The output of the DCO is going in the PFD through the feedback network. Xilinx Vivado suit 2018.2 tools is used for simulating Verilog code. Board chosen in vivado is zed board Zynq. First, with the help of circuit diagram of ADPLL Verilog code is being written on project window. After compilation of code it is simulated with the help of test bench. After that it is going to be implemented and verified with the board zedboard. Number of LUTs used are 32 and Flip Flops used are 35. This paper presents an all digital approach for the design, simulation, synthesis and implementation of FPGA based ADPLL centered at 195.31 KHz using Verilog HDL code. The proposed design methodology resulted in reduction of ripple, power dissipation, junction temperature of board. Proposed research work further can be used in communication for frequency synthesizer. Any system whether it is from communication or digital etc ADPLL is common to use for ripple reduction at its output. So ADPLL is basic building block in any type of communication system.***

Index Terms**: *ADPLL, Ex-or Phase detector, Kth counter, Counters, Ripple Cancellation Circuit.***

I. INTRODUCTION

In earlier times, Phase locked loops are most widely used in telecommunication system. DPLL is the main element used in telecommunication system to improve phase error [1].It ensures that the clock must be synchronized in the receiver and transmitter. One of the earliest DPLL was discovered by adding a sample and hold circuit between the loop filter and the voltage controlled oscillator (VCO) in an analog loop. As the improvement in technology increases there is a demand for better resolution PLL. Advancement in PLL increases to All Digital PLL where all the blocks are in digital form with better resolution. Over DPLL ADPLL has the advantage that all the component is digital. To obtain good phase error and frequency error new DCO was invented in 1980's.The most common function of the ADPLL is to provide synchronization of the signal. ADPLL is easy to implement into FPGA. The circuit design of ADPLL consists of Digital Controlled Oscillator (DCO), loop filter, and Phase Frequency detector (PFD). Here phase detector used is Ex-or gate, for loop filter Kth counter is used and Increment/Decrement circuit is used as DCO. Divide-by-N counter is used for feedback system. The output of the DCO is going in the PFD through the feedback network. With the advantage of zero phase error the scope of using ADPLL becomes popular. ADPLL circuit can be implemented in lock detection techniques, Phase Demodulation, FSK decoding, Data synchronization, Position indicator, Frequency synchronization and multiplication. PLLs have four types –digital PLL, linear PLL, **All digital PLL**, and software PLL [3].

The paper describes about phase detection system using Ex-or phase detector and loop filter used in this design is K counter. The advantage of ADPLL is its DCO block which is digital in nature. The feedback circuit is replaced with Divide-By-N counter.

This paper is organized as: Section I describes an overview of ADPLL section II describes about the design of ADPLL where all the components are described precisely. Another circuit is added to ADPLL is Ripple Cancellation Circuit. Section III shows the tool used for simulation is Xilinx Vivado. Equations used to calculate some parameters are to be calculated in section IV. Simulation and result is discussed in the section V. Paper ends with conclusion part in section VI.

II. DESIGN OF ADPLL

The basic ADPLL consists of four elements: phase detector, a Kth counter, an I/D network and N counter (D/N) [4].

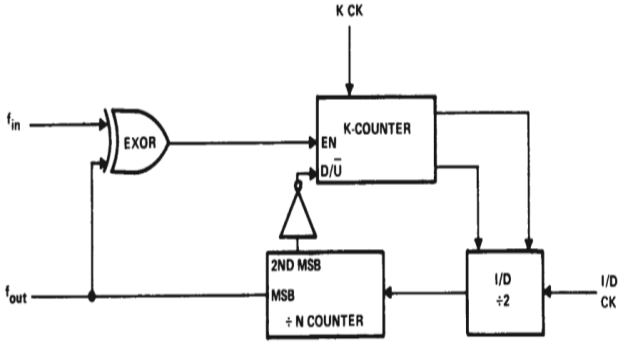

Figure 1 : ADPLL with ripple cancellation circuit

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Ripple circuit contains an additional not gate in between two counters.

A. Phase Detector (PD)

Here, Ex-or gate is used as a phase detector. Two inputs are fed into PD. One is an input frequency which can be varied with respect to reference frequency. Minimum input frequency is 9.76MHz with reference frequency 5GHz. Output should be zero so that frequency of input and output matches.

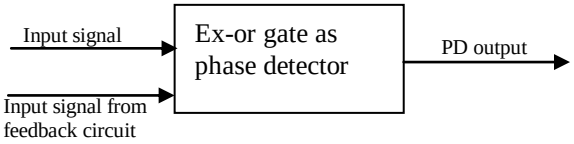

Figure 2: Phase Detector Using Ex-Or Gate

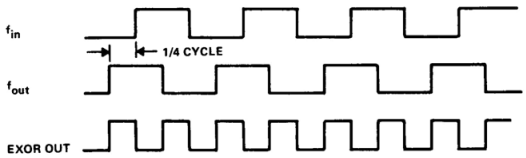

Figure 3 : Phase detector output using Ex-or gate

Figure shows the PD compares the output signal with the incoming signal.

B. Loop Filter

K counter is used as a loop filter in this circuit. K counter is a combination of two counters Up and Down counter.

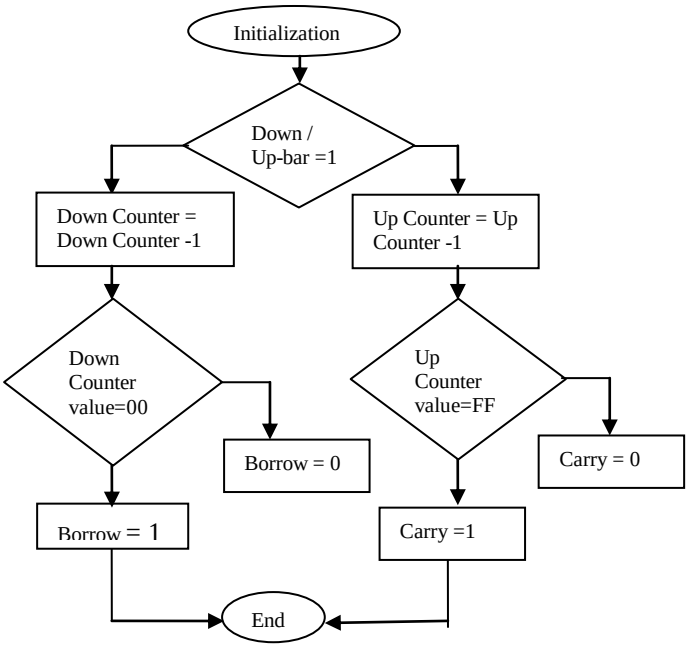

Figure 4 : Flow chart for K counter

Two external clocks are to be provided one is K-clock and another is I/D clock. The Kth up/down counter consists of one reference clock, up and down counter, and at the output it gives carry and borrow. Reference clock for K counter and I/D circuit is same. There is a flow chart for K counter. Counter works for 0 or 1. If 0 occurs up counter starts counting from 00 to FF because value of K is 256 where K is the modulus of K counter. Then carry becomes 1 and again it will check for PD output. Alternatively, same for down counter , it counts from FF to 00.

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C. Digital Controlled Oscillator (DCO)

DCO block contains I/D circuit. And I/D circuit consists of I/D clock, carry input, borrow input. The output of DCO block depends on value of carry and borrows. Output is invalid for carry=1 and borrow=1. The output of I/D circuit is given to counter circuit and the output is again given to phase comparator if phase is not locked.

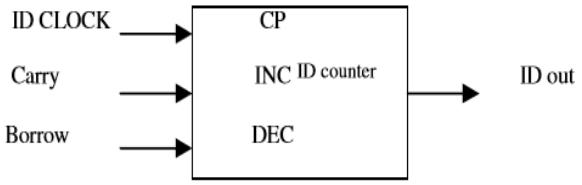

Figure 5: DCO Block Diagram

Flow chart is drawn of DCO block. With the positive pulse of reference clock circuit is checked for carry and borrow. If both are zero then the frequency is automatically divided by 2. If carry occurs then clock is incremented by adding a pulse. If borrow occurs then clock is decremented by deleting a pulse.

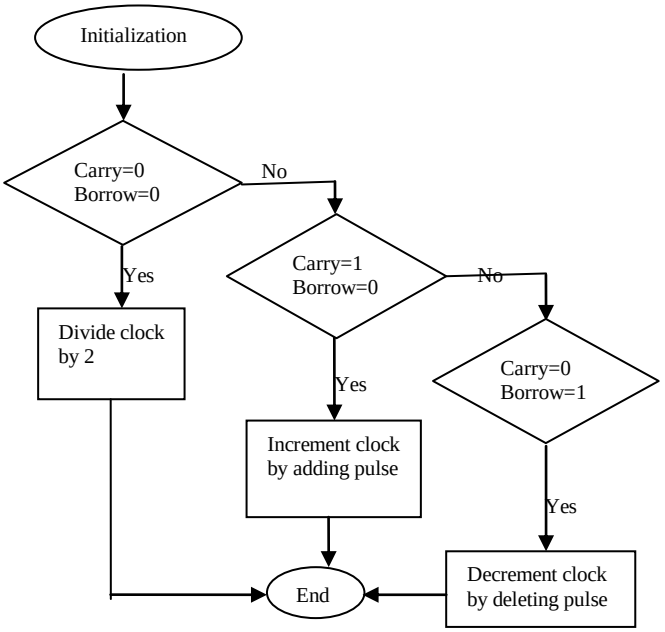

Figure 6: Flow chart for Increment/Decrement circuit

Figure shows the waveform of carry and borrow with ID out. Output of K counter is named as carry which is increment signal in ID block. Same applied with borrow output and decrement input.

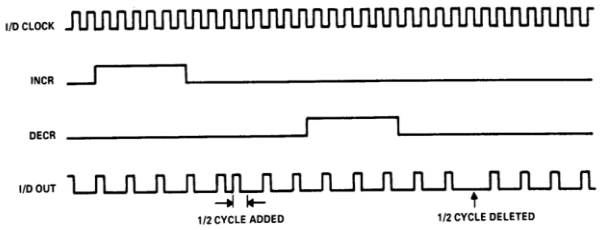

Figure 7: I/D Circuit Waveform

III. ADPLL USING VERILOG HDL

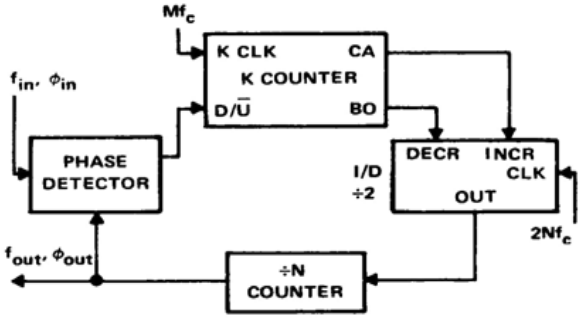

Figure 8: Structure of ADPLL

Knowing that PLL compares the phase of incoming signal $\emptyset_{in}$ with the signal produced by PLL $\emptyset_{out}$, the phase detector in ADPLL do the same and output an error signal, $k_d \emptyset_e$, where k_d is the gain of phase detector and $\emptyset_e$ is the phase error $(\emptyset_{in} - \emptyset_{out})$. The Ex-or phase detector has a gain k_d of 4 and has phase error limit of $\pm 90^0$. The Kth up/down counter consists of one reference clock, up and down counter, and at the output it gives carry and borrow. The I/D circuit works together with increment/decrement (I/D) circuit which also has a reference clock. If 2N=M, then reference clock of the block is same for K counter as well as for I/D circuit. Here, reference clock of I/D and Kth counter is same. By applying Ripple cancellation technique K counter is disabled causing minimum ripple. The PD gain reduces to half and phase error limit reduces by the factor 1/(1+1/2K). The ADPLL continually adjusts the phase of f_{out} so that in the lock condition a definite phase difference will exist between f_{in} and f_{out}.

When code is simulated on Xilinx tool it has different frequencies and fixed frequencies are captured where phase is locked. At maximum input frequency 9.76MHz phase is locked with same output frequency by applying reference frequency of 5GHz. For implementation on FPGA zedboard is selected for proposed work. Centre frequency is 195.3 KHz. K is the modulus of Kth counter and its value taken is 256. N is the modulus of N counter and also its value is taken as 256. Values of N and K can be varied. At K=N=256 all the input and output frequencies are locked. Code is simulated for various K=256, 128, 64 and is implemented on Xilinx Vivado tool 2018.2. Code is written on Verilog HDL language. The output results are 35 Flip flops and 32 LUTs..

IV. MATHEMATICAL MODEL FOR PROPOSED WORK

K- clock has frequency of Mf_c , where M is constant number and f_c is loop center frequency ,

$$f_c = I/D \ \ clock/2N \ \ Hz \qquad (1)$$

I/D clock has frequency $2Nf_c$ where N is modulus of D/N counter.

k-counter and I/D circuit outputs are :

$$K_{out} = (k_d \ \emptyset_e M f_c)/K \qquad Hz \qquad (2)$$

$$I/D_{out} = N f_c + (k_d \ \emptyset_e M f_c)/2K \qquad Hz \qquad (3)$$

K_d is phase detector gain and $\emptyset_e$ is phase error and K is the modulus of Kth counter .

The loop output is :

$$f_{out} = f_c + (k_d \emptyset_e M f_c)/2KN \qquad Hz \qquad (4)$$

refer to this equation we can calculate the tracking frequency range Δf_{max} . At the limit of lock range $k_d \emptyset_e$ is ±1.

Therefore :

$$\Delta f_{max} = (f_{out})_{max} - f_c = M f_c/2KN \qquad Hz \qquad (5)$$

Lock range may be adjusted by adjusting K.

When DPLL is in lock condition f_{out} equals f_{in} and a definite phase error ,$\emptyset_e$, will exist between two signals.

From equation (4)

$$\emptyset_e = 2KN \ (f_{in} - f_c)/k_d M f_c \qquad cycles \qquad (6)$$

Which is phase error between f_{in} and f_{out} under lock.

By applying ripple cancellation circuit lock range will be:

$$\Delta f_{max} = M f_c/(1 + 1/2K)4KN \qquad Hz$$

V. SIMULATION ANALYSIS AND RESULT

Behavioral Simulation is analyzed on Xilinx vivado. Vivado is a complete package for FPGA. Simulation, synthesis, and implementation of FPGA are done on same platform.

A. Simulation result

Figure shows the simulation result of proposed work. The input frequency with respect to reference frequency can be taken upto 9.76MHz. This result is for K=256. After synthesis power dissipation become 0.374W which is less with previous work.

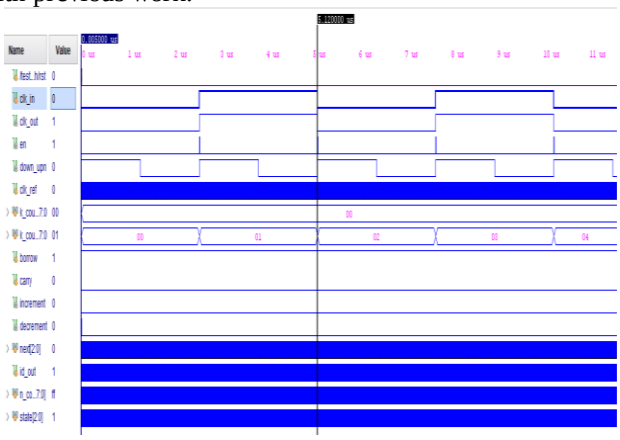

Figure 9: Simulation result of proposed work.

B. RTL view of proposed work

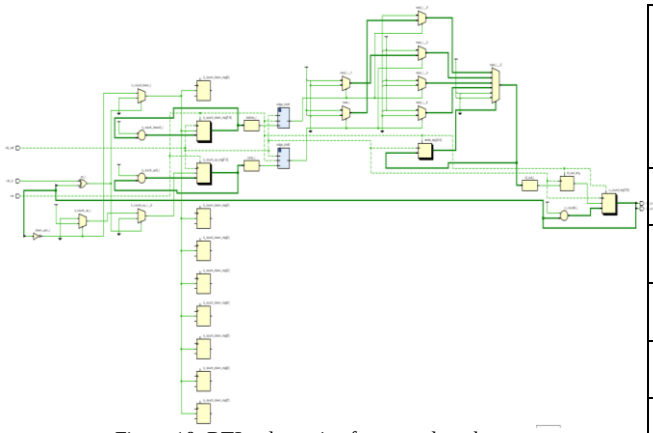

Figure 10: RTL schematic of proposed work

C. Comparative analysis with previous work

Table 1 shows the comparison of FPGA board zedboard with Spartan 6 [4]. Power dissipation is compared with [28].

Table 1: Comparative Analysis With Proposed Work

Parameters	Proposed ADPLL	ADPLL [28]	ADPLL[4]
Power dissipation	0.374W	0.405W	-----
Junction Temperature	30.6°C	31.0°C	----
Phase error	0	0.5	0
Lock range	389.86KHz	-	90KHz
Centre frequency	195.31KHz	19531.25	196KHz
Flip Flops	35	-----	75
LUTs	32	------	75

Different values for K are simulated with different input frequency. Table and graph shows different output frequencies for K=128.

Table 2: Difference between output frequencies for K=128.

INPUT FREQUENCY(Hz)	OUTPUT FREQUENCY(Hz) AT K=128 FOR NORMAL ADPLL	AT K=128 FOR RCC
3.9	3.92	3.9
3.9K	3921	3906
19.5K	19607	19531
39.06K	39215	39060
48.8K	49019	48820
97.6K	98030	97656
100M	196000	196000
1.9G	1960000	1953000
1.95G	19607000	19450000
39.06G	19607000	19530000

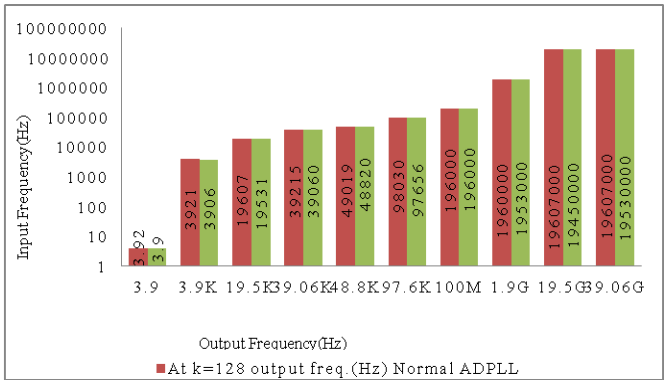

Figure 11: Input v/s output for K=128

VI. CONCLUSION

ADPLL with ripple Cancellation Circuit is well simulated and implemented on Vivado. The proposed ADPLL naming ADPLL with ripple cancellation circuit consists of PD, loop filter and DCO and one not gate. Phase detector used is Ex-or gate. Kth counter used as a loop filter and Increment/Decrement circuit to make DCO. Here in the feedback circuit component used is N counter. The value of K which is modulus of K-counter is varied. Value of K is taken as 256, 128 and 64. Circuit is free from ripple and input is equal to output frequency at fixed reference frequency. Power dissipation decreases up to 2%. Phase error becomes zero with centre frequency 195.31 KHz. Junction temperature also decreases in the program. Number of flip flops used are 35 and slices of LUTs are 32.Bar graph gives the result of proposed ADPLL and previous ADPLL at K=128. Hence, the proposed ADPLL can widely used in phase detection where it gives 100% result because of no ripple.

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