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Low Phase Noise Current Starved Ring VCO on MOS Capacitance

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Abstract: ***In Wireless communication system VCO is major part which regulates the frequency according to the voltage. Ring oscillator of one type of VCO is used. The topology of Ring oscillator is current starved Ring VCO, is used. In this topology the oscillation frequency is regulated by MOS capacitance. MOS capacitance is added at the end of every stage of inverter.180 nm CMOS technology is used in this paper. The supply voltage is 1.8V and control voltage is varied from 0V to 1.8V. The simulated results are shown that good tuning range from 2.06GHz to 2.62 GHz. which is used in application of wireless system. The phase noise is measured -112dbc/Hz at 1MHz.***

Keywords: VCO, MOS Capacitance, tuning range, Phase noise.

I. INTRODUCTION

Wireless communication systems are driven with high frequency signals like Radio Frequency signals, microwave signals and radio signal. Its range is varied from some Hz to GHz. VCO is playing major role in wireless communication system.VCO is an electronics system. It provides good enough high frequency to system. VCO provides periodic signal which is required in digital system, analog system and RF system etc.VCO also provides the linear relationship that is control voltage with the oscillation frequency. VCO is key point in PLL, LNA. In PLL power dissipation and occurring area are decided by VCO. In power dissipation term VCO controls the oscillation frequency with the control voltage.

There are some parameter of VCO like frequency of oscillation, tuning range, phase noise and figure of merit. Some application depends on these parameter are Bluetooth, Cell phone, PLL, LNA etc. Generally VCO is divided into different part one is ring oscillator and another is LC VCO. LC VCO consists of inductor and capacitor. It provides the periodic signal. It can be used where the size of area is not big issue. Because of size of inductor is higher than another component. It provides higher phase noise than ring oscillator. Ring oscillator consists of odd number of inverter stage. It provides the multiphase. It covers less area than LC VCO.It provides better tuning range than LC VCO.In communication system data is transferred with high speed rate. Clocking recovery is key point in it. Multiple phase handle the clock recovery. The output frequency expression of VCO is given as

$$f_{out} = f_o + K_{vco} * V_{ctrl}$$

Where fo is carrier frequency, Vctrl is control voltage, Kvco is sensitivity or gain of VCO. The proposed design describe the performance of 5-stage current starved Ring VCO with switching MOS capacitance in terms of higher frequency of oscillation, low power supply and low phase noise. In the section I. shows brief information about switched capacitor Ring oscillator. Section II shows explanation about current starved Ring VCO. Section III. Shows explanation about proposed circuit of switched capacitor Ring oscillator.

II. RING VCO WITH MOS CAPACITANCE

Figure.1 shows switched capacitance based Ring VCO. It consists of 3 stage cascaded inverter. The MOSFET Q2-Q6 having W/L ratio is 1.12 and Q1-Q5 having W/L ratio is 2.13. Three NMOS is connected at each every stage of inverter. It acts as MOS capacitance. This is controlled by control voltage. This circuit is simulated in 90nm CMOS Technology. It provides 23 % tuning range. Phase noise is given as -76 dbc/Hz at 1MHz offset frequency. It uses the supply voltage is 1.8V. The linear tuning characteristics are shown with varying control voltage from 0V – 0.5V.

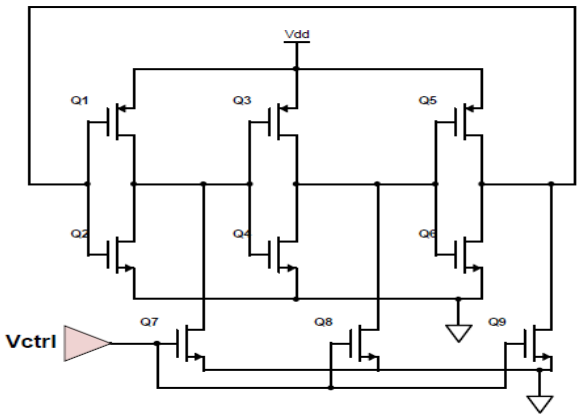

Figure. 1 Ring VCO with switching capacitance

III. CURRENT STARVED RING OSCILLATOR

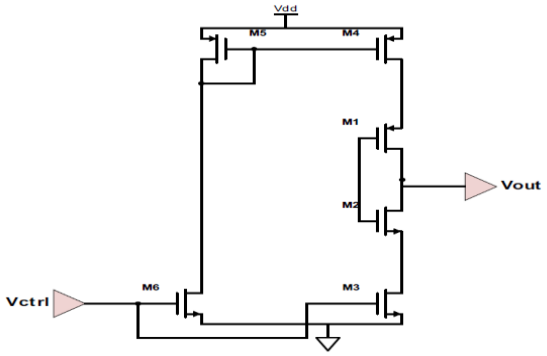

Figure.2 Single delay of current starved Ring VCO

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In Ring oscillator oscillation frequency is regulating by variation in delay, which is offered by the each inverter stage. The delay is regulating by control voltage.

Another way of delay controllation is that control the amount of current which is present to capacitive load of each inverter stage, this is called Current starved Ring VCO. In this control voltage regulate the amount of current which is available to the inverter stage. If the value of control voltage is high than large amount of current will flow so that delay will be reduced. In the current starved Ring VCO oscillation frequency is controlled by variable bias current as illustrated in Fig. 2 [6].

The MOSM1 and MOSM2 acts as inverter, MOSM3 sinks the current, available to inverter and MOSM4 works as source of current. The current source controls the flowing current into the inverter. The bias current of MOSM5 and MOSM6 are same which is controlled by the control voltage (Vctrl). The current in MOSM4 and MOSM5 are mirrored. With the help of this topology we get higher frequency of oscillation. It can be achieved for wide band by regulating the Vctrl.

IV. PROPOSED DESIGN CIRCUIT

A. Circuit Explanation

The Current Starved Ring VCO with switched capacitor is shown in figure.3. Generally this circuit works similarly Ring oscillator. In this circuit every stage is connected with inverter the MOSN13 –MOS17 having W/L ratio is 1.18 and the MOSP7 – MOSP11 having W/L ratio is 2.15. The 5 extra NMOS is connected with end of each stage inverter. These MOS capacitances controlled by the control voltage (Vctrl). An extra inverter is connected at the output side which is acts as buffer circuit. The resistances R1-R5 are connected at each stage of inverter.

B. Controlling Capacitance

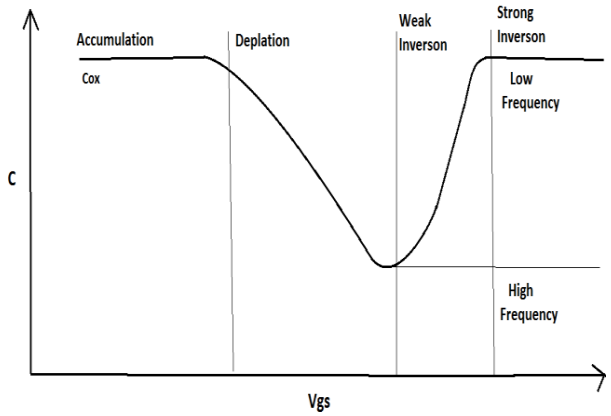

Figure.4. CV characteristics of MOS Capacitance

The range of operating frequency is opted by the changing in gate capacitance of NMOS which is controlled by variable control voltage (Vctrl). This phenomenon is explained through CV graph of MOS capacitor which is shown in Figure.4.

In accumulation region (Vg < Vfb) in this region gate capacitance is maximum. Where Vg denotes gate voltage and Vfb is flat band.

In depletion region when the Vcrtl is increased (0< Vctrl < Vtn), gate capacitance of MOS is decreased. Where Vtn denotes threshold voltage of MOSFET. Gate capacitance of MOS is inversely proportional to the width of region.

When the Vctrl is further increased (Vctrl > Vtn) then it enters into inversion region.

In weak inversion region (Vds < = Vgs-Vtn). In this region gate capacitance is increased corresponding to Vctrl. It is also called linear region. In this region oscillation frequency is higher.

In strong inversion region (Vds > Vgs-Vtn). It this region gate capacitance is decreased corresponding to Vctrl. It is also called saturation region. In this region oscillation frequency is lower.

The gate capacitance of NMOS at each stage of inverter acts as a switches. It can be changed by a resistance .The delay can be expressed as

$$Td = (CL' \| CL)/Gm \quad (1)$$

The frequency of oscillation can be described as

$$f_o = \frac{Id}{2N * Ctotal * Vctrl} \quad (2)$$

$$Ctotal = CL' \| CL \quad (3)$$

Id = Bias current, f_0 = frequency of oscillation

V. MATHEMATICAL ANALYSIS

Phase noise is a vital specification of any oscillator. It is unwanted signal from the main carrier signals. It means random frequency fluctuation. Frequency stability is a term to which oscillator keeps the constant value of oscillation frequency of given time intervals. It is generally expressed as

$$L(\Delta w) = 10\log\frac{Pssb}{Ps} \quad (4)$$

Where P_{ssb} is the power of single sideband and P_s is the total power.

Classical equation of phase noise is given by Lesson formula as

$$(fm) = \frac{FkTB}{2Pavg}\left[\frac{1}{fm^2}\frac{f0^2 fc}{4QL^2} + \frac{1}{fm^2}\left(\frac{f0}{2Ql}\right)^2 + \frac{fc}{fm} + 1\right] \quad (5)$$

Where QL is loaded quality factor, k is Boltzmann constant, F is noise factor of active device, T is temperature in k, fm is carrier offset frequency, fo is carrier center frequency, Pavg is average power and fc is flicker corner frequency.

Power is determined by

$$Pdc = Vs\ Id \quad (6)$$

Where Pdc is DC power and Vs is supply voltage, Id is drain current

The tuning range is given as

$$\text{Tuning range} = \frac{fmax - fmin}{\left(\frac{fmax + fmin}{2}\right)} \quad (7)$$

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VI. SIMULATION CURVE

The proposed design VCO is analyzed using the Cadence 180nm CMOS Technology with Virtuoso software. Figure.5. shows the transient analysis of proposed VCO. In this control voltage is set at 1V and frequency of oscillation is 2GHz.Figure.6 shows the tuning characteristics of proposed VCO. It shows the tuning range varies from 2.06 GHz to 2.62 GHz with control voltage (0.5V-1.2V). Fig. 7 represents the phase noise of proposed oscillator. It is -112.00 dBc/Hz. This is at offset frequency of 1MHz

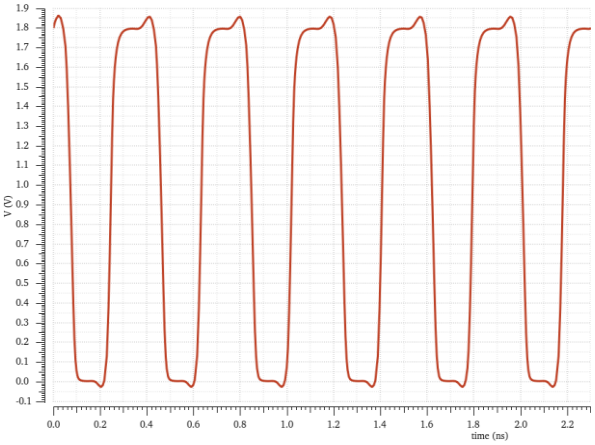

Figure.5. Transient Analysis

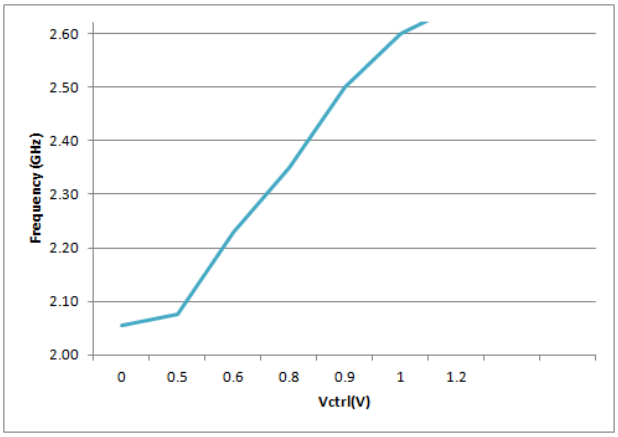

Figure.6 Tuning Range

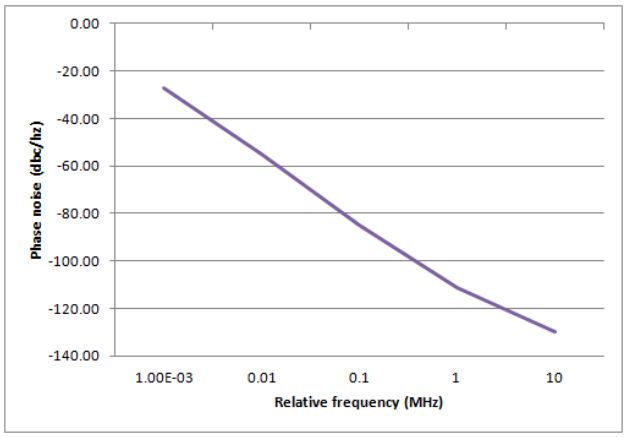

Figure. 7 Phase Noise

Figure.8 shows graph plot between variation in control voltage and regulating frequency of oscillation. It shows linear correlation when the gate capacitance voltage is increased, resulting frequency will be increased. It is suitable for wireless communications.

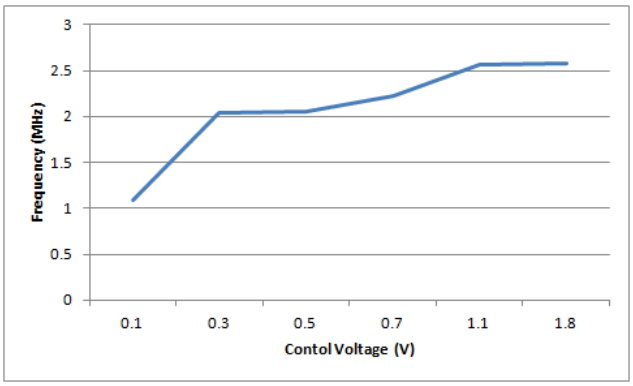

Figure .8 Oscillation Frequency V/S Control Voltage

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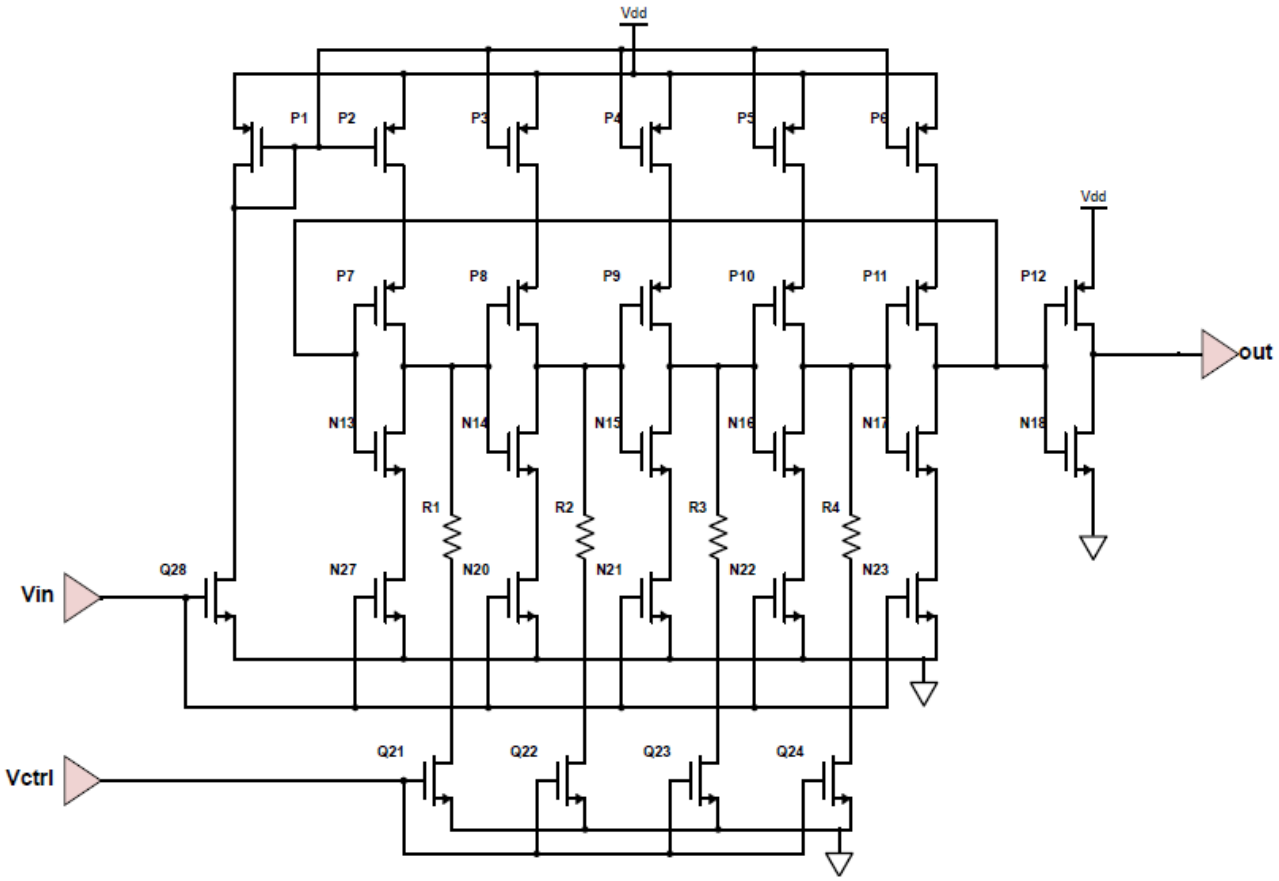

Figure.3 Schematic of Proposed design circuit

COMPARISON WITH PREVIOUS RESEARCHS

Control voltage(V)	Frequency (GHz)
0.1	1.085
0.2	2.044
0.3	2.044
0.4	2.045
0.5	2.056
0.6	2.106
0.7	2.227
0.8	2.406
0.9	2.532
1	2.56
1.1	2.569
1.2	2.575
1.3	2.577
1.4	2.579
1.5	2.581
1.6	2.582
1.7	2.583
1.8	2.585

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Specification& Reference	3- stage [2]	4- stage [10]	3-stage [3]	This Work
CMOS Technology (nm)	180	180	90	180
Voltage (V)	1.8	1.8	1.8	1.8
Tuning Range (%)	20	19	23	23
Power Consumption (mW)	6.99	12.6	0.295	36
Phase Noise(dBc/Hz)	-112 @ 10MHz	-91 @ 1MHz	-76.27@ 1MHz	-111@ 1MHz
Control Voltage (V)	0.0-1.1	-0.8 -0.2	0.0- 0.6	0.5-1.2

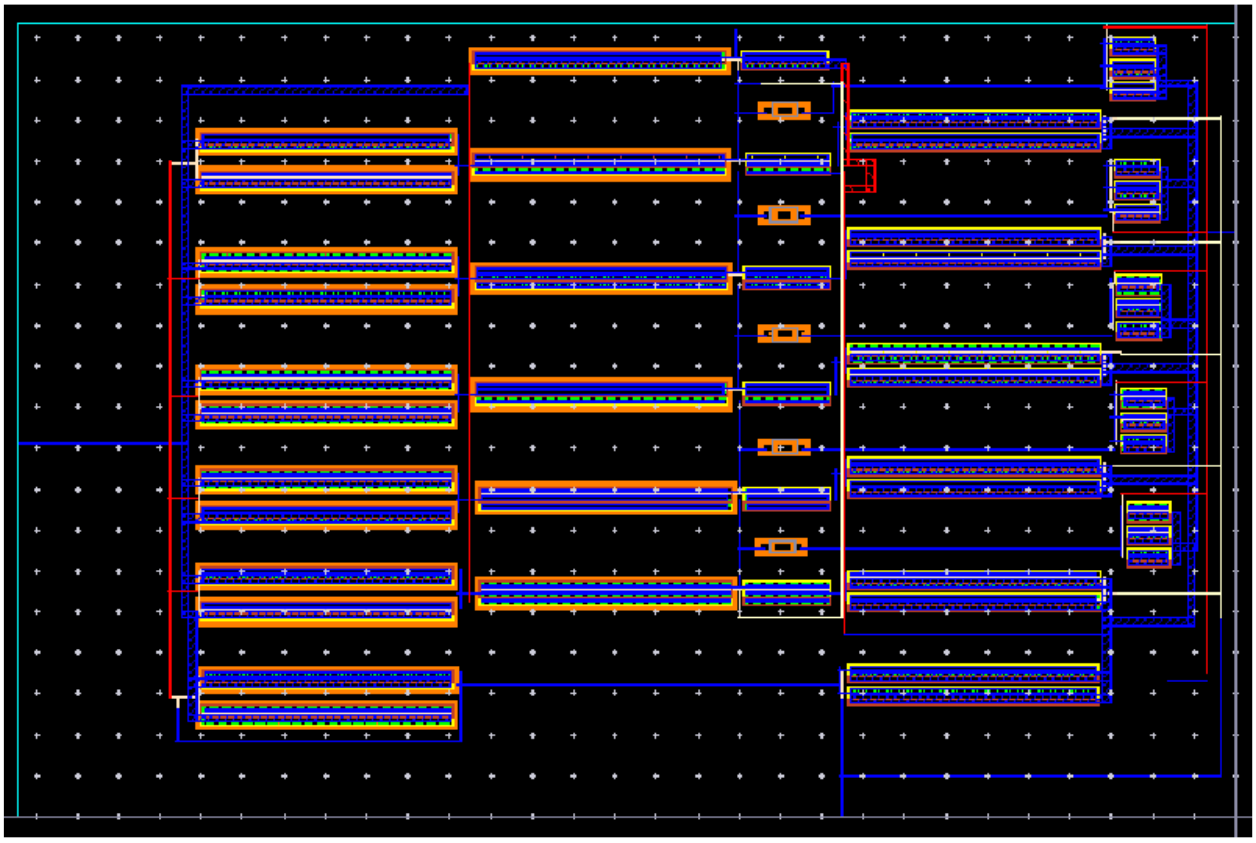

Figure.7 Layout of proposed design circuit

Vin	1.8 V
Vctrl	0V-1.8V
Vdd	1.8V
R1,R2,R3,R4	1K Ohm

VI. CONCLUSIONS

This paper represents the implementation of switched based Ring VCO. The 5- stage current starved switching based Ring VCO gives better performance than switched based Ring VCO. It is better in respect of schematic and simulation. The proposed circuit is simulated in Cadence Virtuoso software with 180nm CMOS Technology. The proposed circuit gives better outcomes in respect of higher Oscillation frequency. It is varied by control voltage.
The maximum frequency is 2.62 MHz. Phase noise is measured -112dbc/Hz at 1 MHz offset, tuning range is measured 2.06 GHz to 2.62GHz which is 23 %.

REFERENCES

1. R. R. Jagtap and S. D. Pable, “Design of low power current starved VCO with improved frequency stability,”Int. Conf. Recent Adv. Innov. Eng. ICRAIE 2014, 2014.
2. J. Jalil, M. B. I. Reaz, M. A. M. Ali, and T. G. Chang, “A Low Power 3-Stage Voltage-Controlled Ring Oscillator in 0 .18 µm CMOS Process for Active RFID Transponder,” pp. 69 – 72, 2013.
3. Rafiul Islam, Ahmad Nafis Khan Suprotik,” Design and Analysis of 3 Stage Ring Oscillator Based on MOS Capacitance for Wireless Applications”in International Conference onElectrical, Computer and Communication Engineering (ECCE), Cox’s Bazar, Bangladesh, pp.723-727.
4. S. Lee, B. Kim, and K. Lee, “A Novel High-Speed Ring Oscillator for Multiphase Clock Generation Using Negative Skewed Delay Scheme,” vol. 32, no. 2, pp. 289 – 291, 1997.
5. A. Mishra, “Design of Power Optimal, Low Phase Noise Three,” pp. 1 – 5, 2014.
6. Gudlavalleti Rajahari, Yashu Anand Varshney, and Subash Chandra Bose, “A Novel Design Methodology for High Tuning Linearity and Wide Tuning Range RingVoltage Controlled Oscillator”, Springer-Verlag Berlin Heidelberg 2013, CCIS 382, pp. 10–18, 2013.
7. Shruti Suman, Monika Bhardawaj Prof. B. P. Singh, “An Improved performance Ring Oscillator Design”, in International Conference on Advance Computing and Communication Technology, Rohtak, India, IEEE digital library, pp. 236-239, Jan. , 2012.
8. C. Sánchez-Azqueta, S. Celma, and F. Aznar, “A 0.18um CMOS ring VCO for clock and data recovery applications,”
9. Microelectron. Reliab., vol. 51, no. 12, pp. 2351 – 2356, 2011.
10. B. Razavi, “Design Of Analog Cmos Integrated Circuits”. H. Shizhen, L. Wei, W. Yutong, Z. Li, and A. C.
11. Circuit,“Design Of A Voltage-controlled Ring Oscillator Based On MOS Capacitance,” vol. II, pp. 18 – 20, 2009. Shruti Suman, Monika Bhardawaj & Prof. B. P. Singh (2012), “An Improved performance Ring Oscillator Design” in International
12. Conference on Advance Computing and Communication Technology, Rohtak, India, IEEE digital library,236-239. Vaishali, Shruti Suman, K. G. Sharma, P. K. Ghosh, “ Design of Ring Oscillator based VCO with Improved Performance,” in.
13. Innovative Systems Design and Engineering- IISTE, Vol. 5, no. 2, February 2014, pp. 31-41.
14. Stephen Docking and Manoj Sachdev “A Method to Derive an Equation for the oscillation Frequency of a Ring Oscillator” IEEE Transaction in Circuits and Circuits and Systems-I: Fundamental Theory andapplications,Vol.50,No.2,February2003.
15. M. R Halesh, K. R Rasane, and H. Rohini “Design and Implementation of Voltage Control Oscillator (VCO) Using 180 nm Technology”, Springer - Verlag Berin Heidelberg, CCIS125,pp.472-483.

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