Reducing the Delay by Optimizing the Via in Compact Automatic Metal Routing Algorithm

Repudi Veerendra Kumar, Gummadidala Venkata Rao

Abstract: ***The Very Deep Submicron Technology (VDSM) shrinking rapidly, we have 22nm, 14nm, 7nm and now research going on 5nm technology. That means size of the transistor shrinking, and number of interconnections increased as well. Resulting interconnections playing a major role in delay, IR drop, area etc. To reduce the delay, we are utilizing higher metal layers. Further we gone for Compact Automatic Metal Routing, nothing but Over the cell channel routing to efficiently perform routing, but the problem for such type of routing technique, stacked vias needed and that results increased resistance, delay, IR drop will degrade the performance. That may be obstacle to meet timing in Clock Tree Synthesis stage (CTS). This paper mainly focus on reducing the delay further by designing the via structure by using the tool cadence encounter***

Index Terms: Via, Routing, Physical Design, VDSM.

I. INTRODUCTION

One of the crucial phases in the VDSM technologies is Routing. The major task is to assign routing segments for interconnections to particular routing tracks, via's and metal layers. Estimating the wire resistance, transition time and capacitance, to determine whether the design meets's timing or not. Delay is one of the major factors to reside the meeting time and that dependence on RC (Resistance Capacitance) constant. To provide a connection between the metal layers we need via (vertical interconnect access). To meet speed, less IR (voltage) drop, increase transition time we gone for higher metal layers and present we have twelve metal layers. When we are going from lower to higher metal layers the resistance will be less , increase in speed , less power consumption as well .If gone for higher metal layers results higher number via's that degrades the performance and leads to increase in manufacturing cost also. To gain better yield we need to reduce the number of via's, but in some cases via's are unavoidable in that situation we need to look for better performance by designing the via properly.

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The circuit performance affects by each via with its own resistance. In this paper, we try to reduce resistance, Rise transition time, fall transition time and that results delay of wire will be reduced. The resistance of wire depends on the length, width and on resistivity of that metal. So here we can't change the length of wire at the same time cannot change thickness also, cause that results current density problems. By varying the width of the via in minimum allowable space in track and with satisfying the DRC (Design Rule Check) rules we are able to control the Resistance and slew transition time. Initially the tool itself generates routing and after that we modify the via and show the results giving better performance than before.

In routing stage when want to go from one metal layer to another metal layer we need a via.

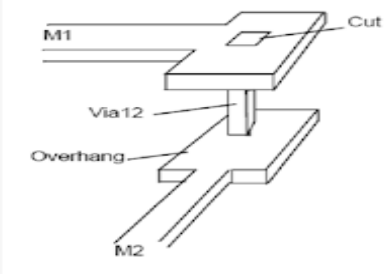

Fig.1.1 Single Via

In routing stage if we try to route to higher metal layers directly from the lower layers we need Stacked Via as shown in below.[1]

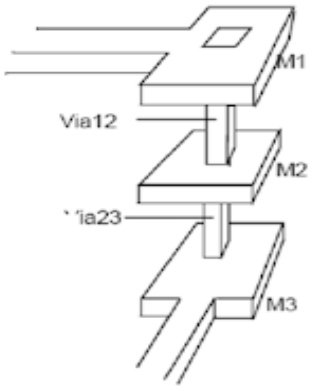

Fig.1.2.Stacked via

II. NECESSITY OF VIA MINIMIZATION

As we have discussed earlier the interconnections playing a vital role for meeting the time at CTS stage. Because via also have some resistance and when we are going for higher metals those results the number of vias are increased and that gives a excessive delay.

A. Utilizing higher metals

As of now we can use up to twelve metal layers for routing. Due to VDSM technology we can add as many layers as per our requirement. Utilizing higher metals more and more that may be benefit for performance, sometimes affects cost also.

B. Congestion

In Routing phase we need assign channel and that channel having the routing tracks. If we route with higher metals then it occupies more tracks that results required tracks will be more, this situation called congestion.[2]

III. EXISTED

We know that the determination of the circuit performance and reliability depends on interconnect which was used in the routing. FinFet technology based on 14nm is the present size in very deep submicron technologies.

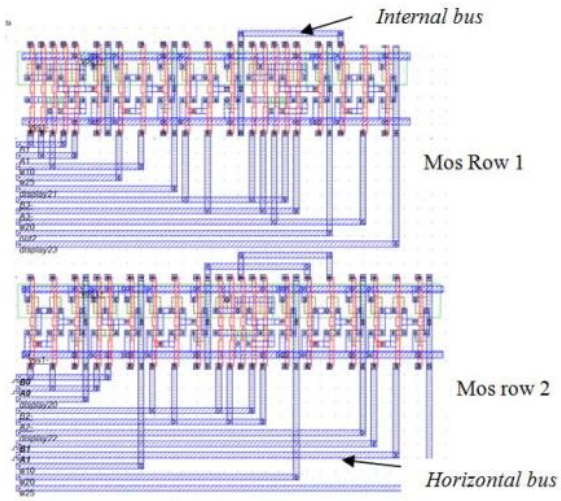

Fig.1.3.Routing evolutions in EDA tool

The routing evolutions and compact routing between the two MOS rows in EDA tool is depicted in the fig 1.3. Different strategies like Bus Routing, Compact Routing and I/O Routing should include in the EDA tool. Different metal strategies have their dedicated function for each. Metal 2 is used for vertical routing and metal 3 is used for horizontal Routing as illustrated in the fig 1.3. Routing cost depends on the Routing coordinates having by 4 internal bus and horizontal bus. Left side of the layout will be routed by metal 2 in the Bus routing process where as metal 4 and metal 3 for some horizontal extensions will be used to route over the cell in the compact routing process.

But, EDA tool provides more than ten metal layers necessary for Routing. Utilization of the maximum metal layers in VLSI design will gives optimum results include speed, power and performance of the circuit.

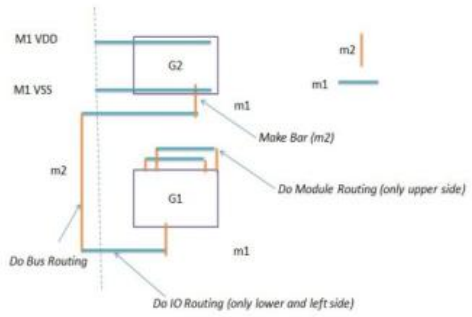

Fig.1.4.M1-M2 strategy

Different strategies for Routing are illustrated in the fig 1.4, 1.5. Internal connections are routed by Metal 1, routing between all nodes are done by Metal 2 with increasing layer. The area required for Routing, parasitic capacitances, coupling capacitances and delay are increased for this strategy and it will not affect the performance of the circuit, transition time and delay. But, the performance may degrade if the number of interconnects getting larger that results congestion.

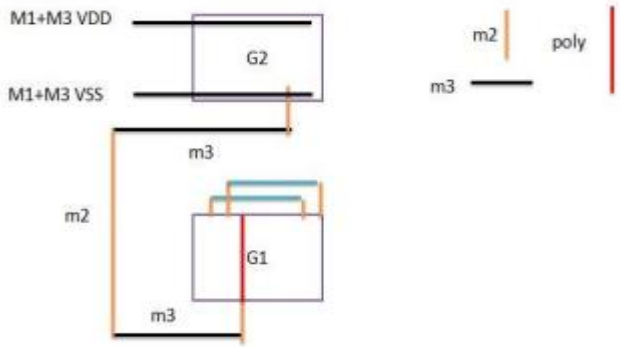

Fig.1.5 More no. of Metal strategy

Different strategies for Routing algorithms of EDA tool are depicted in the fig 1.5. From the fig, Metal 1 and Metal 2 are different metals, now the algorithm has the ability to routing with same metals even the circuit is divided in to two MOS rows. For vertical and horizantal connections M1 and M2 will be used respectively . The interconnections between these nodes will be routed automatically within the EDA tool. Likewise it is possible to route/ create a contact using Metal 3 automatically.[3]

Earlier designs of the circuits by using different metals, contacts are done in manual procedure. But, there is no chance to modify the design due to complexity of the circuit. And there is no guarantee that that the designed circuit will work properly or giving better performance. It takes more time to design and implement more area for manual connections. To overcome this Compact Routing is introduced which is a automatic routing by the EDA tool which has a lot of advantages like establishing connections with less interconnect length within less time. It has a special feature i.e., Over the Cell Routing. In this routing procedure, connection made by Metal 4 for creating the contact with different metal on route. The tool will give the required Optimization for the design which includes time, design area, power consumed by the circuit, and high performance. MICROWIND is one of the Automatic Compact Routing Algorithm provided by EDA tools. This algorithm

supports DSM (Deep Submicron Technologies) like 20nm, 14nm, 7nm, technologies. As we know that, the size of the transistor channel shrinking gives opportunity to integrate more and more modules on a single chip. To design at this technology high precision EDA tools are required to accomplish the task without even minor errors. A compact routing is shown in the fi 1.6.

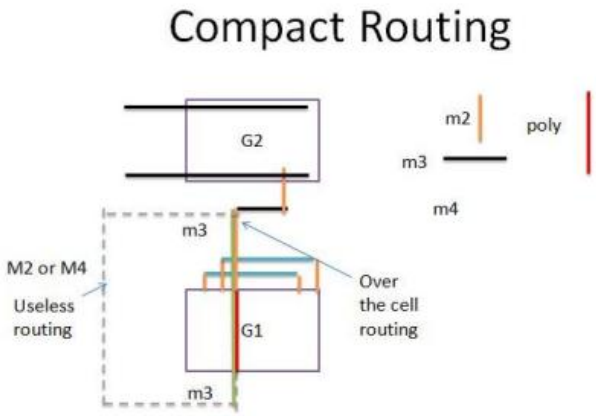

Fig 1.6. Compact Routing

IV. PROPOSED

The problem in the existed method is we are directly going to route higher metals that results stacked via and that will affect the transition time. So the drive strength will be reduced. In CTS stage we need to reduce the skew and meeting the setup and hold time. If we meet with in the timing results number of instructions per cycle will increase that means frequency will be very high. The below fig.2 represent one net.[4]

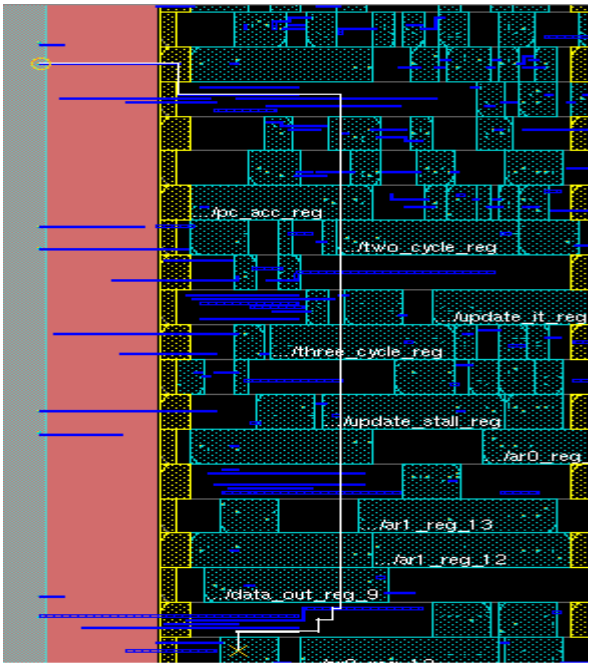

Fig 2. A net routed in Cadence Encounter

The below fig2.1 shows a single cut Via generated by tool itself and we have taken the report for that perticular net and observe the resistance ,transition time and delay as shown in below.

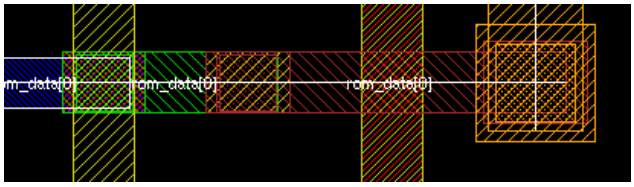

Fig 2.1 Single cut via

The below table 1 showing table, how much transition time it takes to reach from logic zero to logic one, Resistance of that particular net, and time taken to propagate a signal from one end to another end. While using such type of vias the delay little bit increased and little bit of transition time will be increased, but here we are about routing thousands and millions of nets and that results huge time delays.

	Rise	fall
Net delay	0.001400 ns	0.001400 ns
From pin transition time	0.161800 ns	0.126200 ns
To pin transition	0.246000 ns	0.191700 ns

Resistance	132.11 ohms

Table.1: Experimental results of default approach.

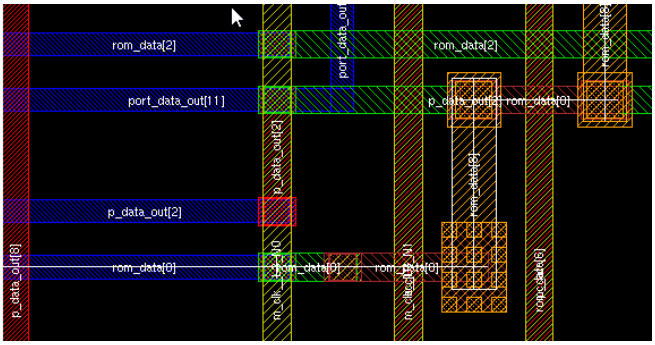

Fig 2.2 Optimized via

The below Table.2 shows the proposed method to use Via properly. Here we are utilizing the tracks properly and we are not occupying the other tracks. We uses a multicut via and increased little bit width of the Via. As we all know that resistance of a net increases with increase in length and reduce with increase width. Hera we increase the width of the via and that will reduce the resistance, transition time, delay .In this method one of the additional advantage is that utilization of that available routing resources that results reduces congestion also.[5]

	Rise	fall
Net delay	0.001300 ns	0.001300 ns
From pin transition time	0.161800 ns	0.126200 ns
To pin transition	0.245900 ns	0.191700 ns

Resistance	130.48 ohms

Table.2: Experimental results of proposed method

Here we have changed only one via, But in real design we have lot of vias. If we apply this approach then it will give good timing .

V. CONCLUSION

Now a day's Very Deep Submicron technology is popular in designing electronic gadgets, instruments, etc. So to reduce the size, increase speed, less cost, less power consumption, these are the deciding factors. And speed is one of the most requirements. Now the interconnections play a crucial role in VDSM technology. By reducing these types of issues we can achieve better designs.

VI. FUTURE SCOPE

In this paper we are concentrated on optimizing via only, but in future we try to change the type of metals used in the routing and also try to give different metal strategies.

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