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Design And Analysis Of RHBD Memory Cells And 4x4 RHBD 10T Memory Cell Architecture

M. Chaitanya, V. Kannan

Abstract: ***CMOS technology plays an important role in the modern electronics world. CMOS technology also plays significant role in aerospace applications. To store data, memories are widely used as the medium in aerospace applications. SRAM cells are the memories made by the CMOS technology. The most vital issues faced by memories are due to single event upsets (SEUs) which are induced by radiation particles. The SEU's due to increase in densities and SEU's. There is a decrease in critical charge and supply voltage in CMOS process technology. There is a need for a technique which can to tolerate these SEU's in such aerospace applications. Which are in the environment of complex celestial radiation? The technique which is considered for such environment is radiation-hardened by design (RHBD) with soft error robustness. This paper aims at is proposing an area efficient and high reliable RHBD memory cell for the above said application using 45nm technology in Cadence Tool. Depending on power, write/read time, the layout area of 14T, 12T and 10T RHBD memory cells and their performance on power for read/write operations are observed. A comparative study is also done on these memory cells based the parameters considered.***

Keywords**:** ***Architecture, CMOS, RHBD.***

I. INTRODUCTION

Memories represent the important part in modern circuit designs .SRAM plays a key role in electronic systems that are widely used as memories. SRAMs were designed using reduced delay, area, power and reliability calculation in [1].In general, SRAM cells are highly affected to reliability changes due to high densities, low critical charge and low supply voltage .In SRAM cells a particle impact can change the state of cells leading to formation of single event upset. The active particles help SRAMs in challenging with the reliability triggering. The electronic device faces the malfunctioning by a failure mechanism known as single event upsets (SEUs) by changing the pre-stored charge temporarily [2]. The transient voltage pulse is generated. When the stored value in a node was modified. By using move-coupled inverters, the 6T SRAM cell is usually built. The charge which is generated in the stored node can trigger observations mechanism, in order to turn the domain in any other responsive node when an error takes place in the memory, due to which data overwrites happens and faults occurs [3-4]. In general with CMOS technique, SRAM cells will be further liable to this reliability task due to increasing densities, reducing critical charge, and lowering supply voltage [1]. Radiation-hardened by-design (RHBD) techniques plays major role in aerospace programs and these are designed in such a way that they can suit the aerospace environment [5-6]. The conventional SEU memory designs like 10T memory cell can tolerate single event upsets at a time but they can't be good at multiple upsets at the same time [7]. To overcome multiple event upsets 12T memory cell was proposed and are effectively work in high radiation environments but consumes more power [8]. The radiation hardened 14T cell increases resilience to both single and multiple event upsets, due to the charge distribution among OFF-transistors. 14T memory cell optimizes speed and power over 12T memory cell [9].This paper is divided into the five sections. Section I is introduction, Section II explains about the different RHBD memory cell schematics with operation. In Section III, the 4×4 architecture of 10T RHBD memory cell and the performance analysis for various memory cells with write/read timings are shown. In Section IV results and discussions are done. Finally, a conclusion is presented in Section V.

II. SCHEMATIC AND OPERATION ANALYSIS

A. 10T RHBD Memory:

10T RHBD memory cell offers the best reliability and can also be used for error recovery at particular sensitive node. It provides improved write and read access time. The schematic of 10T RHBD memory cell is shown in Figure 1.

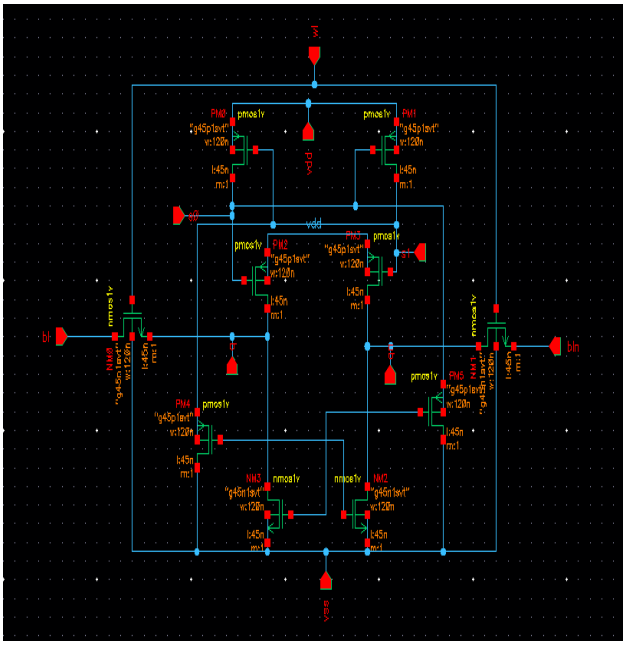

Figure 1: Schematic of RHBD 10T memory cell

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***Correspondence Author(s)**
M. Chaitanya, PG Scholar, GMR Institute of Technology, India
V. Kannan, Professor, Department of ECE, GMRIT, Rajam, India

B. 12T RHBD Memory:

12T RHBD memory cell gives higher stability and tolerates both single node and multiple nodes upsets. It calculation for area, power and read/write access time has been done. The schematic of 12T RHBD memory cell is shown in Figure 2.

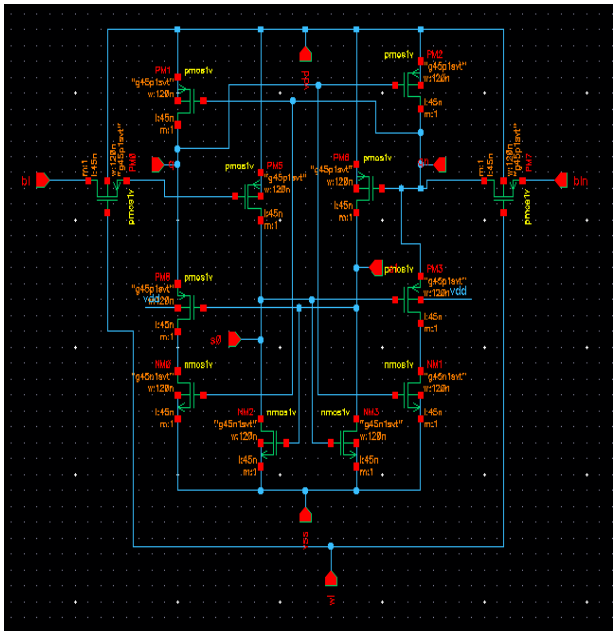

Figure 2: Schematic of 12T memory cell

C. 14T RHBD Memory:

The 14T RHBD memory cell utilizes isolation technique to achieve optimized speed and power. The schematic of 14T RHBD memory cell is shown in Figure 3.

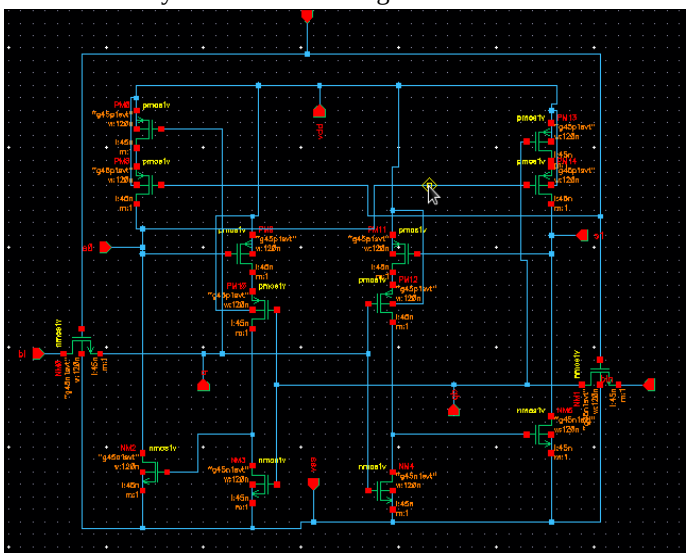

Figure 3: Schematic of RHBD 14T memory cell

III. ARCHITECTURE

A 4×4 RHBD memory is designed by using i.e.2 to 4 decoders (both row and column decoders), sense amplifier circuit and write driver circuits. The main objective of the memory design is to perform the operation of read/write the data with reduced power and delay. The 2byte architecture schematic of RHBD memory cell is shown Figure 4.

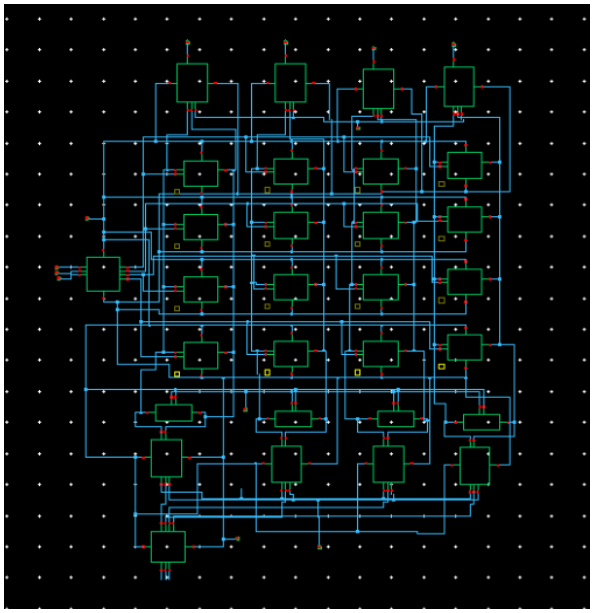

Figure 4: Schematic of RHBD Memory cell architecture

A. The Pre-Charge Circuit:

The pre-charge circuit is one of the crucial module used to perform SRAM memory operations. Pre-charge circuit is to charge Vdd=1V in both bit line and bit-line bar when PMOS gate voltage is low. The pre-charge circuit enable the memory write and read operations are performed. The schematic of pre-charge circuit is shown in Figure 5.

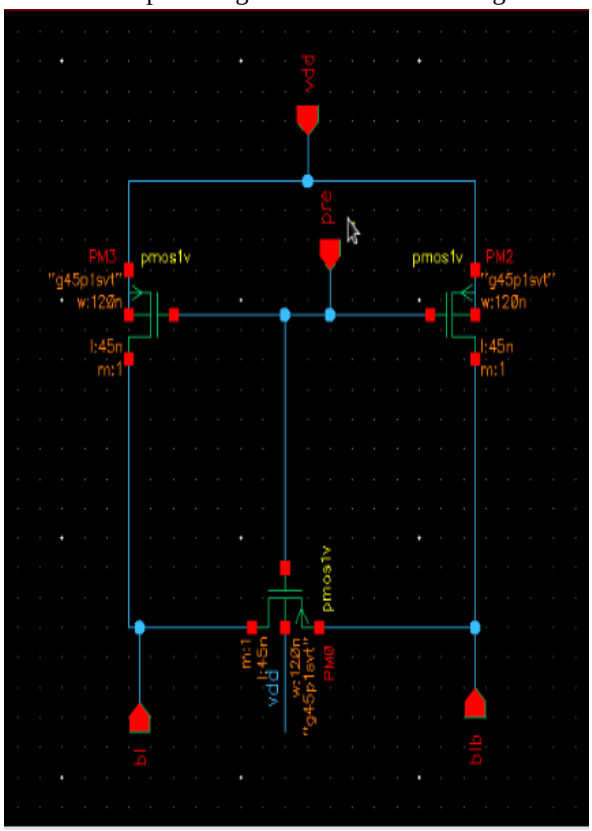

Figure 5: Schematic of Pre-charge circuit

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B. Row Decoder:

The block diagram for the N: 2^N decoder and its connected circuitry are mentioned in the above diagram. Essentially, the decoder selects only one among 2^N outputs, as according to the deal with input lines. The decoder output is given to the rows of SRAM cells, in according to the given N- bit address. Row decoder selects one of the memory rows and can be designed with the help of common logic gates.

C. Column Decoder:

For analyzing the data or to regulate its contents, the column decoder chooses a specific column inside the memory array of the chosen cell. Similar to the row decoder, the column selector is also choosing a particular column.

D. Write-Driver Circuit:

The write-driver circuit discharges one of the bit lines i.e., bit line bar or bit line from the pre-charge circuit value which is in the write noise margin of the SRAM memory design. Usually, the write driver circuit is operated with Write Enable (WE) signal of the design to discharge and drives the bit line to ground from the precharge level. Write-driver circuit is designed by using two pass transistors and AND gates. The schematic of write-driver circuit is shown in Figure 6.

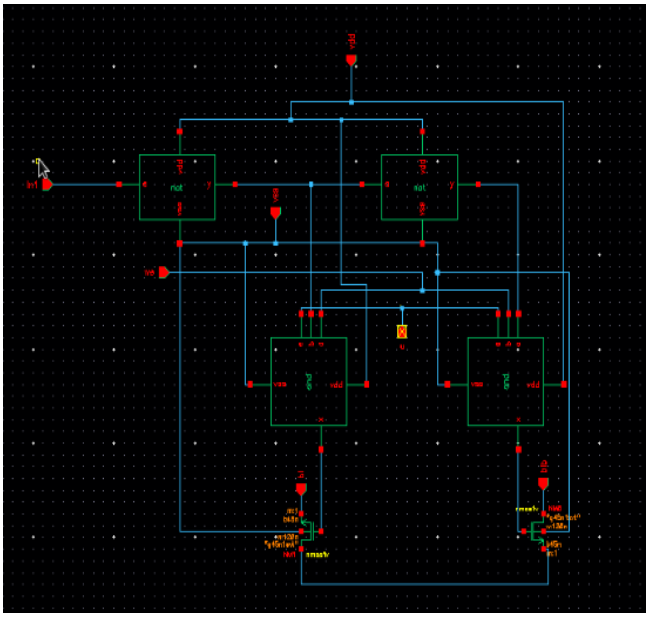

Figure 6: Schematic of write-driver circuit

E. Sense Amplifier:

Sense amplifier (SA) circuit in SRAM memory architecture is used to perform bit line sense operation. Differential voltage is generated by the precharge circuit at the bit lines by significantly reducing the operational time. The principle of the sense amplifiers on each pair of bit lines is to turn the weak signal into a normal logic signal that can then be fed to additional data multiplexers and/or I/O pin drivers. The schematic of Sense Amplifier is shown in Figure 7.

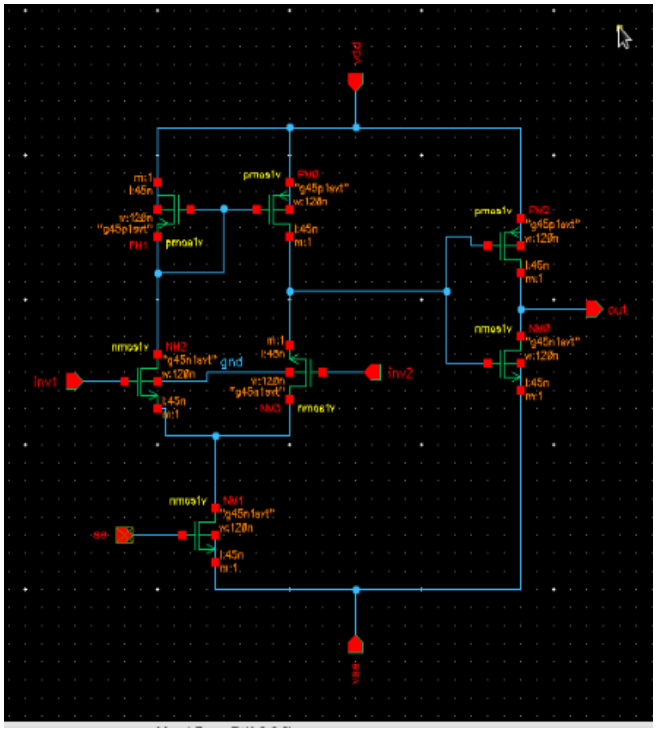

Figure 7: Schematic of Sense Amplifier

IV. RESULT AND DISCUSSION

This Section presents the simulation results of 4x4 memory architecture, 10T RHBD memory, 12T RHBD memory, and 14T RHBD memory. Cadence virtuoso tool is used to simulate all the mentioned designs with the 45nm technology libraries. Figure 8 shows the transient response for read and write operations in 4x4 memory arrays.

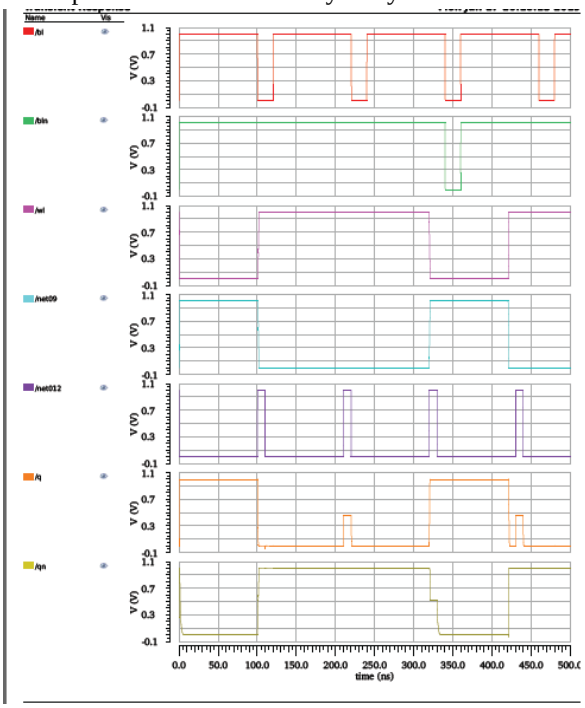

Figure 8: Simulation results of 10T RHBD Memory

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Figure 9 shows the 12T RHBD memories cell. It also shows the write 0, write 1, read 0, and read 1 operation and its simulation results.

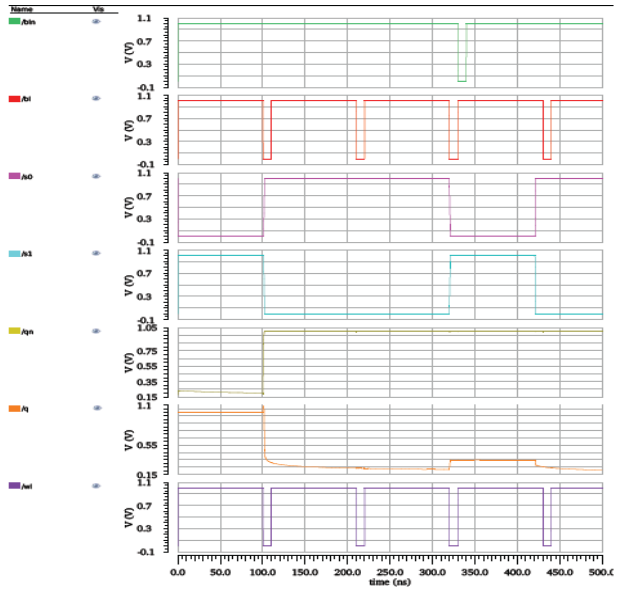

Figure 9: Simulation results of 12T RHBD Memory

Figure 10 shows 14T RHBD memory cell. It also shows the write 0, write 1, read 0 and read 1 operation and its simulation result. The parameter values obtained for different memory cells are shown in table 1.

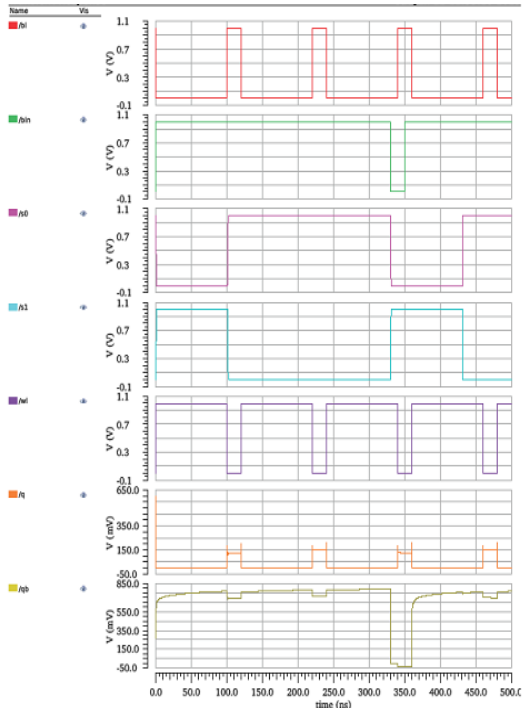

Figure 10: Simulation results of 14T RHBD Memory.

PARAMETERS COMPARISONS:

The table 1 shows the values of the different memory cell parameters**.**

Table 1: Different memory cells parameter values

PARAMETERS	10T RHBD memory	12T RHBD memory	14T RHBD memory
AREA(µm²)	6.89	7.12	8.26
POWER(nW)	20	38.9	55.6
DELAY(µs)	2	4.12	6.24

The parameters considered for the analysis are discussed below.

A. AREA:

The area for the memory designs are compared and shown below in Figure 11. The areas of different RHBD memory cells are 6.89, 7.12 and 8.26 in terms of micro square meters. It is observed that 10T memory cell is occupying less area and 14T memory cell is occupying more area.

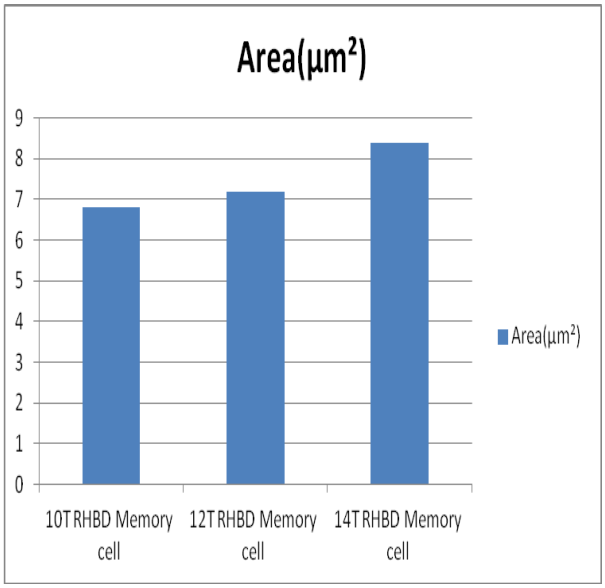

Figure 11: Area results of different RHBD Memory cells

B. POWER:

The power dissipation in different memory cells are shown in figure 12. The RHBD 10T memory cell exhibits low power dissipation than other hardened memory cells. The dissipation of power in the 10T memory cell is low is due to the usage of less PMOS transistors when compared with 12T and 14T cells. The power for the memory designs are also compared and shown in Figure 12.

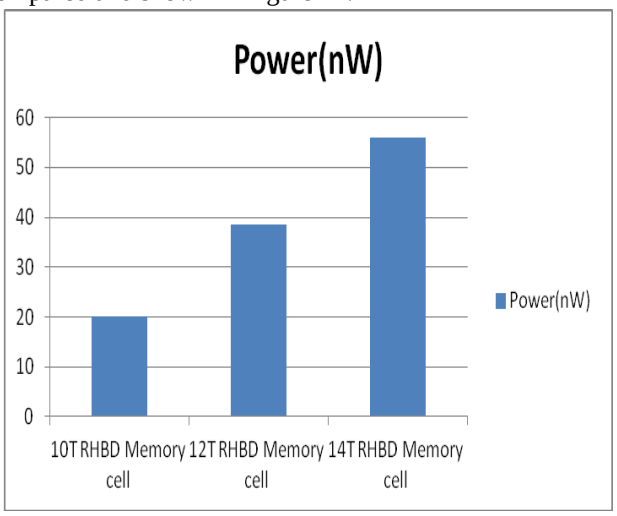

Figure 12: Power results of different RHBD Memory cells

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C. DELAY:

The delay occurred in different memory cells are shown in Figure 13. RHBD 10T memory cell exhibits less delay than other radiation hardened memory cells. The delay of the 10T memory cell is less since less number of transistors are used when compared with other memory cells.

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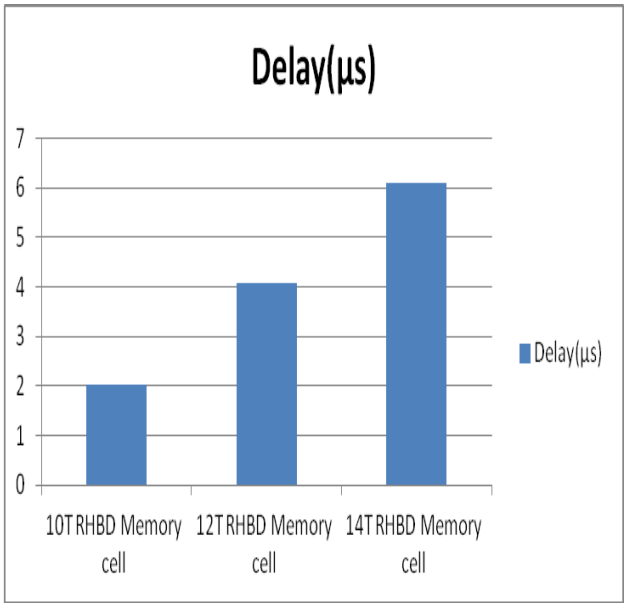

Figure 13: Delay results of different RHBD Memory cells

D. READ AND WRITE OPERATION OF 4*4 MEMORY ARCHITECTURE:

The 10T RHBD memory architecture parameter results are shown in figure 15. The output voltage in 4*4 memory architecture is low when bit and bit bar inputs are at low voltages. When d0 and d3 changes from high to low and low to high, the memory cell's read operation is observed. In write operation, when the write enable gets on after that the data goes high from low to high and then remains constant, which shows that the data is being read by the memory cell. The 10T RHBD memory architecture parameter values are below shown in table 2.

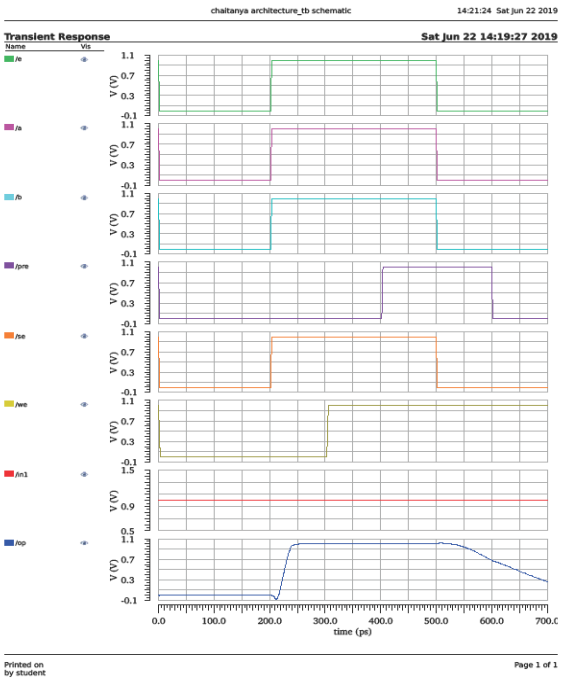

Figure 14: Simulation results of 10T RHBD Memory Architecture.

Table 2 shows the parameters of the 10T RHBD memory architecture.

Table 2: 10T RHBD memory architecture parameter values

PARAMETERS	AREA (μm^2)	POWER (nW)	DELAY (µs)
10T RHBD memory cell architecture	**210.9**	**50**	**415**

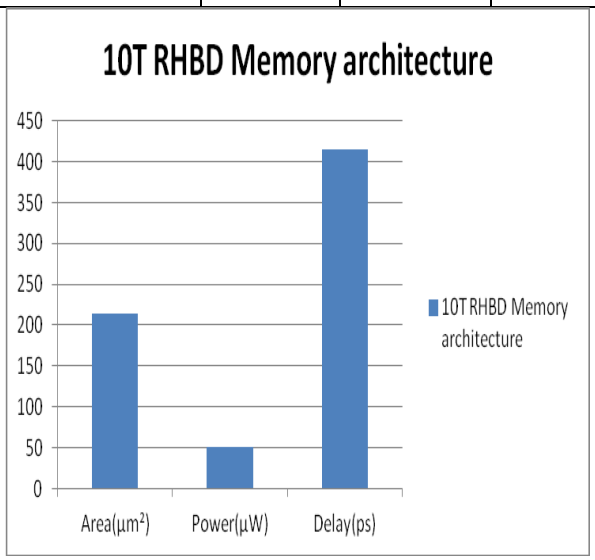

Figure 15: Parameter results of 10T RHBD Memory architecture

V. CONCLUSION

In harsh environments, general memory cells suffer with soft errors caused due to high energy particles. In order to overcome these soft errors like single event upsets and multiple event upsets, the radiation hardened designs with 10T, 12T and 14T memory cells are used. The performance comparison analysis of single event upsets to multi event upsets, are performed. The use of 10T cell increases the robustness of the memory cell design. Compared all the radiation hardened memory cells, 10T memory cells exhibits less in area, power and delay. A 2 byte RHBD memory is designed using 10T memory cells. This memory architecture can be implemented in any high radiation environment.

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AUTHORS PROFILE

Mudadla Chaitanya received his Bachelor Degree in Electrical and Electronics Engineering from Sri Sivani College of Engineering in the year 2017, Master's Degree from GMR Institute of Technology in the year 2019. His main research areas are Analog VLSI design.

Dr.V. Kannan received his his Bachelor Degree in Electronics and Communication Engineering from Madurai Kamarajar University in the year1991,Master's Degree from BITS, Pilani in the year 1996 and Ph.D., from Sathyabama University, Chennai, in the year 2006. His interested areas of Research are Optoelectronic Devices, VLSI Design, Nano Electronics, Digital Signal Processing and Image Processing and Wireless Sensor Networks. He has more than 220 Research publications in National/ International Journals/ Conferences to his credit. He has 28years of experience in teaching and presently working as Professor in GMR Institute of Technology, Rajam, Andhra Pradesh, India. He is a life member of ISTE.