

# Effect of Latitudinal and Longitudinal Grain Boundaries on the characteristics of Polycrystalline Silicon MOSFET Devices

Kiran Sharma, Tarun Kumar Dhiman, Pankaj Negi, D. P. Joshi

**Abstract:** The MOSFETs, Complementary MOS-ICs are the core switch devices of current which also critically affects the ICs. For higher IC performance the present era has shifted to the device scaling to sub-50nm range TFT (thin film transistor) based MOSFET which involves complex fabrication process. The presence of grain boundaries greatly affects the characteristics of these devices. Present paper describes dependence of output characteristics in polycrystalline silicon MOSFET devices on the longitudinal and latitudinal grain boundaries (GBs) have been investigated theoretically. It is observed that in both latitudinal and longitudinal GBs, the GB scattering potential ' $q\phi$ ' and the GB distribution parameter ' $s$ ' are equally involved. At all values of gate voltages the contribution in drain current of the device is more due to latitudinal GBs in comparison to longitudinal GBs. However, at high gate voltages longitudinal GBs play a significant role in the drain current of the device. The theoretical computations of the model are synonymous to the experimental work.

**Keywords:** longitudinal, GBs, MOSFET, MOS-ICs.

## I. INTRODUCTION

MOSFET is the most widely used semiconductor device in digital and analog monolithic integrated circuits. MOSFET technology is also used for very large scale integrated circuits. Recently, the device parameters size has been reduced down into the deep sub 50nm range. The sub-0.1  $\mu\text{m}$  technology node for complementary MOSFET is used for many large scale ICs which shows a commensurate rise in speed and in integration scale [1, 2]. Recently Yoon et al [3] presented a study on dual gate based poly-Si 1T-DRAM cell which consists of huge number of intrinsic grain boundaries (GBs). A separate storage region is used for accumulating charges in the trap states. The characteristic of the fabricated device were also studied with temperature variation. Many studies [4-8] are proposed for scaling down the dimension, so as to examine the short-channel effect of poly-Si TFT. The unsymmetrical source/drain doping type is considered to build the tunnel field-effect transistor (TFET). The poly-Si TFET shows high short-channel effect immunity and low device variation due to its novel carrier transport phenomena: interband tunneling.

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However, high threshold voltage ( $V_T$ ), low On-current ( $I_{ON}$ ), gentle sub threshold slope and immense leakage current in TFTs and MOSFETs is restricted by the tremendous amount of randomly arranged grain boundaries (GBs) present in the channel [9-10].

Experimental results [11] show that the stability of the devices depends on the grain boundaries and the presence of impurities such as hydrogen, oxygen and others. The exponential law is governing the threshold voltage during the gate bias stress which is linked to the disordered structure. Moreover the inconstant behaviour of grain arrangement results in important device-to-device variation, hence weak circuit yield. MILC technique film are reported to have better device performance since the arrangement of the grain boundaries is also inconstant, but match in the direction of propagation order of the recrystallization agent [12]. Due to effect of grain boundaries the output parameters can be enhanced. Usually both types of GBs parallel and perpendicular along with flow of current are present in the channel zone of the device.

Jagar et al. [13] carried an experimental study on the behaviour of N-MOSFET constructed on large-grain PX-Si film considering the result of longitudinal and latitudinal GBs. They found that MOSFETs built on large-grain polysilicon-on-insulator (LPSOI) film carried the fusion of only longitudinal or latitudinal GBs. In correlation to latitudinal GBs that give more resistance to the inversion carriers, the longitudinal GBs add extra leakage current result in less effect on the flow of current. Chen et al. [14] investigated a model for polycrystalline silicon thin film transistor to study the performance of grain boundaries on the transfer behaviour of TFTs. Concentration is only on the number and the width of grain boundaries in the channel space and determined the transport phenomena of carrier over grain boundaries.

Jagar et al. [15] experimentally performed the effect of grain boundaries result on the efficiency of the MOSFET built on large-grain polysilicon-on-insulator (LPSOI), film of grain size varied from 10 to 100  $\mu\text{m}$  were taken. They observed that the parallel GBs source of large leakage current in the off-state and show minimum impedance to the conduction carriers; hence the simultaneous GB's devices are regulating the high drive current, low threshold voltage, and steep sub threshold slope. The perpendicular GBs in the channel spacer result in high impedance to the conduction carriers that result in more threshold voltage, lower current drive, and gentle sub threshold slope.



Gupta and Tyagi [16] studied the carrier transport through diagonal and longitudinal grain boundaries (GBs) in polysilicon thin film transistors (poly-Si TFTs) by considering a matrix of square grains in the channel region. Barletta and Ngwan [17] analyzed the transport carrier process through the polyoxide layer by the Frenkel–Poole model. Through Frenkel–Poole model it is found that the trapped charge density inside polyoxide layer is liable for the barrier height decrement and the gate current leakage decrement after gate voltage pulse. Dutta and Kundu [18] studied theoretically the drain current in MOSFET device at different doping concentration of polysilicon gate region due to the presence of only latitudinal grain boundary height.

The present literature on PX-Si MOSFETs proved that, no study is carried to explain effect of carrier transport mechanism through diagonal and latitudinal grain boundaries on the drain current. In the present work, the authors have extended their conduction model developed in [19] to further investigate the outcome of diagonal and latitudinal grain boundaries on the device characteristics of MOSFET (n-TFT) devices.

## II. THEORY AND DISCUSSION

Conventional TFTs contain randomly oriented GBs in the channel region, however analysis shows that [13] if TFTs are built by high temperature MILC technique on massive grain polysilicon-on-insulator (LPSOI) film then the GBs align along the recrystallization agent and their orientation of is no longer random. These fabricated MOSFETs contain the combination of only parallel or perpendicular GBs. According to the study of Jagar et al. [13] GBs parallel in the direction of flowing current has less affect to the flow of current and the performance of the device can be improved. The low leakage current and high mobility are desirable in TFT/MOSFET devices. However, the performance of MOSFET/TFT devices is limited by the random orientation of GBs existing in the channel. Many workers [13-15] have studied the effects of longitudinal GB existing in the channel. Jagar et al. [13] observed that when channel width reaches a level the leakage current in these devices increases rapidly it also depends at the average grain size of the LPSOI film. They also found that longitudinal GBs, as compared to the latitudinal GBs, have a less affect at the long channel devices and shows better ideal device performance. If both types of GBs parallel and transverse to the channel length are present, then the total current will have two components via current passing through the grain interior and across GBs ( $I_{D\perp}$ ), and current passing along disordered GB ( $I_{D\parallel}$ ). These two components are expressed by

$$I_{D\perp} = \left( \frac{\mu^* Z' \epsilon_{ox}}{L} \right) [(V_{GS} - V_T) V_D], \quad (1)$$

$$\text{And } I_{D\parallel} = \left( \frac{\mu_{\parallel}^* W_{\parallel} \epsilon_{ox}}{L} \right) [(V_{GS} - V_T) V_D], \quad (2)$$

where  $Z$  is the channel width,  $W_{\parallel}$  ( $=N' \delta$ ) is the total width of GB regions parallel to the channel,  $Z'=(Z-N'\delta)$  is the width of the channel for perpendicular GBs in the presence of GBs parallel to the channel length,  $\mu^*$  is the effective movability for a carrier going through the grain interior and across the GB,  $\mu_{\parallel}$  is the mobility for a carrier passing along a GB, and  $N'$  ( $=Z/d_{eff}$ ) is the count of parallel GBs present in the space. Here  $d_{eff}$  is the effective grain size. Note that author has assumed that the GBs are along the full length of the device. It is also assumed that carrier distribution is uniform throughout the channel of the device. Under this condition, the total current in the MOSFET device is the sum of the two components

$$I_D = I_{D\parallel} + I_{D\perp} \quad (3)$$

On substituting Eqns. (1) and (2) in Eqn. (3) we get,

$$I_D = \left( \frac{\epsilon_{ox}}{t_{ox} L} \right) [(V_{GS} - V_T) V_D] \left[ \mu^* Z + (\mu_{\parallel} - \mu^*) \left( \frac{Z \delta}{d_{eff}} \right) \right]. \quad (4)$$

If GBs traverse perpendicular to the channel region, the measured carrier mobilities are found to be  $320 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $255 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  respectively [13].

$$\sqrt{\frac{8\epsilon V_g C_{ox} (V_{GS} - V_T + \gamma V_m)}{t_{si}}} = \int_{E_T - s/2}^{E_T + 3s/4} \frac{q N_g s \exp\left(\frac{-(E - E_T)^2}{2s^2}\right) dE}{(\sqrt{2\pi} s) \left[ 1 + 2 \exp\left(\frac{E_F + E + qV_g}{kT}\right) \right]} \quad (5)$$

This equation is used to study  $qV_g$  as a function of gate voltage [19].

The space charge potential barrier height PX-Si MOSFET device is calculated using Eqn. (5). The calculated variation of  $qV_g$  with  $V_{GS}$  and  $T$  (K) is shown in Fig.1 and 2. It is observed that  $qV_g$  decreases on increasing the gate voltage and the device temperature. This dependence of  $qV_g$  on  $V_{GS}$  is due to the increase in carrier density in the vicinity of the device.

Fig. 3 illustrate the change of drain current as a variable of gate voltage for PX-Si MOSFET device on considering effect of both latitudinal and longitudinal GBs. It is clear from the plot that the theoretical computations of author's model are synonymous to the experimental work of Jagar et al. [13]. The parameters used in Figs. 3 are listed in Table 1. It is found that effect of 'qφ' and 's' are same in both latitudinal and longitudinal grain boundaries, both parameters do not depend on grain size and doping density, however they show dependence only on temperature. From the present study it is clear that at all values of gate voltage the contribution in drain current of the device is more due to latitudinal GBs in comparison to longitudinal GBs. However, longitudinal GBs play a significant role in drain current at high gate voltages.

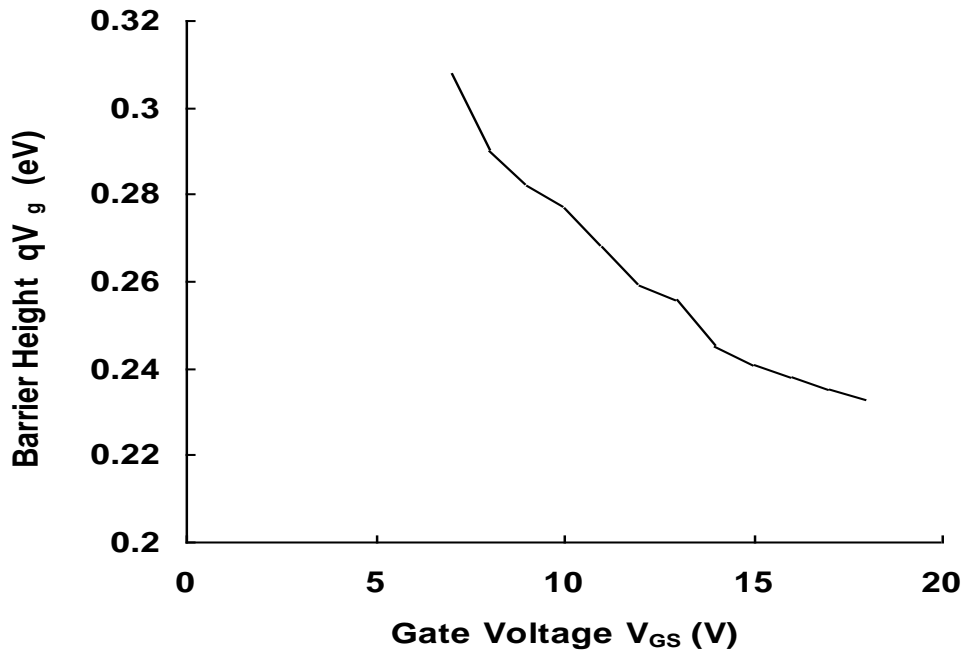


Fig.1 Computed variation of barrier height versus gate voltages for PX-Si MOSFETs.

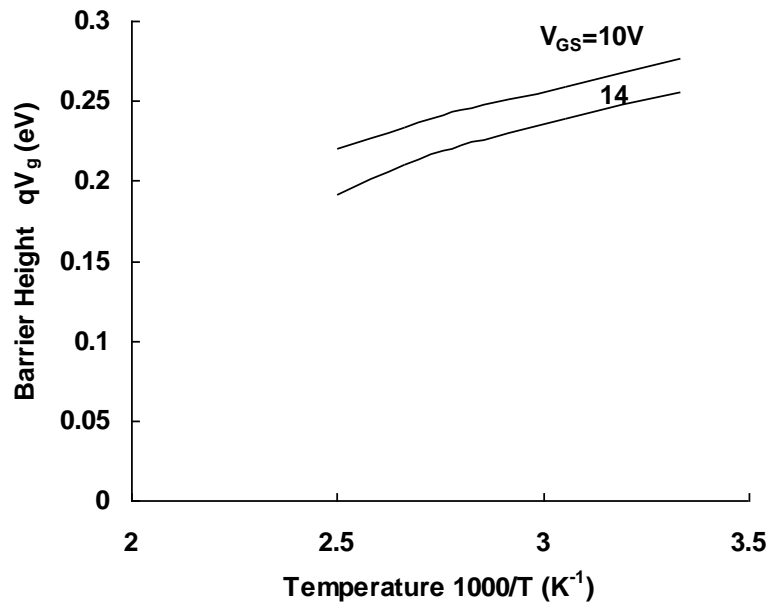


Fig. 2 Computed variation of barrier height at different temperatures for PX-Si MOSFETs

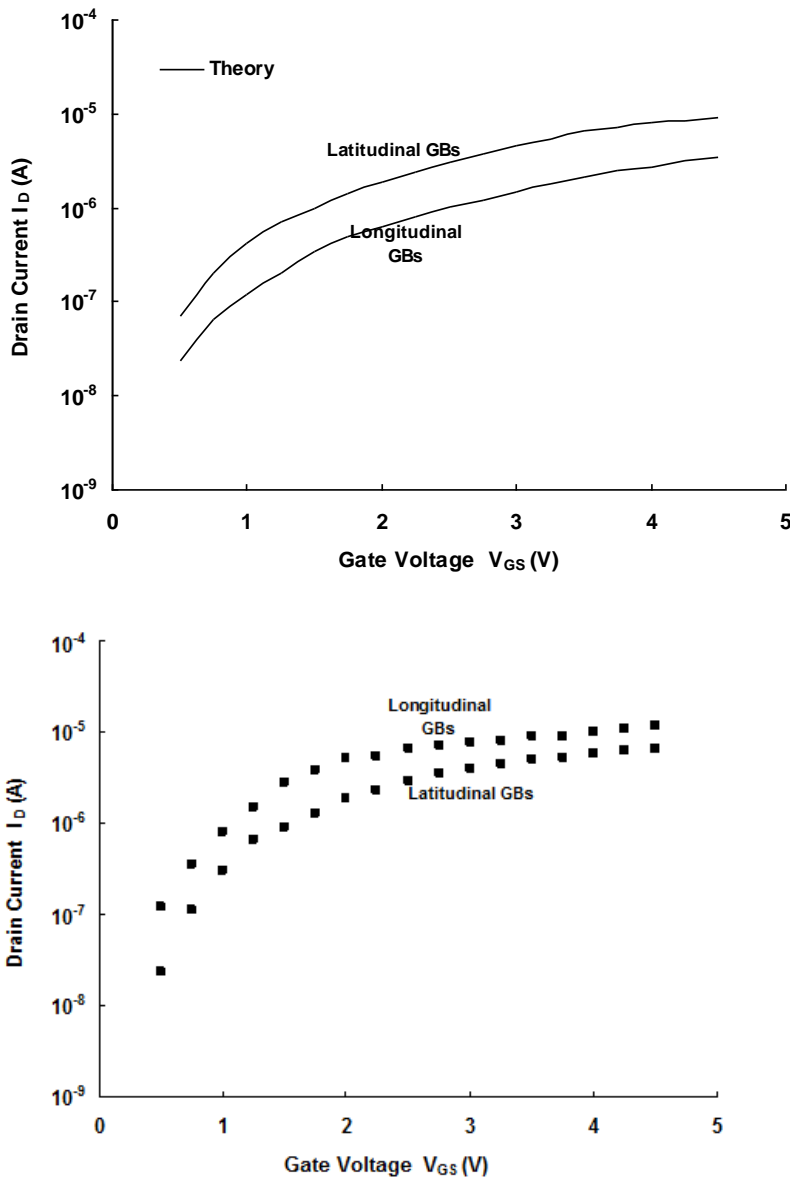


Fig. 3 (a) Calculated variation of drain current with  $V_{GS}$  for latitudinal and longitudinal GBs. (b) Experimental results for dependence of drain current with  $V_{GS}$  for latitudinal and longitudinal GBs of Ref. [13].

Table 1: List of parameters in proposed theoretical model

Parameters	Ref. [13] Fig. 3	
	Longitudinal GBs	Latitudinal GBs
d	100000 nm	100000 nm
T	300K	300K
$N_{gs}$	$3 \times 10^{12} \text{cm}^{-2}$	$5 \times 10^{12} \text{cm}^{-2}$
$E_T$	0.1eV	0.15eV
q $\phi$	0.1(eV)	0.1
s	4.0kT	4.0kT
$\delta$	20 Å	20Å

### III. CONCLUSIONS

If both types of GBs parallel and transverse to the channel length are present in the MOSFET device then the total

current will have two components viz current passing through the grain interior and across GBs ( $I_{D\perp}$ ), and current passing along the disordered GBs ( $I_{D\parallel}$ ). At all values of gate voltages the contribution in drain current of the device is more due to latitudinal GBs in comparison to longitudinal GBs, but on the other hand the presence of longitudinal GBs cannot be neglected since at high gate voltages they plays a vital role in the drain current of the device. The potential ‘q $\phi$ ’ and parameter ‘s’ are same in both latitudinal and longitudinal GBs.

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