International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-8 Issue-11, September 2019

FDTD modeling for Crosstalk Reduction in Coupled RLC Interconnects with Active Shielding

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Abstract—This paper presents efficient geometry for crosstalk noise and delay reduction using Active shielding in RLC interconnects with resistive drivers .FDTD modeling has been used for proposed geometry and is validated by HSPICE simulations for 32nm global interconnects .From the results it has been verified that the proposed model results and HSPICE simulations differ by 5% . From the outcomes it has been confirmed that the proposed model outcomes and HSPICE outcomes differ by 5% and by using proposed geometry crosstalk noise and delay has come down by 73% and 60% when compared to unshielded line.

Index Terms—Crosstalk noise, Delay, Active shielding RLC interconnects, FDTD

I. INTRODUCTION

Crosstalk is one of the significant structure worries in current time of Large Scale Integration and nano scale interconnectors because it causes unwanted voltage variations on bus line due to transition on bus lines placed adjacent to each other and lead to performance degradation by inducing delay on interconnects. Delay due to crosstalk depends on several factors such as coupling capacitance, relative driver strength because of crosstalk relies upon a few factors, for example, coupling capacitance, relative driver quality h and on transition time skew. Due to Scaling of devices and increase in chip size and density according to ITRS-2009 interconnect delay is more when compared to gate delays[16] Further, crosstalk may result in undesired potential glitch on a interconnect line due to transition in one or more bus lines adjacent to each other. Therefore, reliability has become a major concern of crosstalk effect.

Crosstalk noise in coupled interconnects is classed into two categories as functional and dynamic crosstalk. A victim line experiencing a voltage spike when an aggressor line switches is defined as Functional crosstalk.

Manuscript published on 30 September 2019.
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On the other hand, dynamic crosstalk is observed when aggressor and victim line switches in out-of-phase or in-phase simultaneously resulting in changes in signal propagation delays. Furthermore, interconnect parasitic like capacitance, resistance and inductance also influence crosstalk delay largely. Thus to evaluate the performance of interconnects accurately, the interconnects should be treated as distributed RLC interconnects.

Distributed RLC interconnects with resistive drivers suffers from frequency to time domain problems, because partial differential equations are used for describing the transmission lines and solution is given in frequency domain Where as nonlinear elements are described only in time domain and this problem can be addressed by using FDTD(finite difference time domain) technique.

In this paper we focused on reducing crosstalk noise and delay, induced due to switching on adjacent lines in RLC interconnects by using active shielding technique. Crosstalk effects are analyzed on coupled three lines with and without shielding. The exemplar proposed takes into transmission line effects of interconnects which include mutual capacitance and mutual inductances into consideration and the coupled interconnect lines are modeled by FDTD technique. The proposed exemplar is validated using HSPICE and the uttermost erroneous between FDTD and HSPICE transient response for 32nm technology is hardly 4%. The repose of the paper is organized as follows: section II describes proposed active shielding geometry to couple interconnects. Section III describes FDTD model for coupled three interconnect lines. In section IV the proposed exemplar is validated by HSPICE and section V concludes the report

II. ACTIVE SHIELDING PROPOSED MODEL FOR COUPLED INTERCONNECT LINES

Interference of signals between adjacent interconnects leads to functional errors. Due to scaling of device sizes and multi layer interconnect structures coupling capacitance and inductance has become major issue for signal integrity and accuracy. Techniques like encoding data bits to reduce switching activity, buffer insertion, increasing wire length and width, increasing spacing between lines and shielding has been proposed to reduce crosstalk [4] Crosstalk noise and delay in coupled RLC interconnects can be reduced effectively by using active shielding .The only limitation is increase in area. According to Miller effect, the basic conception of active shielding is that if transitions on adjacent lines take place in same direction simultaneously ,then the coupling capacitance seen between the interconnects will be zero

The geometry of Coupled interconnect lines driven by resistive drivers with and without shielding as been shown in Figs 1 and 2.[5].Here R,L,C are line resistance ,inductance

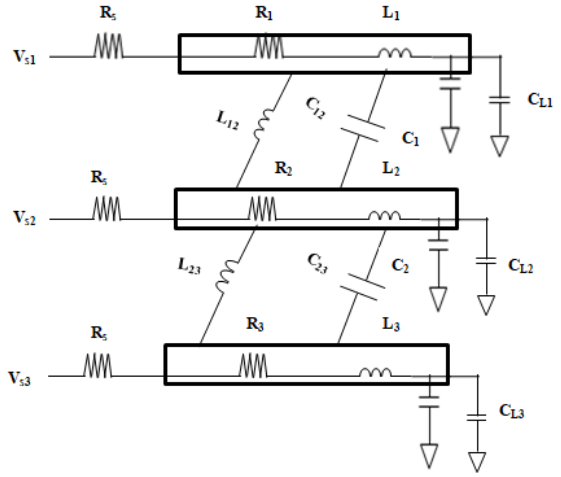

Fig.1.Coupled three line RLC Interconnects with resistive driver

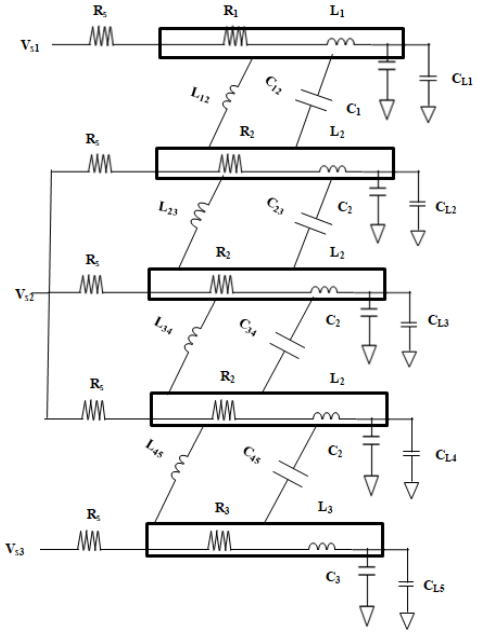

Fig.2.Coupled three line RLC Interconnects with Active shielding

and capacitances per unit length and mutual inductance and coupling capacitance between the interconnects are represented as Cc and L_M. The middle line in shielding geometry is used for transmission of signal and the peripheral lines above and below the middle line act as shields. Care has been taken to ensure that peripheral lines have same input signal and same parasitic elements as that of middle line to ensure proper synchronization between the lines.

III. PROPOSED FDTD MODEL

The Coupled RLC interconnect lines are modeled by FDTD technique [6].Interconnect lines has resistive drivers at the input and are terminated by capacitive loads. Resistance, capacitance and inductance values are defined per unit length. x is used to denote the position along the interconnect line and t represents time. Line resistance are represented as R_1,R_2,R_3 ,Line capacitance as C_1,C_2,C_3 and line inductance as L_1,L_2,L_3.Coupling capacitances and mutual inductances are denoted as C_{12},C_{23},L_{12},L_{23} and C_{L1},C_{L2},C_{L3} represent load capacitance.

Telegraphers equations for interconnect lines with active shielding in TEM mode are given as

$$\frac{d}{dx}V(x,t) + RI(x,t) + L\frac{d}{t}I(x,t) = 0 \qquad (1)$$

$$\frac{d}{dx}I(x,t) + \frac{d}{dt}CV(x,t) + GV(x,t) = 0 \qquad (2)$$

V,I are line voltages represented by 3 x1 column vectors and 3 x3 matrix of p.u.l is used for representing the parasitic elements as

$$V = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix},\ I = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}, R = \begin{bmatrix} R_1 & 0 & 0 \\ 0 & R_2 & 0 \\ 0 & 0 & R_3 \end{bmatrix},$$

$$L = \begin{bmatrix} L_{11} & L_{12} & L_{13} \\ L_{21} & L_{22} & L_{23} \\ L_{31} & L_{32} & L_{33} \end{bmatrix},$$

$$C = \begin{bmatrix} C_{11}+C_{12} & -C_{12} & C_{13} \\ -C_{21} & C_{22+}C_{12}+C_{23} & -C_{23} \\ C_{31} & -C_{32} & C_{33+} \end{bmatrix}$$

The equations are analyzed using Central differential approximation. As seen in Fig.3 for better accuracy With FDTD modeling the voltages and currents nodes are placed alternatively are separated by $\Delta x/2$ times in space and by $\Delta t/2$ times on time axis

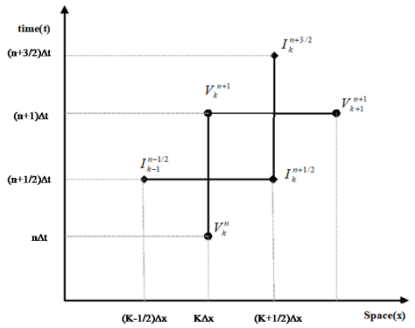

Fig.3.Discritized voltage and current nodes with respect to space and time

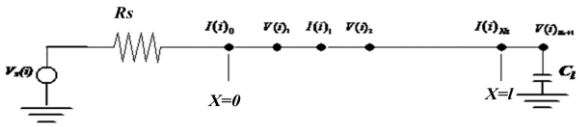

Fig.4.Discretized line in space for FDTD analysis

The Fig.4.repsents the interconnect line of length L driven by resistive driver at x=0 and terminated by capacitive load at x=l. Differential equations (1) and(2) are discretized with respect to time and space to implement FDTD analysis. length of transmission line is divided into Nl sections, each of Δx length and total time into Nt segments ,each of Δt length . Relation between current and voltage with respect to space and time is as shown in fig3

On applying finite difference approximations to (1) and(2) gives

$$\frac{V_{k+1}^{n+1}-V_k^{n+1}}{\Delta x} + L\frac{I_k^{n+3/2}-I_k^{n+1/2}}{\Delta t} + R\frac{I_k^{n+3/2}+I_k^{n+1/2}}{2} = 0 \qquad (3)$$

for K =1, 2, 3, ……., *Nl*

Retrieval Number: J11000881019/19©BEIESP
DOI: 10.35940/ijitee.J1100.0981119
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$$\frac{I_k^{n+1/2}-I_{k-1}^{n+1/2}}{\Delta x}+C\frac{V_k^{n+1}-V_k^n}{\Delta t}+G\frac{V_k^{n+1}+V_k^n}{2}=0$$

(4)

for K= 2, 3, 4, …….., *Nl*, where voltage and current are denoted as

$$V_i^j = V[(i-1)\Delta x, j\Delta t] \ , \quad I_i^j = I[\left(i-\tfrac{1}{2}\right)\Delta x, j\Delta t]$$

(5)

Thus from (3) and (4) the current and voltages at different segments along the interconnect line can be represented as

$$V_k^{n+1} = FV_k^n + \frac{E}{\Delta x}(I_{k-1}^{n+\frac{1}{2}} - I_k^{n+\frac{1}{2}}) \qquad (6)$$

for K =1, 2, 3, ……., *Nz*

$$I_k^{n+3/2} = ABI_k^{n+1/2} + \frac{A}{\Delta x}(V_k^{n+1} - V_{k+1}^{n+1}) \qquad (7)$$

for K= 2, 3, 4, …….., *Nz*

$$E = \left[\frac{C}{\Delta t}+\frac{G}{2}\right]^{-1} \ , \quad F = \left[\frac{C}{\Delta t}-\frac{G}{2}\right] \ ,$$

$$A = \left[\frac{L}{\Delta t}+\frac{R}{2}\right]^{-1} \ , \quad B = \left[\frac{L}{\Delta t}-\frac{R}{2}\right]$$

Equations (6)and (7) can be used to estimate current and voltages, further can also be extended to multiple transmission lines The voltage and current at near-end point of interconnect in discretized form can be given as

$$V_1^{n+1} = HJV_1^n + HK(V_s^n + V_s^{n+1}) - 2HKR_sI_1^{n+1/2} \qquad (8)$$

Where $H=(U+K)^{-1}$, $J=(EF-K)$, $K=E/\Delta xR_s$

At far end currents and voltages terminated by capacitive load in discretized form can be expressed as

$$I_l^{n+1} = C_l\left[\frac{V_{Nl+1}^{n+1}-V_{Nl+1}^n}{\Delta t}\right] \qquad (9)$$

$$V_{Nl+1}^{n+1} = Q_1Q_2V_{Nl}^n + \frac{2E}{\Delta x}\left[I_{Nl}^{n+1/2}\right] \qquad (10)$$

Where $Q_1 = \left[1+\frac{2EC_l}{\Delta t\Delta x}\right]^{-1}$, $Q_2 = \left[EF-\frac{2EC_l}{\Delta t\Delta x}\right]$

Assement starts with evaluating voltage along the line starting from x=0 at particular time step in terms of previous current and voltage values and current is evaluated from voltage and current values from previous time step. Accurate solutions using FDTD method are obtained only when the position and time discretization satisfy the Courant condition $\Delta t \le \frac{\Delta x}{V}$ Where V represents velocity of signal on line. The second point to be considered is the spacial increments Δx should be small enough to obtain good resolution [7],[8]

IV. VALIDATION OF THE PROPOSED MODEL

Validation of the model proposed is done by estimating the results with HSPICE simulations, carried out in W element simulation tool. Same parasitic for interconnect lines as that in proposed model are maintained for HSPICE. Coupled three lines with shielding as shown in Fig.2 is considered for validation. Crosstalk noise and delay are measured at the output node of victim line 2. Functional crosstalk and dynamic crosstalk effects [9] are estimated using resistive driver and capacitor load as shown in the Fig.4.

Crosstalk effects are also compared on victim line2 of proposed active shielded coupled interconnect with unshielded coupled interconnects based on the transient waveforms considered at the far end terminal of line2, using various other methods for crosstalk reduction such as widening and increasing the space between interconnects

V. RESULTS

As can be seen from the transient response the improvement in crosstalk noise with the proposed model has been by 73% and delay has come down by 60% when compared to unshielded coupled lines. The improvement using shielding is considerably good even when we compare the values with other reduction technique like widening and increasing the lengths of interconnects

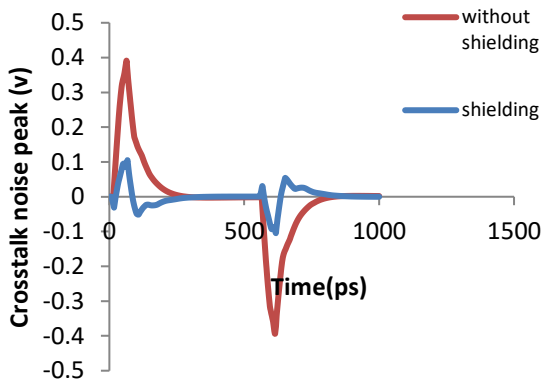

Fig.5. Crosstalk noise on interconnects

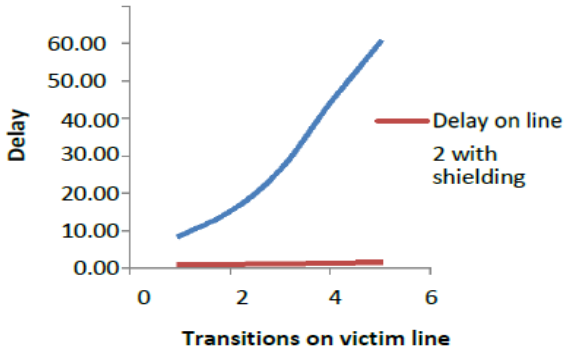

Fig. 6..Delay on interconnects

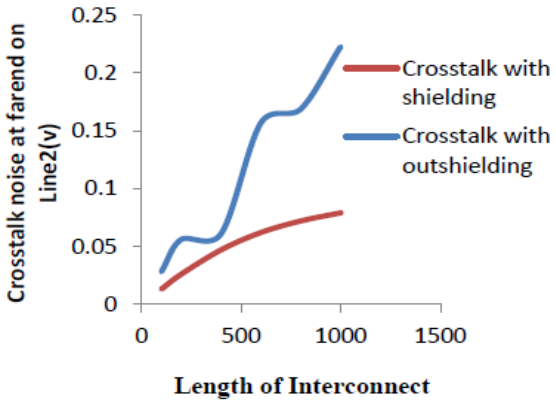

Fig. 7.Crosstalk noise peak for global interconnects

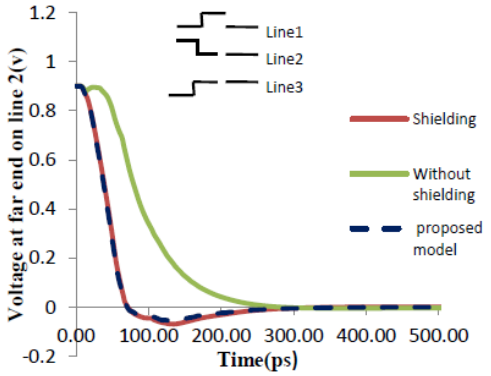

Fig:8(a)

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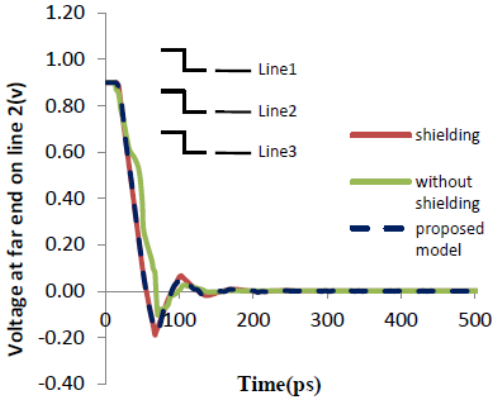

Fig:8(b)

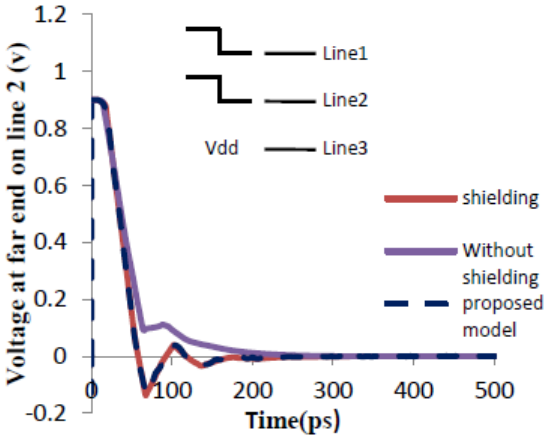

Fig:8(c)

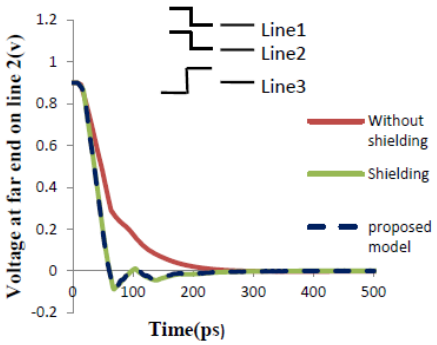

Fig:8 (d)

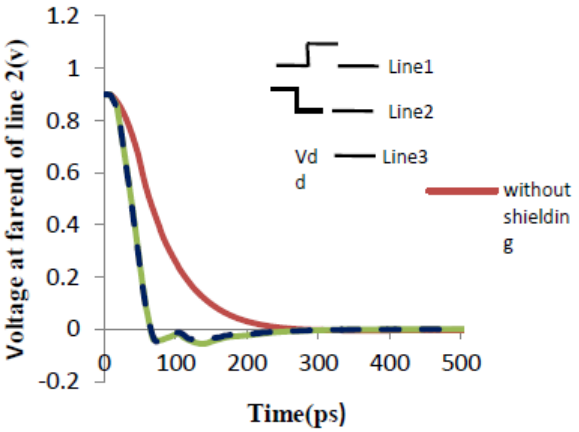

Fig:8(e)

Fig. 8. TRANSIENT RESPONSES FOR DIFFERENT INPUT SWITCHING ON VICTIM LINE 2 (a) Case-1 (b) Case-2 (c) Case-3 (d) Case-4 (e) Case-5

TABLE I: PROPAGATION DELAY FOR DIFFERENT SWITCHING CASES ON VICTIM LINE 2

Input Switching cases				Propagation Delay on victim line 2			
				Delay on line 2 with shielding		Delay on line 2 without shielding	%error between proposed model and HSPICE
Switching Case mode	line1	line2	line3	HSPICE(ps)	Proposed model(ps)		
Case-1	1-0	1-0	1-0	10.95	11.5	8.88	4.7
Case-2	1-0	1-0	0-1	13.3	13.5	26.4	1.4
case-3	1-0	1-0	Vdd	12.04	12.5	15.24	3.6
case-4	0-1	1-0	Vdd	14.88	14.5	44.4	2
case-5	0-1	1-0	0-1	16.84	16.3	60.5	2.7

TABLE II: IN AND OUT-PHASE DELAY ON LINE 2

Delay on line 2 (ps)	With Shielding	Without Shielding
In-phase Delay	10.87	88.08
Out-phase Delay	16.84	60.05

Fig.5.compares the functional crosstalk noise between shielded lines to unshielded coupled lines where the the aggressor lines are switched and the victim line is kept quite at a constant value .75% of improvement in functional crosstalk is seen in shielded lines when compared to unshielded lines.Fig.6 gives the delay values on victim line 2 for different cases of switching transitions on three lines for both shielded and unshielded lines. Fig.7 evaluates crosstalk noise for different interconnect lengths and the effect of crosstalk noise with increase in length is very less on Shielded lines when compared to unshielded lines.

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DOI: 10.35940/ijitee.J1100.0981119
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In Fig.8.from (a) to (e) analyzes different switching cases and compares transient responses on line2 for both shielded and unshielded lines. For all the cases
Considered in Fig.8, proposed model values match exactly with the simulations of HSPICE. Table I provides the crosstalk induced delays on line 2 for both shielded and unshielded lines. It can be observed from the table that average error between HSPICE and proposed model is less than 5%.In-phase and out-phase delays for shielded and unshielded lines have been provided in Table II and can be seen that there is a drastic decrease in delays using Active shielding when compared to unshielded line

VI. CONCLUSION

An effective geometry with active shielding of coupled interconnect lines has been proposed in this paper for reduction of crosstalk noise and delay induced in interconnects. Active shielded coupled interconnect lines with resistive driver are modeled using FDTD technique. Considerable improvement has been seen in proposed geometry when compared with unshielded interconnect lines in terms of crosstalk noise and delay. The results obtained using HSPICE simulation coincides with that of FDTD modeling with a very little difference 5%

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