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# Design and Simulation of a Novel Nine Level Inverter Topology for Motor Application

**Ruchika Sharma, Shimi Sudha Letha, Rohit kumar**

***Abstract*: In the couple of years, the demand of multilevel inverter has expeditiously increased in the field of utilization of electrical energy. Because the multilevel inverter is a key technology to integrate the different renewable energy sources (wind, solar etc) with the grid. In this research work, authors have configured a novel topology of nine level multilevel inverter has less number of switches with dc voltage sources. The presented approach has been designed to 9-level inverter with seven unidirectional switches with voltage sources. It comprises of an H-bridge which synthesize to ac voltage by utilizing almost all possible additive and subtractive cases of the voltage sources with its combinational power switches and generated optimal firing angles using selective harmonic elimination method with Genetic Algorithm to decrease the lower order harmonic present in the output voltage of the, which supplied by the presented nine-level inverter. It has been concluded that presented approach use a less number of power switches in drive circuit and the number of dc voltage sources also make a simple circuit and enhance the efficiency of the complete system.***

***Keywords:* Selective harmonic elimination(SHE); Genetic algorithm (GA); Multilevel-inverter***

## I. INTRODUCTION

The power quality and large amount of energy consumption are the major concern today. Non –renewable energy sources such as coal, natural gas and petroleum are depleting very fast. Thus, renewable energy sources such as Magneto hydrodynamic generator (MHD), wind, solar, hydro, etc. can replace non-renewable sources. Mostly the output of such renewable energy sources is direct current (dc) for integration with grid an dc to ac converter is required [1]. So that, conversion of dc to ac power is a key technology in the recent set-up for generation to utilization of electric power [2]. But these power electronics conversion devices generate power quality issue in front of generating and distributing utility of grid. MLI generates the stepwise voltage waveform with illustrious power quality and scant harmonic distortion [3], by which these organizations can be commitment to fulfil various IEEE power quality standard such as IEEE Standard 519, IEEE Standard 1547 and IEEE Standard 141 etc. In general, the MLI can be designate in three main cliques as donated in fig.1. This paper aims to achieve maximum capacity from dc link by a suitable arrangement of switches which improves economic implementation cost, switching frequency, TSV, number of levels, and THD. Further, lower order harmonic can be minimized by exchange the switching strategies. For elimination of initial order harmonics, a SHE technique has been implemented for multilevel inverters [4]. In the term of trigonometric equations, a multiple solution can be possible by eliminate the lower order harmonics making using the control the switching angle. In proposed work Genetic Algorithm (GA) has been utilized to solve the nonlinear equations. The circuit arrangement of the proposed topology of MLI has shown in Fig.2.

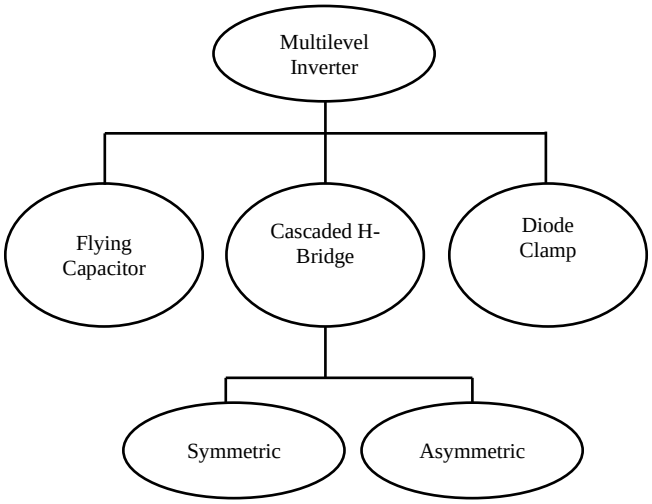


**Fig. 1 Classification of Multilevel inverters**

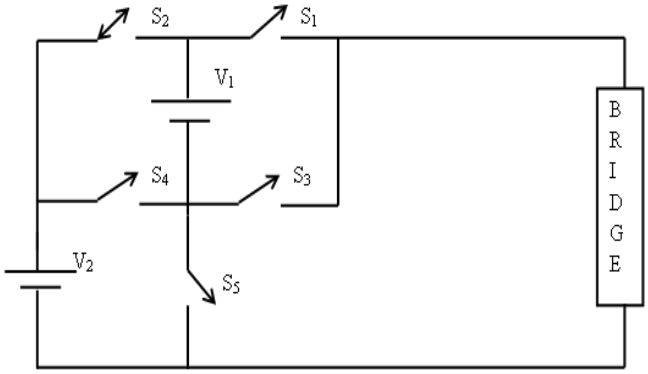


**Fig. 2 Single Phase Nine Level Inverter Topology**

This paper is structured as follows: literature research using with existing topologies for multilevel inverters have been discussed in section II. Then, proposed topology for nine level inverter is presented in section III. In the section IV, simulated model of nine level inverter with selective harmonics elimination has been presented.

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The performances of the proposed topologies with different load loads has been presented in section V. Lastly conclude the proposed topology in section VI.

## II. EXISTING TOPOLOGIES

Among the different classification of the multilevel inverters that ware made known by few researchers, cascaded multilevel inverter is a most crucial in harmonic reduction. Moreover, SHE method has used to terminate the initial order harmonics for multilevel inverters. SHE has more powerful, combine with genetic algorithms. GA technique has found the optimal solution for the switching angles. This approach has more advantage of less number of switches compared to conventional configurations and easily increases the more number of levels [5-6]. A couple of few researches [7-10] deal with the Neutral Point Clamped (NPC) and Active Neutral Point Clamped (ANPC) plus cascaded full bridge inverters topologies which are widely applied in the three phase power conversion. Fast switching diode has been used to split the single dc link into two or more then, two equal voltage levels which clamps the maximum value of voltage of the main switch. A new topology was introduced by [11]. For seven level inverter topology, five switches with three dc voltage sources and also along with one H-bridge which having four semiconductor switch used for opposite polarity to generate three positives(+ve), three negative(-ve) has been developed. For 1 zero-voltage level, one H-bridge which having four semiconductor switches have been used for reverse polarity [12]. Sub-multilevel inverter contains both bidirectional and unidirectional switches to implement the designing strategy of bidirectional switches is designed by combination of two back to back connected IGBTs with antiparallel diode [13-14]. To reduces the switches, an optimal modulation topology has been developed by [15], but it has been observed that conduction losses is increases and because of series connection of semiconductors devices which results as a high output current in load circuit. A new multilevel inverter topology which has some advantages like simplicity, redundancy and modularity w.r.t. the cascade H-Bridge converter [16]. However, the more components have been used in this topology. A novel configuration which consist the series module and each series module included six insulated gate bipolar transistor (IGBTs) and two dc sources [17]. A novel dc–ac inverter has been developed. TMS320LF2407 digital signal processor (DSP) has been used to control the sinusoidal pulse-width modulation (SPWM). Experimental results have achieved the maximum and full load efficiencies are 96.9% and 94.6% respectively [18]. An optimal design of MLI inverter is developed for the applications like EV and HEV drives. The Topology of the power circuit uses less number of power semiconductor switches. Subsequently, reduced the THD according to the IEEE-standard-519, absent of filters i.e. 3.82% [19]. Recently, few novel topologies have been implemented with reduce number of switches which deals with better power quality using GA-SHE for symmetric and asymmetric approaches of multilevel inverter [20-21].

## III. PROPOSED TOPOLOGY

The input of multilevel inverter is ac signal and It is divided into three parts negative, zero and positive half cycle. Each half cycle further divided into subpart, but the output in the form of (a) negative (b) zero and (a) positive. Single phase configuration consists of two dc voltages sources (V1 and V2) with different magnitude, four unidirectional (S1, S3, S4, S5) and one bidirectional (S2) switches and an isolated H-bridge. The required levels of output voltage, computed by using this equation,

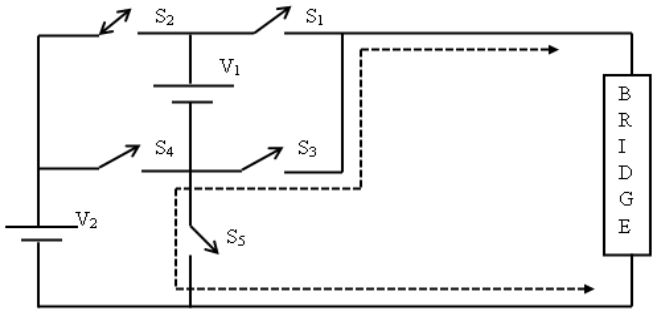
$$N\_level=2n+1 \quad (1)$$

Where, the number of dc voltage sources represent by n which used in Simulink model. In Simulink model, The total number of required switches except bridge switch has been compute using equation (7).

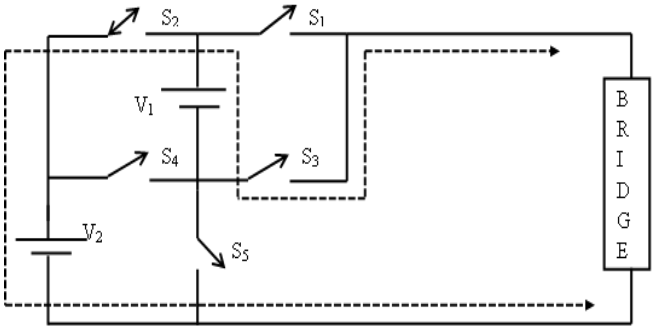
$$N\_switch=n \quad (2)$$

The switching states of the topology are illustrated in Fig.4 (a) to Fig.4 (e) H-bridge is used to generate positive and negative voltage level.

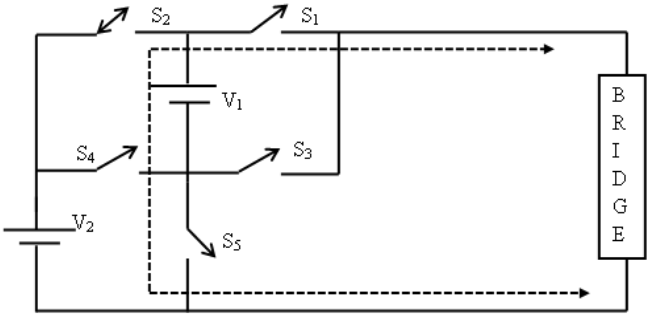
Different switching operation to get the desired nine level voltages from the structure analyzed in Fig.4, and the state of the switches which is indicate by 1 and 0 respectively imply the ‘ON’ and ‘OFF’.




(a)




(b)




(c)

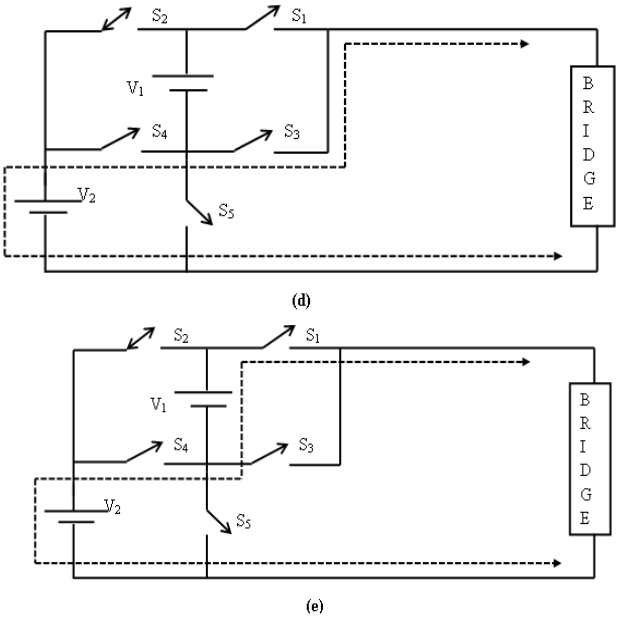



**Fig.4 Different Switching Sequence of the Presented Nine-Level Topology (a-e)**

**Table 1 Nine level Switching Sequence Topology**

| Sr. No | S1 | S2 | S3 | S4 | S5 | Vo | Fig.4 (a-e) |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | a |
| 2 | 0 | 1 | 1 | 0 | 0 | $V_2$-$V_1$ | b |
| 3 | 1 | 0 | 0 | 0 | 1 | $V_1$ | c |
| 4 | 0 | 0 | 1 | 1 | 0 | $V_2$ | d |
| 5 | 1 | 0 | 0 | 1 | 0 | $V_2$+$V_1$ | e |

SHE the most commonly approach to compute the angles α1, α2, α3, α4, α5 by to eliminate eleven dominant lower order of the harmonic components (5th,7th,111th,13th) while obtaining the desired fundamental output voltage. Fourier series coefficient bn can be expressed as (from equations (3) to (6)):

$$b_1 = \frac{4}{\pi}[(V_2 - V_1)\cos(\alpha_1) + (V_1)\cos(\alpha_2) + (V_2)\cos(\alpha_3) + (V_1 + V_2)\cos(\alpha_4)] \quad (3)$$

$$b_5 = \frac{4}{5\pi}[(V_2 - V_1)\cos(5\alpha_1) + (V_1)\cos(5\alpha_2) + (V_2)\cos(5\alpha_3) + (V_1 + V_2)\cos(5\alpha_4)] \quad (4)$$

$$b_7 = \frac{4}{7\pi}[(V_2 - V_1)\cos(7\alpha_1) + (V_1)\cos(7\alpha_2) + (V_2)\cos(7\alpha_3) + (V_1 + V_2)\cos(7\alpha_4)] \quad (5)$$

$$b_{11} = \frac{4}{11\pi}[(V_2 - V_1)\cos(11 \propto_1) + (V_1)\cos(11 \propto_2) + (V_2)\cos(11 \propto_3) + (V_1 + V_2)\cos(11 \propto_4)] \quad (6)$$

The basic objective of SHE problem is to decrease the cost function, which is the sum of the harmonics to be terminated normalized to the fundamental. The cost function for SHE problem in nine-level is given by,

$$fitness\ F = \sqrt{b_5^2 + b_7^2 + b_{11}^2} \quad (7)$$

The switching angles α1 to α5 have been chosen in as the possibility of the selective 5th, 7th, 11th, harmonics can be terminated and satisfied the constraint equation

$$0 \leq \alpha\_1 \leq \alpha\_2 \leq \alpha\_3 \leq \alpha\_4 \leq \pi/2 \quad (8)$$

Following steps have been utilized to developed the Genetic Algorithm

**Step I.** In the first step initialize all the parameters for genetic algorithm toolbox such as Crossover and Mutation.

**Step II.** Fitness function has evaluate using equation (7)

**Step III.** Check all the constraints of the equation (8)

**Step IV.** Parent chromosomes have been chosen for further process.

**Step V.** Initial parameter crossover and mutation have been used to generate the new offspring.

**Step VI.** Observed, the maximum number of iteration has been reached by the termination condition Otherwise comeback to step number two. Finally end the problem, if the optimized switching angles has been obtained.

## IV. SIMULINK MODEL OF NINE LEVEL MULTILEVEL INVERTER

The Simulink model is implemented in the MATLAB/Simulink environment. Multicarrier Pulse Width Modulation (MPWM) has been used to generating the signals for the inverter which analysis the model behavior of an inverter for improving its control strategy.

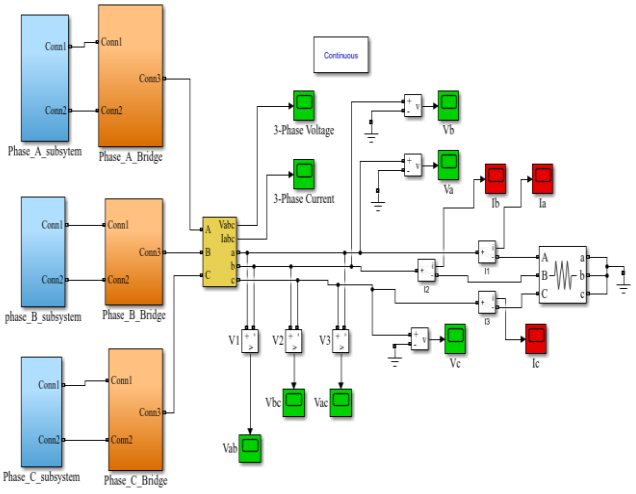



**Fig.5 Simulink Model of Three Phase MLI Subsystem Model of Nine Level Inverter**



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Fig.5 shows the internal blocks of nine levels Phase A subsystem blocks which consist battery connection with switch. Phase B and Phase C subsystem blocks have same connection configuration.

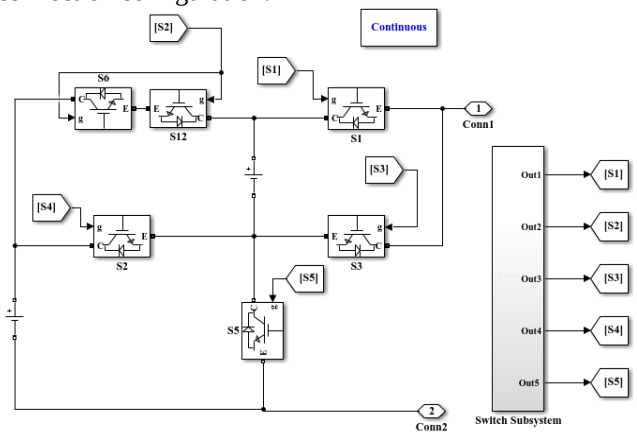


**Fig. 6 Phase A Subsystem Block for Nine Level Inverter**

The methodology of presented work comprises of a Hybrid-bridge which synthesize an ac voltage by utilizing almost all the possible cases of the voltage sources with its combinational power switches.

## V. SIMULATION RESULTS

The simulation analysis of the implemented MLI topology in the generation of a required waveform of output voltage and current for resistive load and induction motor has been simulated and implemented. The harmonic analysis using Fast Fourier Transform (FFT) for proposed 9-level inverter with Genetic Algorithm Selective Harmonic Elimination) has been implemented with optimal angles $\alpha_1$=13.4029°, $\alpha_2$=20.9991°, $\alpha_3$=36.3220° and $\alpha_4$=59.1644°. The input voltage and load magnitude of the proposed topology has been discussed in Table 2.

**Table.2 Parameters used in Simulation**

| | | |
|---|---|---|
| Simulation Step Size | | Ts=2.458215e-005 |
| Three-Phase Voltage Source | Nine -Level | $V_1$=40V, $V_2$=60V |
| R Load | | R=100Ω |
| R-L Load | | R=100Ω, L=1e-3H |
| Switching Element | | IGBT/Diode(mask) |

### A. *Result Analysis of Nine-Level Inverter for R-Load*

Fig.5.1(a) to Fig.5.1(e) respectively show the obtained three phase line voltage(V), three phase current (I), phase voltage (Va), Phase voltage (Vb) and phase voltage (Vc) waveforms for the given optimal switching angles.

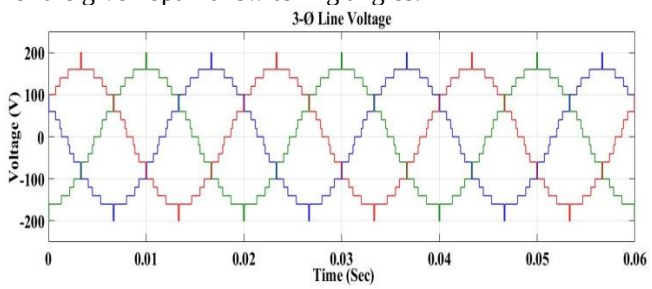


**Fig.5.1 (a) 3-Ø Line Voltage Waveform of 9-level MLI for R-Load**

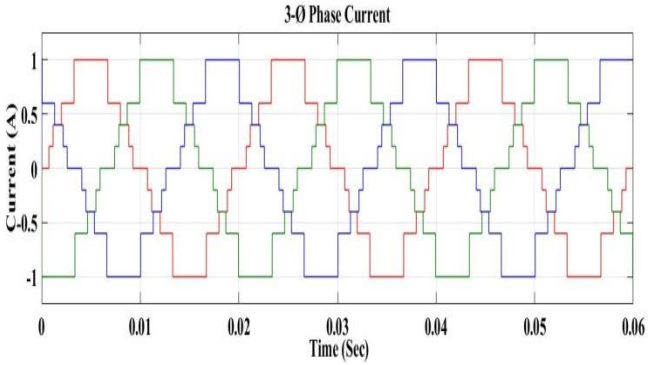


**Fig.5.1 (b) 3-Ø Phase Current Waveform of 9-level MLI for R- Load**

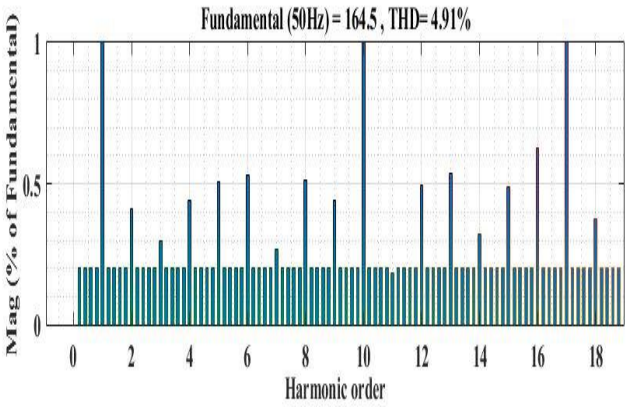


**Fig.5.2 Harmonic Spectrum of Line –Voltage for Nine-Level MLI for Resistive Load**

### B. *Result Analysis of Nine-Level Inverter for Motor-Load*

Fig.5.5 to Fig.5.5 (e) respectively show the obtained three phase line voltage (V), Three phase current (I), phase voltage (Va), Phase voltage (Vb) and phase voltage (Vc) waveforms for the given optimal switching angles.

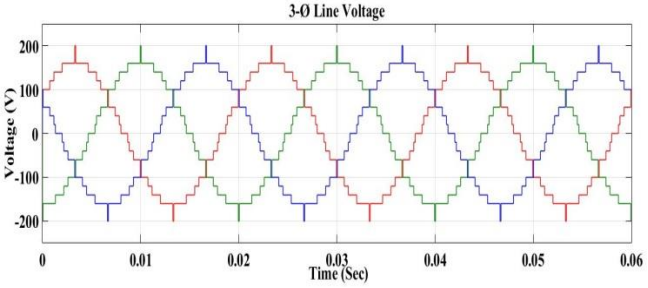


**Fig.5.5 (a) 3-Ø Line Voltage Waveform of 9-level MLI for Motor –Load**

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**Table 3 Comparison Based on Number of Components till 9 -Level n Number of Components till 9 -Level**

| Sr .No | Reference | Year | level | No. of Switch | No. of Capacitor | Number of Diode | No. of Source | Harmonics Elimination Technique | 3rd Harmonics | 5rd Harmonics | THD % |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | **Purposed** | **2018** | **9** | **9** | - | - | **2** | GA-SHE | 0.30 | 0.51 | **4.38** |
| 3 | [22] | 2018 | 9 | 8 | 2 | 1 | 1 | FW | - | - | FW |
| 4 | [23] | 2018 | 9 | 12 | 2 | - | 1 | FW | - | - | FW |
| 5 | [24] | 2017 | 9 | 9 | 2 | 2 | 1 | SHE | - | - | 5.13 |
| 6 | [25] | 2017 | 7 | 7 | 1 | 2 | 2 | LPF | 0.28 | 0.46 | 3.3 |
| 7 | [26] | 2016 | 9 | 10 | 2 | - | 2 | LS-SPWM | 4.6 | 2.1 | 9.53 |
| 8 | [27] | 2015 | 9 | 10 | - | - | 3 | SPWM | 5.2 | 2.5 | 9.93 |
| 9 | [28] | 2015 | 7 | 8 | - | - | 3 | PS- SPWM | 10.5 | 7.3 | 20 |
| 11 | [29] | 2015 | 7 | 6 | - | - | 1 | VAPD | 8.6 | 5.9 | 15 |
| 12 | [30] | 2015 | 11 | 20 | - | - | 5 | SPWM | 4.9 | 2.3 | 8.68 |
| 13 | [1] | 2016 | 11 | 10 | - | - | 4 | PSO-SHE | 0.28 | 0.46 | 3.7 |

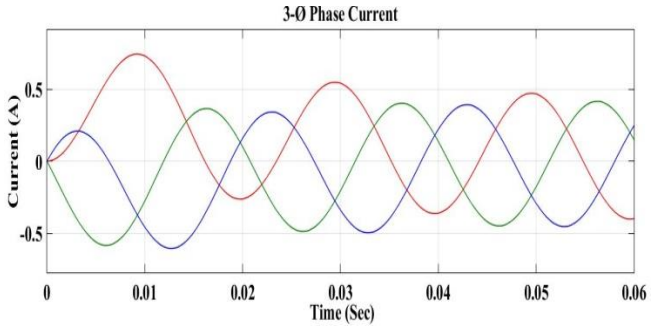


**Fig.5.5 (b) 3-Ø Phase Current Waveform of 9-level MLI for Motor –Load**

The frequency spectrum of line voltage obtained using FFT analysis in Fig.5.4. It has been observed from Fig.5.6 that the minimum value of line voltage THD is 3.41%.

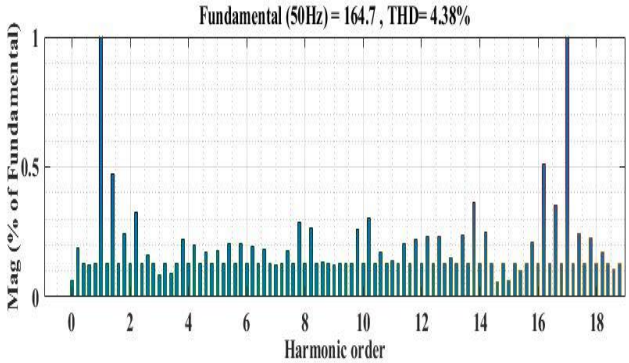


**Fig.5.6 Harmonic Spectrum of Line –Voltage for 9-level MLI for Motor –Load**

## VI. CONCLUSION

The present thesis work proposed, new topologies of asymmetrical configuration of 3-phase MLI are proposed. The proposed nine –level 1-phase inverter topology consists one bidirectional and eight unidirectional switches with two batteries. Furthermore, medium-to-high voltage applications topology-I has been extended in two different ways as shown in topology-II. Topology-II has achieved twenty-five level inverter, which consists two bidirectional and ten unidirectional switches with three batteries per phase. The mathematical analysis of switch stress voltage for each step is widely discussed in chapter third, which will very useful for hardware implementations of the proposed topologies. The present study focused on fundamental switching scheme for harmonic elimination and the mathematical modelling of SHE has further been elaborated. For the proposed 9-level 25-level and the switching angles that minimize lower order harmonics have been determined using GA. A detailed simulated experimental study has been carried out of the proposed topologies for different type of loads. The simulations are carried out and the magnitudes of the harmonics contents have been calculated using the FFT analysis.

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