Modified LECTOR Technique for Level Shifters

G.V.S.R. Indraja, T.V.S.Divakar

Abstract: ***Static power dissipation is a major problem in CMOS circuits and this is due to the increase in sub threshold leakage current which is the effect of voltage scaling and also leading to reducing the threshold voltage. Here we propose Lector technique to reduce the leakage current and at the same time it will not increase the dynamic power dissipation. Two leakage control transistors of which one is p-type and the other one is n-type were introduced into the logic gate. The source of one transistor controls the gate terminal of the other transistor. For any combination of input one of the two leakage control transistors will be near to its cutoff voltage by this the leakage currents can be minimized as the path resistance to ground will increase. For both idle and active states of circuit the proposed Lector technique is applicable which will result in more leakage reduction when compared to remaining techniques used for leakage reduction and it will also out pass the limitations Occurred due to the implementation of other power and delay reduction techniques. Experimental results indicate a delay is reduced by 50.3% and power is reduced by 94.4% for proposed level shifter circuits.***

Keywords : Leakage power, transistor stacking, power optimization, Deep submicron, Level shifter.

I. INTRODUCTION

This Reduction of the battery life is the major drawback of battery powered devices and applications with high consumption of power[1]. This will affect the cooling cost and packaging of the device along with reliability. Leakage currents, short-circuit currents and dissipation due to capacitive power are the three major reasons for dissipation of power[2]. The charging and discharging cycles of the capacitance will lead to the dissipation of capacitive power[3]. A conducting path which connects voltage supply and ground whenever there is s transition in logic gate will lead to short circuit currents[4-7]. A lot of research is done to reduce the leakage current which consists of a diode in reverse bias state and the leakage current consists of the currents due to the sub threshold and the diode in reverse bias[8]. The reverse bias currents are generated due to the diffusion of carriers in the OFF state transistors. The sub threshold currents are generated due to charge stored in the active transistors[9-10].

In this paper, we describe a modified LECTOR (Leakage Control Transistor) leakage power reduction technique for designing CMOS circuits. In section we will discuss about various types of level shifters and in section 3we will discuss about the proposed LECTOR technique. Section 4 deals with the results and discussion.

II. DESIGN OF LEVEL SHIFTER CIRCUIT

Multi-supply voltage techniques require level shifters on signals that go from one voltage level to another. Without level shifters, signals that cross voltage levels will not be sampled correctly. It is suggested that formal techniques be used in the design flow to identify missing level shifters. Finding these missing definitions early will save time in simulation and synthesis debugging.

Level shifters are added to ensure that blocks operating at different voltages will operate correctly when integrated together in the SoC. Level shifters must ensure the proper drive strength and accurate timing as signals transition from one voltage level to another. Level shifters can be inserted during the synthesis or implementation stage. Every signal that crosses an MSV power domain should have a level shifter attached to it. Although level shifting from a higher-voltage power domain to a lower one is usually optional, level shifting from a lower-voltage power domain to a higher one is mandatory. Level shifters are placed close to the power domain boundaries. However, level shifters have two power rails:

- Primary power rail: usually set at the top and bottom edge of the level shifter
- Secondary power rail: usually set at the center horizontal line of the level shifter

The power domain where the level shifter resides depends on which voltage the primary power rail matches. For example, if the primary power rail of the level shifter is a 0.8V rail, that level shifter should be placed in the 0.8V power domain. Therefore, some knowledge about the library is needed to decide in which power domain to place the level shifter. Using low-power level-shifting cells can have a significant impact on timing and physical design.

Fig 2 below shows a level shifter with a cross coupled differential amplifier with single ended output. Depending upon the input value the output value changes from 0 to 1.

Fig 3 below shows a level shifter with a PMOS differential amplifier and current mirror circuit at the output stage. Depending upon the input value, the output value changes from 0 to 1.

Fig 4 below shows a level shifter with a differential amplifier, current mirror circuit and inverter at the output stage. Depending upon the input value, the output value changes from 0 to 1.

Revised Manuscript Received on September 05, 2019.

G.V.S.R. Indraja, Dept. of E.C.E, GMRIT, Rajam, Andhra Pradesh, India

T.V.S.Divakar, Dept. of E.C.E, GMRIT, Rajam, Andhra Pradesh, India.

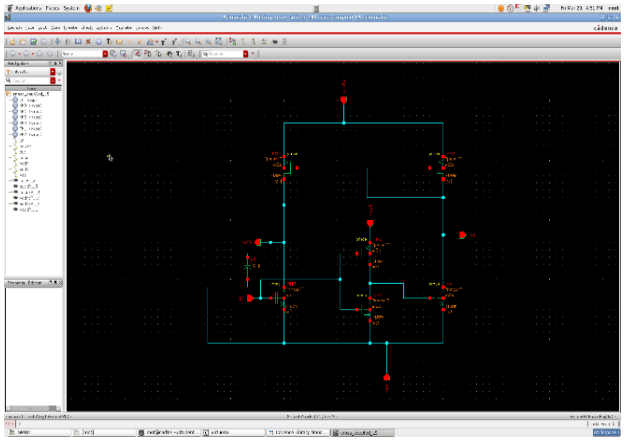

Fig. 2: Schematic of type 1 level shifter

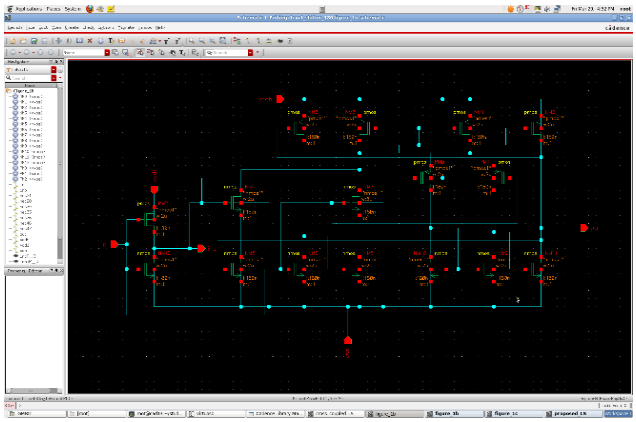

Fig. 3: Schematic of type 2 level shifter

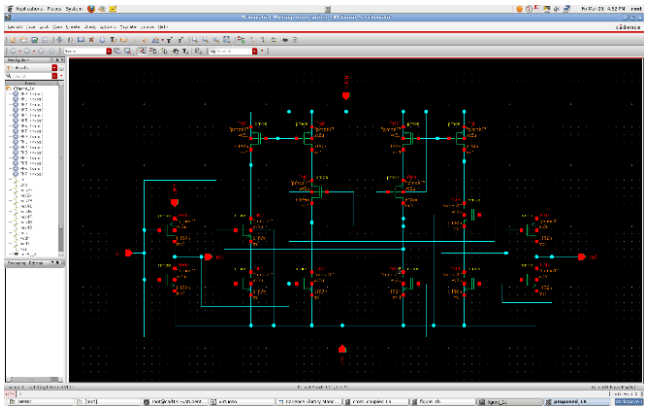

Fig. 4: Schematic of type 3 level shifter

Fig 5 below shows a level shifter with a two differential amplifier stages with current mirror load followed by a differential amplifier with current mirror load and cross coupled pair to obtain the single ended output. Depending upon the input value, the output value changes from 0 to 1.

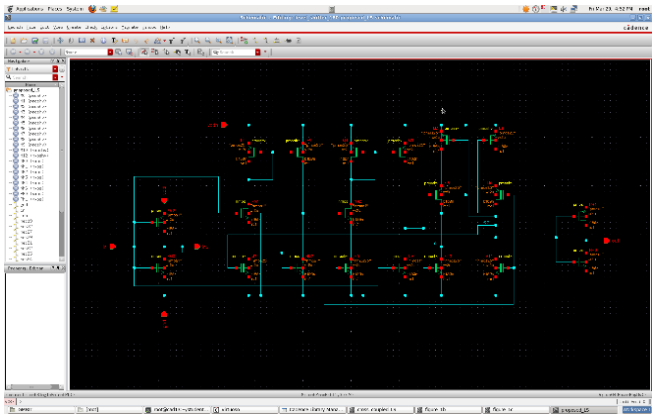

Fig. 5: Schematic of type 4 level shifter

III. PROPOSED LEVEL SHIFTER CIRCUIT USING LECTOR TECHNIQUE

The proposed technique involves inverter at the primary stage and differential amplifier with current mirror load. An inverter is introduced at the input end and the inverted value is considered for differential amplifier input. The double ended input and unbalanced output differential amplifier is used in this proposed technique. The output of the differential amplifier is feeded as the input for the Lector low power reduction technique.

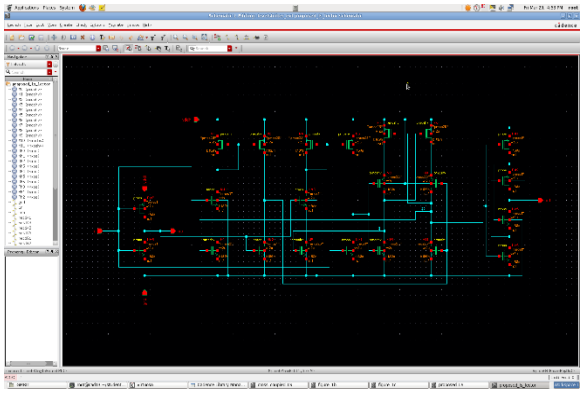

Fig. 6: Schematic of proposed Lector level shifter

IV. RESULTS AND DISCUSSIONS

Figure 7 below shows the output waveform of the type 1 level shifter. An input voltage of 900mV is given to the circuit and an output of 1.8V is obtained.

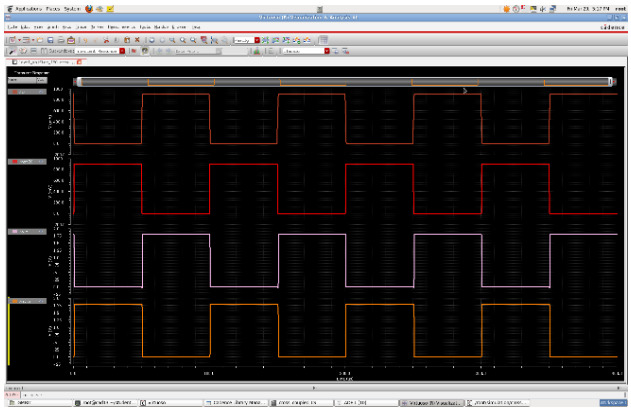

Fig. 7: Output waveform of type 1 level shifter

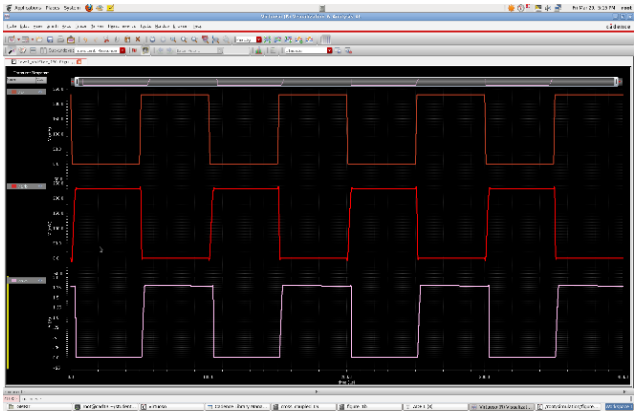

Fig. 8: Output waveform of type 2 level shifter

Figure 8 below shows the output waveform of the type 2 level shifter. An input voltage of 230mV is given to the circuit and an output of 1.8V is obtained.

Figure 9 below shows the output waveform of the type 3 level shifter. An input voltage of 300mV is given to the circuit and an output of 1.8V is obtained.

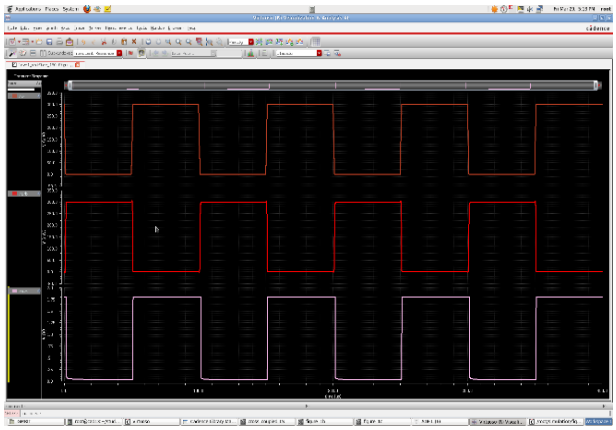

Fig. 9: Output waveform of type 3 level shifter

Figure 10 below shows the output waveform of the type 4 level shifter. An input voltage of 90mV is given to the circuit and an output of 1.8V is obtained.

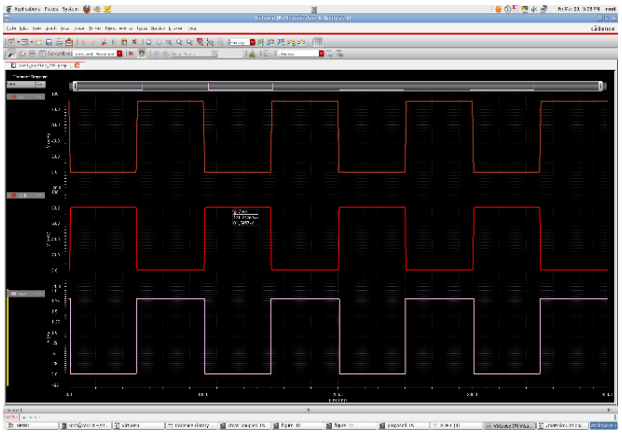

Fig. 10: Output waveform of type 4 level shifter

Figure 11 below shows the output waveform of the proposed Lector level shifter with 90mV. An input voltage of 90mV is given to the circuit and an output of 1.8V is obtained.

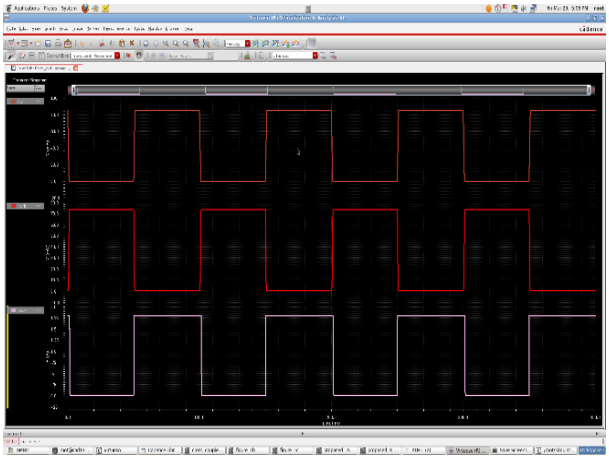

Fig. 11: Output waveform of proposed Lector level shifter with 90mv

Figure 12 below shows the output waveform of the proposed Lector level shifter with 85mV. An input voltage of 85mV is given to the circuit and an output of 1.8V is obtained.

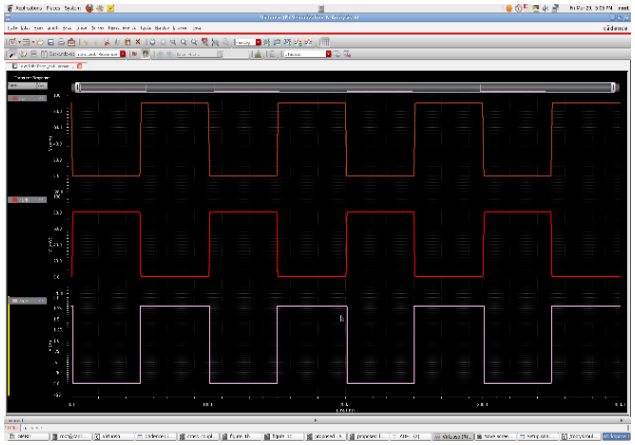

Fig. 11: Output waveform of proposed Lector level shifter with 85mv

Table 1: Comparison of Delay and power of various level shifters

Level Shifter Technique	Delay (10^{-6})	Static Power (10^{-12})	Dynamic Power (10^{-6})
Type 1	93.76	374.4	37.7
Type 2	85.44	377.3	131. 6
Type 3	49. 66	356.8	49.01
Type 4	49.34	151.4	37.70
Proposed 1(90mv)	49.09	122.8	37.06
Proposed 2(85mv)	46.82	33.49	2.09

V. CONCLUSION

The proposed level shifter with lector technique shows better performance in terms of delay static power and dynamic power. An efficient design methodology for CMOS circuits have been presented which can reduce the leakage power. Transistor size Minimization and reduction of supply voltage are the two major advantages of using the Lector technique. This is possible because Lector technique have low threshold voltage which lead to reduction of leakage power. We dont need any circuitry to control and monitor the circuit states in Lector technique which is a must in other techniques used for leakage control. As there are no additional circuits for the controlling and monitoring the circuit states the dynamic power utilization is very low. Experimental results show that our technique yields reduction of about 51% in terms of delay compared to existing level shifter. In terms of static power 90% of improvement is observed when compared to existing level shifter. In terms of dynamic power 95% of improvement is observed when compared to existing level shifter

REFERENCES

1. H. J. M Veendrick, “Short circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits ,” *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 468–473, Aug. 1984.
2. A. P. Chandrakasan and R. W. Brodersen, “Minimizing power con-sumption in digital CMOS circuits,” *Proc. IEEE*, vol. 83, pp. 498–523, Apr. 1995.

3. R. X. Gu and M. I. Elmasry, "Power dissipation analysis and op-timization for deep submicron CMOS digital circuits," *IEEE J. Solid-State Circuits*, vol. 31, pp. 707–713, May 1999.
4. Q. Wang and S. Vrudhula, "Static power optimization of deep sub-micron CMOS circuits for dual V technology," in *Proc. ICCAD*, Apr. 1998, pp. 490–496.
5. B. J. Sheu, D. L. Scharfetter, P. K. Ko, and M. C. Jeng, "BSIM: Berkeleyshort-channel IGFET model for MOS transistors," *IEEE J. SolidState Circuits*, vol. SC-22, pp. 558–566, Aug. 1987.
6. S. Thompson, P. Packan, and M. Bohr, "MOS scaling: Transistor challenges for the 21st century," *Intel Technol. J.*, vol. Q3, 1998.
7. J. P. Halter and F. Najm, "A gate-level leakage power reduction method for ultralow-power CMOS circuits," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1997, pp. 475–478.
8. D. Duarte, Y.-F. Tsai, N. Vijay Krishnan, and M. J. Irwin, "Evaluating run-time techniques for leakage power reduction," in *7th Proc. ASP-DAC*, 2002, pp. 31–38.
9. M. D. Powell, S.-H. Yang, B. Falsafi, K. Roy, and T. N. Vijaykumar, "Gated-Vdd: A circuit technique to reduce leakage in deep submicron cache memories," in *Proc. IEEE ISLPED*, 2000, pp. 90–95.
10. M. C. Johnson, D. Somasekhar, L. Y. Chiou, and K. Roy, "Leakage control with efficient use of transistor stacks in single threshold CMOS," *IEEE Trans. VLSI Syst.*, vol. 10, pp. 1–5, Feb. 2002.