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Design, Implementation and Power Analysis of Low Voltage Heterojunction Tunnel Field Effect Transistor based Basic 6T SRAM Cell

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Abstract*: The battery-powered mobile devices limited energy process by MOSFET's due to subthreshold swing and underneath 60mV/dec for ultra fewer energy applications. This research introduces the layout and execution of a mobile electronic device full-on-presence, extended Miller potential, and reduced HETT subthreshold swing effectiveness has been compared with MOSFET's Gate oxide blending on source can increase channel tunneling in this work. To enhance transistor line, Miller capacitance impact can be decreased by using low band offset equipment and small power product of metals such as Ge or SiGe. This, in turn, leads to stronger transistor efficiency features. The proposed layout and execution of HETT includes manufacturing of mutually NHETT and PHETT and efficiency analyzes of both NHETT and PHETT. Concerning the fundamental and skeletal distinctions among MOSFET and HETT to promote the utilization of MOSFET instead of HETT, the benefits and constraints of both NHETT and PHETT have been detailed. HETT's construction process is by no means entirely different, suitable for the scheme of MOS method and suitable for transportable motorized applications. HETT provides the 6T SRAM cell electricity evaluation and the output was reviewed using standard SRAM cell. The average power, maximum power and minimum power of SRAM by using both MOSFET and HETT are obtained and compared. The mask layers of HETT fabrication is not that much difference than MOSFET and hence CMOS MOSFET fabrication is friendly to HETT fabrication. In future, the combination of both CMOS MOSFET and HETT are used, CMOS technology for digital logic and HETT for semiconductor memory applications.

Keywords: Tunneling, Heterojunction, low power, SRAM, ultra-low voltage, band to band tunneling

I. INTRODUCTION

The product in transistors sited near the silicon tray rises under law of Moore's [1], in IC's energy utilization also improves as a result of more processor function. This raises chip heat in rotation and limits the activity of the processor. To preserve the chip operation and restrict the heat generated [2], fresh energy optimization techniques are needed. Voltage leveling is one of the finest methods for achieving the necessary energy effectiveness, but it results in elevated leakage and poor operating speed [3]. On the other hand, limiting the sub-threshold tilt of MOS transistor won't enable the threshold voltage to be further scaled [4] leading to decreased closed-loop state flow and restricting ON to the rental ratio of OFF-state [5]. Using a TFET [6] to increase chip effectiveness instead of MOSFET is the biggest choice to manage the bottom constraints. Ge, SiGe or InAs has low bandgap [7], the TFET design offers elevated leakage, reduced subthreshold swing and lower energy usage and runs by little load potential. Authors pay some importance to TFET because in future IC systems they are strong. The TFETs, however, have a small drop voltage in ON state [8]. A HETT [9] is used to solve this TFET limitation.

The BTBT [10-11] is strong in HETT and thus raises the flow of the ON-state drive [12]. On the other hand, it is easier to obtain reduced power consumption, reduced swing of the subthreshold and less leakage current. Also, possible is the further scaling of the transistor [13] and thus more compact size can be acquired. In this, to boost the BTBT and enhance the Miller capacity, the oxide is overlapped with the source [14-15]. Hence, the chip's performance can be enhanced and thus HETT is one of MOSFET's best options for techniques beyond CMOS. In this document, N-HETT and P-HETT layout and execution were given in detail. MOSFET's volt-ampere features and transfer features are discussed. To checks the NHETT and PHETT's of the Standard 6T SRAM cell timing performance and power.

II. CONSTRUCT AND ARCHITECTURE OF HETT

HETT with gate oxide overlapping technique uses low band gap materials such as Ge or SiGe. In HETT, if lower bandgap products such as those Ge or SiGe has used instead of Si when ON to OFF also enhanced the state currently. The epitaxial method is used for HETT production. Using CVD (Chemical Vapor Deposition), the SiGe and the ground Si structures are created. The Si length of the top surface Si layers is between 20 nm and 30 nm and the length of the SiGe layer is between 20 nm and 50 nm where SiGe sheet is made up of Ge material ranging from 10% to 25%. The size of the SiGe or Ge layer is between 5 nanometers and 20 nm. The film's size is well controlled from 5 nm to 20 nm. Oxidation and annealing methods are utilized Oxygen and nitrogen are respectively. Temperature between 1005 ° C and 1100 ° C is needed for two task duration in annealing, oxidation, Although the later phases are within 900 ° C and 950 ° C and the necessary moment for twice model is almost 30 minutes to an hour the Si_3N_4 layer was distinguished by thermal etching of phosphoric acid and SiO_2 strands were divided by hydrogen fluoride (HF) etching.

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HETT consists a SOI including a top Si layer, a Case layer with a rear substratum, a flap on the underside of Si, the inactive area under the gate where the dynamic fields in the SiGe or Ge area as the origin and Si area for start are trained and a Ge / Si heterojunction between two active regions is formed. SiO_2 in gate terminal isolating coating upon the ground of the Silicon rock plus the door of the electrode is positioned on the layer of SiO_2.

Transistors have two alternatives one with P source and drain as N fields, and the other among N-type and P channel regions. Boron and Boron difluoride are employed like PHETT component and Sulphur is used for both these transistors Arsenic or N-type antimony for n-type & p-type doping procedures, implantation of ion, and heat, laser annealing is carried out. Accelerated closed and open-loop state current is acquired as the reference is created at the SiGe or Ge region; the Si region filter is created. The instrument manufacturing method is easy and well suited to the current CMOS manufacturing method without altering the technology and can, therefore, be used for mass production of ICs with decreased costs in manufacturing apps Exposes the diagrammatic arrangements of NHETT and PHETT figures 1and 2 respectively.

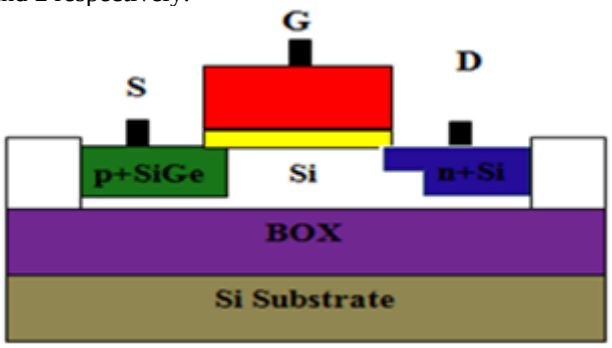

Fig.1. N-type HETT structure

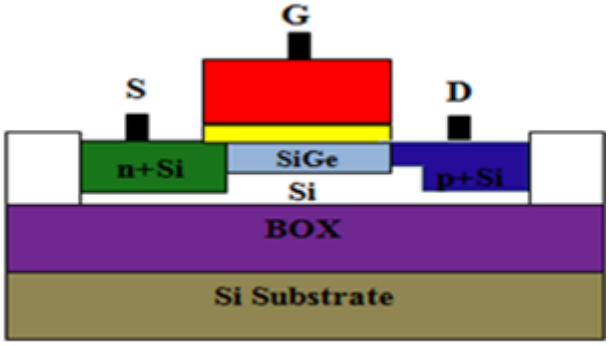

Fig.2. P-type HETT Structure

The proposed HETT device output drain characteristics and input-output characteristics are shown in figures 3 and 4 respectively. The output characteristics give the ON state drive current and input-output transfer shows the subthreshold swing which is the slope of this curve. The HETT with gate oxide over lapping device parameters are represented in the table. I. The fabrication of HETT is not different from MOSFET in CMOS technology. It is compatible to CMOS technology with little modifications in the fabrication steps. The proposed fabrication steps of HETT are illustrated in the flow chart of fig. 5. The CMOS technology is good for the logic implementation where as HETT technology is good for the semiconductor memory such as SRAMs. In future, both CMOS and HETT technologies are combined together for the design and implementation of portable digital systems for ultra-low power embedded applications.

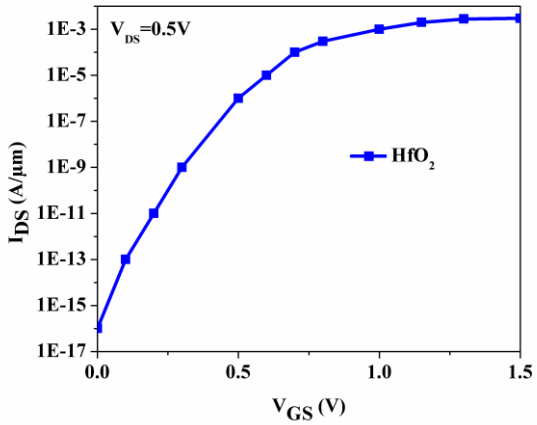

Fig.3. Output drain characteristics of proposed HETT

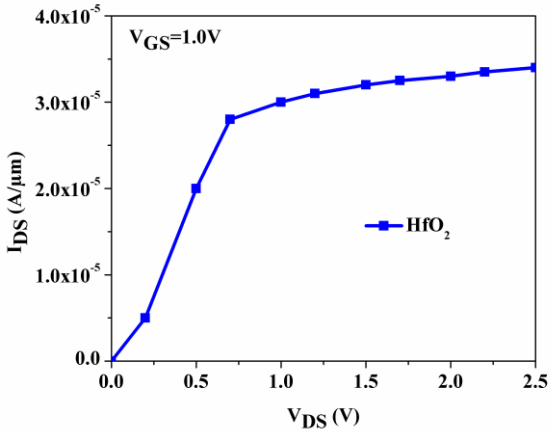

Fig.4. Input-output characteristics of proposed HETT

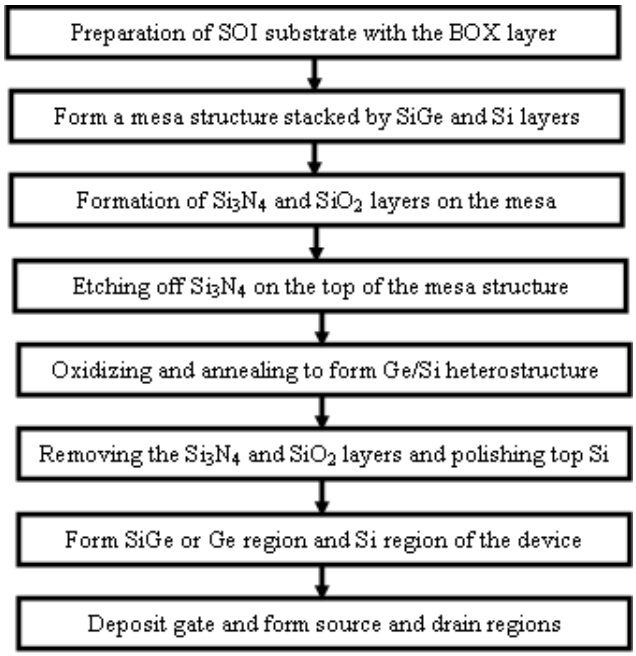

Fig. 5. Process flow of HETT fabrication

Table I Parameters of HETT device

Parameter	
Source material	p^+ SiGe
Drain material	n^+ Si
Channel material	Si
Source Doping Concentration	$5X10^{19}cm^{-3}$
Drain Doping Concentration	$5X10^{18}cm^{-3}$
Channel Doping Concentration	$1X10^{15}cm^{-3}$
Dielectric Constant(k)	15.4
Body Thickness	5µm
Bandgap of InAs	0.5437eV
Bandgap of $In_{0.53}Ga_{0.47}$	0.9130eV
Effective Oxide Thickness(EOT)	1.2nm
Channel length	20nm
Supply Voltage/Operating Voltage	1.2V

III. DESIGN AND IMPLEMENTATION OF 6T SRAM

The primary components of integration plan are implementation path & storage essentials. Due to small leakage and elevated drive present with enhanced Miller capacity, SRAM is suggested to the memory layout of small energy in HETT devices. Regular 6T SRAM cell includes two coupling inverters with two transistors for entry passes. In this construct, conventional MOSFETs are substituted by HETTs to enhance SRAM efficiency by decreasing the leakage energy.

The figure.6 and figure.7 exposes the 6T SRAM cell schematic lines and arrangements in the MOSFET & HETTs. The organization design shall be physically verified applying the Mentor Graphics Calibre tool that contains LVS, XRC DRC. In the production of low potential integration processors, the business utilizes these designs.

The 6T SRAM memory cell consists of six transistors, out of which four transistors forms basic memory unit with two cross coupled inverters to store one bit. The remaining two transistors act as pass transistors to access data from the memory unit. WL is the control signal that can be enable the user to read or write the data into the memory unit. If WL is 1, the data can be read or write. If WL is 0, then it is hold state .Pre-charge capacitors are used to identify the logic 1 or 0 at the inputs. BL and BLB are two complementary inputs used in the 6T SRAM memory design. The same data and control signal are also used in the HETT based design with same W/L ratios of the transistors.

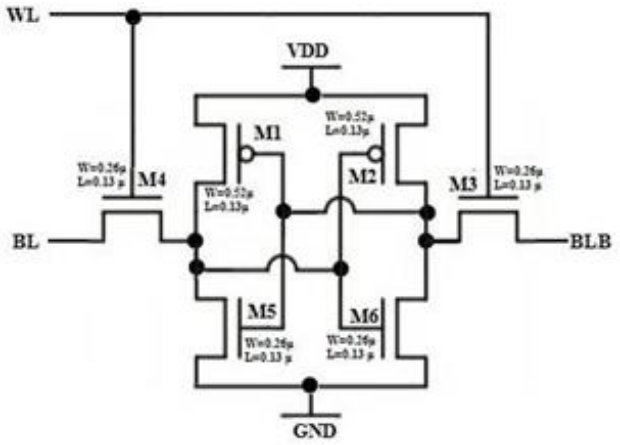

Fig. 6: Schematic Circuit 6T SRAM

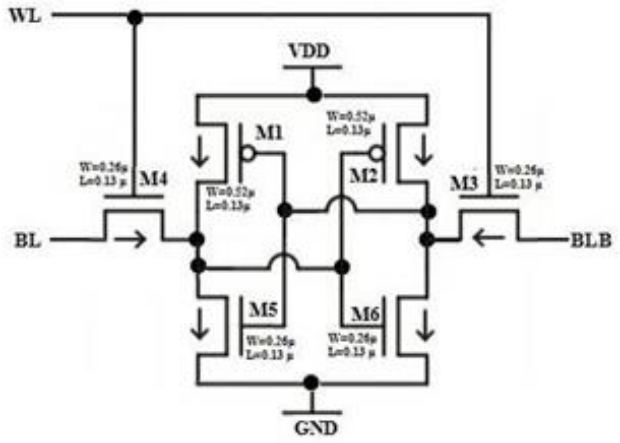

Fig. 7: Schematic Circuit 6T SRAM using HETT

The layout diagram is the last level of abstraction which gives the complete details required for the physical design of SRAM. The design rules must be followed while design the layout. The speed of the design is decided at this level of abstraction. Figure 8 and figure 9represents the layouts of 6T SRAMs using both MOSFET and HETT respectively. The Mentor graphics tool is used for the implementation of both 6T MOSFET based SRAM and 6T HETT based SRAM. The internal resistance, parasitic capacitances and delays are the parameters decided at the layout level of abstraction.

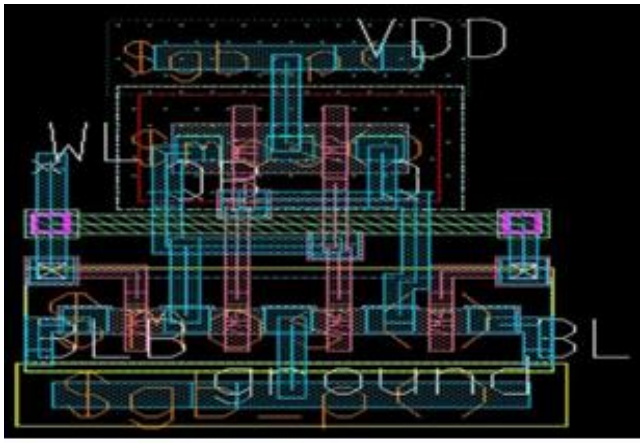

Fig.8: 6T MOSFET SRAM Layout

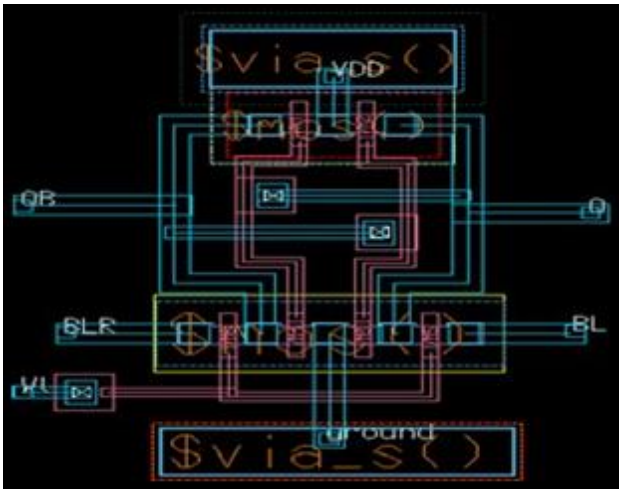

Fig.9: 6T HETT SRAM layout

IV. RESULTS AND DISCUSSION

Gate oxide intersecting of NHETT and PHETT at source are built but HETT 6T SRAM verifies the performance at these devices; performance validated with traditional 6T MOSFET SRAM. The reduced threshold swing of the device can create high change in current w.r.t. input voltage changes and hence low voltage is enough to create sufficient drive current by using HETT with oxide overlapping. Compared to MOSFET based design, HETT based designs dissipates consumes reduced powers. Temperature is one of the critical parameter in the CMOS VLSI design which effects the power consumption of the device. Table 2 presents the topology power analysis at different temperatures, i.e. SRAM cell median power consumption, maximum energy, and minimum energy.

Table 2: Power dissipation of 6T MOSFET SRAM

Temperature	Average power (µW)	Maximum power (µW)	Minimum power (µW)
0°C	0.805	38.718	0.0082
10°C	0.861	40.125	0.0673
25°C	1.093	51.223	0.1278
40°C	1.696	54.148	0.0357
50°C	1.887	55.787	0.2186
60°C	1.945	41.246	0.2451

Table 3 illustrates the 6T HETT SRAM proposed topology power dissipation at distinguishable changes in temperature. The power of 6T SRAM using HETT is better reduced than 6T MOSFET based SRAM. At room temperature i.e. 25°C, the power dissipation is better reduced than MOSFET based designs due to the heterojunction transistor with overlapping technique of oxide and low bandgap materials. Hence these devices are considered in the semiconductor memory design for all electronic gadgets for portability. Battery backup becomes better for design.

Table 3: Power dissipation of 6T HETT SRAM

Temperature	Average power (µW)	Maximum power (µW)	Minimum power (µW)
0°C	0.717	38.730	0.0083
10°C	0.809	40.959	0.0642
25°C	0.934	48.464	0.0132
40°C	1.048	48.033	0.0268
50°C	1.133	48.033	0.0268
60°C	1.302	35.385	0.0409

Average power consumption of proposed HETT-based SRAM is shown in table 4 at separate temperatures relative to 6T MOSFET SRAM and the average similarity of power consumption is illustrated by figure 10. At 25°C, HETT SRAMs average power comparatively small,

Table 4: 6T SRAMs average power consumption

Temperature	Average power of 6T MOSFET SRAM (µW)	Average power of 6T HETT SRAM (µW)
0°C	0.805	0.717
10°C	0.861	0.809
25°C	1.093	0.934
40°C	1.696	1.048
50°C	1.887	1.133
60°C	1.945	1.302

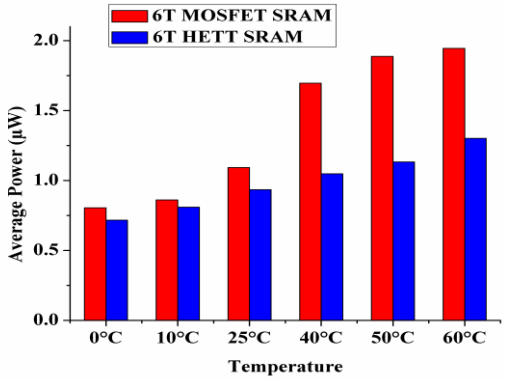

Fig.10. Average power evaluation of 6T SRAMs

In the low energy VLSI system, the peak and least energy of the system performs the desired part and is given. There highest potential of the modified 6T HETT SRAM is lowered at distinguishable temperatures corresponding to 6T MOSFET SRAM and is describing in Table 5 and the maximum energy ratio has exposed in Figure. 11. At room temperature, maximum power is well behind the MOSFET SRAM.

Table 5: 6T SRAMs maximum power

Temperature	Maximum power of 6T MOSFT SRAM (µW)	Maximum power of 6T HETT SRAM (µW)
0°C	38.718	38.730
10°C	40.125	40.959
25°C	51.223	48.464
40°C	54.148	48.033
50°C	55.787	48.033
60°C	41.246	35.385

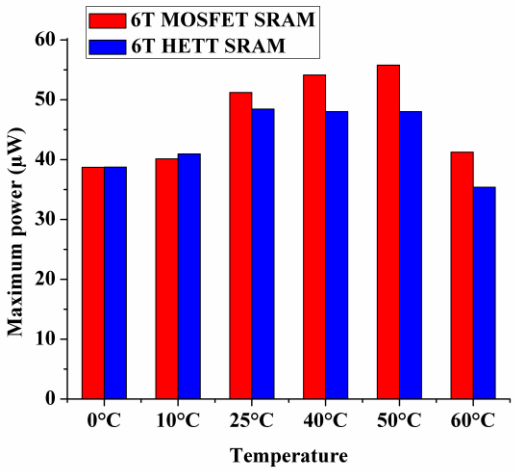

Fig.11: Maximum power evaluation of 6T SRAMs.

Matched to 6T MOSFET SRAM, suggested HETT SRAM minimum energy relying on HETT is decreased at distinct temperatures and is displays displayed in table 6. The minimum power evaluation of 6T SRAMs illustrated in figure 12. At normal temperature, HETT SRAM minimum power is reduced.

Table 6: 6T SRAMs minimum power

Temperature	Minimum power of 6T MOSFT SRAM (µW)	Minimum power of 6T HETT SRAM (µW)
0°C	0.0082	0.0083
10°C	0.0673	0.0642
25°C	0.1278	0.0132
40°C	0.0357	0.0268
50°C	0.2186	0.0268
60°C	0.2451	0.0409

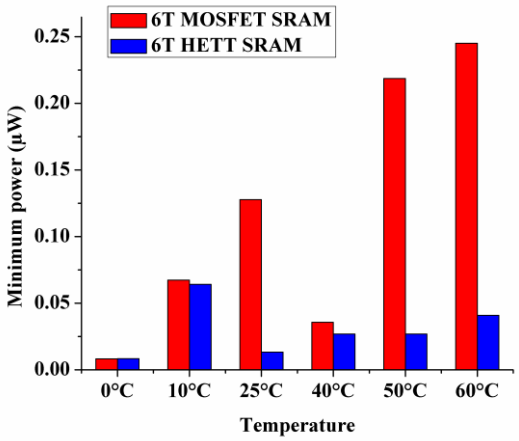

Fig.12: Minimum Power evaluation of 6T SRAMs.

Fig 7, Fig 8 and Fig 9 show that average power consumption, most energy and least 6T SRAM cells power based on HETT is lessened related to 6T MOSFET SRAMs greater than 40° C and therefore HETT SRAM cells are more helpful in more-temperature lower energy industrialized purpose. Because HETT offers better drive current, lower loss, then enhanced Miller power has decreased sub-threshold and helpful to apps with ultra-low voltages.

V. CONCLUSION

The HETT with the gate electrode overlapping the origin to amplify the closed circuit state current and reduce the leakage voltage with improved Miller capacitance ability is designed and implemented. HETT becomes the best solution to overcome MOSFET's circuit constraints for beyond-CMOS systems. HETT-based 6 T SRAM cell was described in this paper for ultra-low power applications using the modified Heterojunction transistors. The analysis of HETT SRAMs power w.r.t. various thermal temperatures with traditional memory cell is described and presented in detail. The average power of the proposed design is reduced by 14.54% compare to traditional approach. Similarly, the maximum and minimum powers are also reduced by 5.38% and 89.67% respectively compared to MOSFET 6T SRAMs. The low leakage power or standby power is added benefit of HETT. The HETT structure is friendly to CMOS and acceptable for applications with energy efficient memory. In digital mobile logic systems, preferably the mixture of CMOS and HETT techniques were used. The digital logic is implemented by CMOS where as memories are implemented by HETTs.

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