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A Low Power, High Speed 18-Transitor True Single-Phase Clocking D Flip- Flop Design In 90nm Cmos Technology

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***Abstract:** In this paper the authors came up with a contemporary low power, high-speed 18- transistor true single-phase clocking D flip-flop (FF) design using complementary pass-transistor logic. This design is a master-slave-type logic structure and hybrid logic design consisting of complementary pass-transistor logic style and static CMOS logic style. In order to reduce the number of transistors and to simplify the circuit complexity complementary pass-transistor logic style is used. In this design state transition is faster in the slave latch which enhances time performance using a virtual VDD technique. The circuit is designed using GPDK 90nm CMOS technology and the simulation results show better performance indices such as average power consumption, clock- to-Q delay, data-to-Q delay, PDP and area of utilization.*

***Keywords:** low power, flip-flop, true single-phase clocking (TSPC), complementary pass-transistor logic (CPL).*

I. INTRODUCTION

Memory units in VLSI based battery operated portable electronic devices are made up of FF's. In those kinds of battery working equipment such as healthcare-associated equipment and internet of things (IoT), power reduction is a very important issue. In the design of any VLSI applications area, power and delay are major issues. FF can store one bit of data. FF is a basic storage element it can be clocked or un- clocked. A latch is known as un-clocked FF. FF's work along with the clock distribution network in the digital system design, so the power consumption of FF constitutes 20% to 45% of the total system power. FF designs in the digital system design are crucial to power consumption performance

and may affect the chip area. The memory units in digital camera, tablet pc, mobile phones are made up of FF's.

The objective of TSPC FF designs is lowering the clock signal loading because, here only one phase of the clock is used. Cross-coupled set-reset latches were used instead of the Transmission gate based latch for supporting single-phase-clock operations. TSPC is high-speed topology which consumes low power and occupies less area. TSPC used in various applications like digital VLSI clocking system, buffers, and microprocessors etc.

The most popularly used FF design is the transmission gate based FF (TGFF) design. In TGFF the clock driven transistors are 12 and transistor count is 24. In this design, excessive workload on clock signals to generate complementary signals. Set-reset latch based FF (SRFF) design has transistor count 30 and the number of clock driven transistors is 10. This design has high dynamic power consumption even though the data switching activity is low, because of high capacitive clock loading problem.

T. Sakurai and H. Kawaguchi proposed a reduced clock swing FF (RCSFF) [1]. To reduce clock power, it was the oldest method. This design has a cross-coupled slave latch and master latch which is true single phase. Due to true single-phase nature of FF it accepts reduced voltage swing as low as 1V. This design reduces RC delay, area and power when compared to conventional FF, but the power was not reduced as required. B. Nikolic, J. K. S. Chiu, W. Jia, V. G. Oklobdzija, M. M. T. Leungand V. Stojanovic, proposed improved sense amplifier based FF (SAFF) design in [2]. This design has high speed when compared to all other FF designs. This FF has strong driving capability and used in the GHz design with high fan-out and a small pipeline.

V. Stojanovic, V. Oklobdzija, N. Nedovic, and D. Markovic, discussed about Digital System Clocking [3]. They described about clock generation and the clock distribution and the various clock signals and their phases. V. G. Oklobdzija and V. Stojanovic, in [4] provides the analysis of flip-flops and masters lave latches for low-power systems and high-performance. They provide set of rules for calculating performance and power of master-slave latch structures. FF.

V. G. Oklobdzija, discussed the methods for measuring the timing parameters of FF like hold time, setup time, power delay product (PDP), clock-to-Q (CQ) delay, data-to-Q (DQ) delay and average power consumption [5]. M. Hamada, H. Hara, C. K. Teh, and T. Fujita proposed Adaptive Coupling FF Design (ACFF) by using Adaptive Coupling Technique [6]. ACFF uses a pass transistor logic with differential latch structure for obtaining operation of TSPC. This design uses two adaptive coupled elements which consists a pMOS and a nMOS transistor connected in parallel whose sources and drains tied together and same data applied to gates. It has total 22 transistors and only 4 transistors are driven by clock. ACFF suffers from power leaking problem and has a longer setup time.

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M. Kawai proposed Topologically compressed FF Design (TCFF) by using Topologically compressed scheme [7]. It is TSPC design with SR-latch based structure which is based on various optimization measures such as single-phase clock is used, reduces transistor count to 21 and only 3 clock driven transistors are used. TCFF suffers from longer setup time.

II. LOGIC STRUCTURE REDUCTION FF DESIGN

Ming-Hwa sheu, Jin-Fa Lin proposed Logic structure reduction FF Design (LRFF) [8] which is the enhancement of TCFF. LRFF uses various optimization measures such as logic reduction for achieving small setup time, circuit simplification for lowering the power consumption and elimination of static power leaking problem by avoiding node floating case. In this design, only 4 clock driven transistors and transistor count is 19. This design suffers from poor hold time performance.

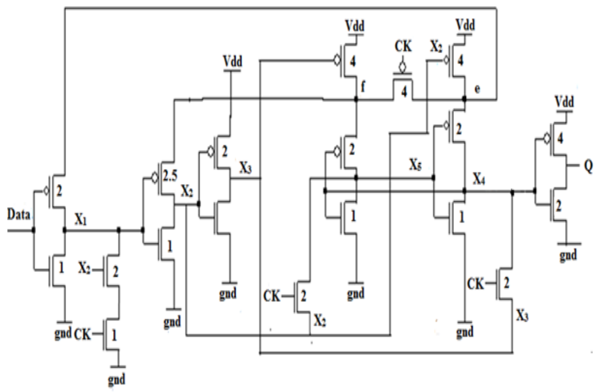

Figure 1: Logic Structure Reduction FF design

III. PROPOSED FF DESIGN USING CPL

Logic structure gives a clear definition of objective and the starting point indicator. They conserve the defects of previous problems and provides alternative solutions which identify the problems and checks whether all objectives are covered. In existing LRFF design, 19 transistors were used which increases delay, power consumption, and area of utilization. To reduce the number of transistors and to simplify the circuit complexity complementary pass-transistor logic style is used.

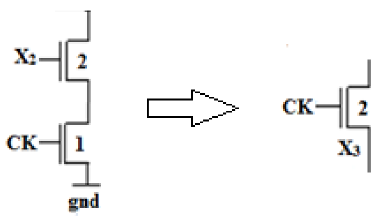

Figure 2: CPL Structure

CPL uses complementary inputs/outputs in nMOS pass-transistor logic along with CMOS output inverters. Here nMOS network is used for implementing the logic functions and for driving the outputs CMOS inverters are used. CPL consumes low power because of the pass- transistor outputs smaller than the supply voltage level, and the outputs are equal to supply voltage level in static CMOS circuits. CPL has many advantages like the high speed of operation, low input capacitance and consumes low power. In CPL structure shown below two series nMOS transistors replaced by one nMOS transistor. X2 signal is a complementary signal of X3.

In LRFF design a total of 19 transistors are used so the power consumption, area of utilization and delay increases, they can be reduced by using the CPL. This design is a master- slave-type logic structure and hybrid logic design consisting of complementary pass-transistor logic style and static CMOS logic style.

In LRFF design [8] the two series nMOS transistors in master latch whose inputs x2 and CK can be replaced by one transistor whose gate is driven by CK and x3 is connected to source. Here x2 signal is a complementary signal of x3. So, instead of two transistors only one transistor is used, it reduces the transistor count to 18 and improves the overall performance of the FF design when compared to existing design LRFF.

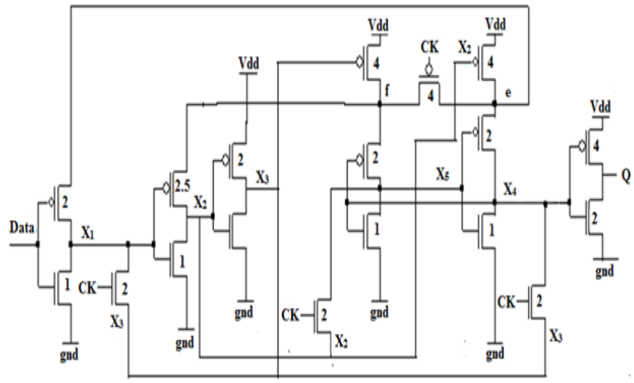

Figure 3: FF design using CPL

The proposed FF design operation is initiated when Clock (CK) is low and Data=0, the master latch is transparent which means whatever may be the input it is reflected at the output of master latch, data input is stored and slave latch is in hold state which means no data is transferred to slave latch from the master latch. When Data=0 and CK is high master latch is in hold state, data saved in the master latch is applied to the slave latch and reflected at the output as Q because slave latch is in transparent mode.

IV. RESULT AND DISCUSSION

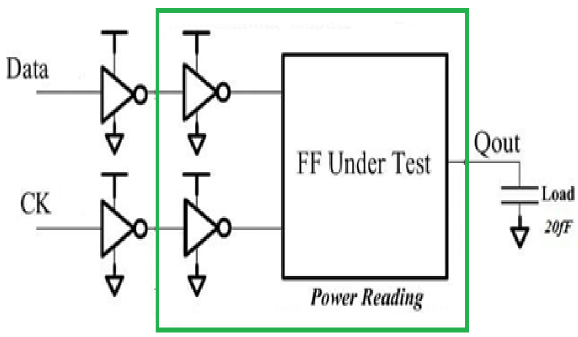

Figure 4: Model setup for FF simulation

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The FF designed in cadence virtuoso using GPDK 90nm CMOS technology. The simulation results of proposed FF design various performance indices setup time, hold time, PDP, average power consumption, CQ delay, DQ delay, Layout area are calculated.

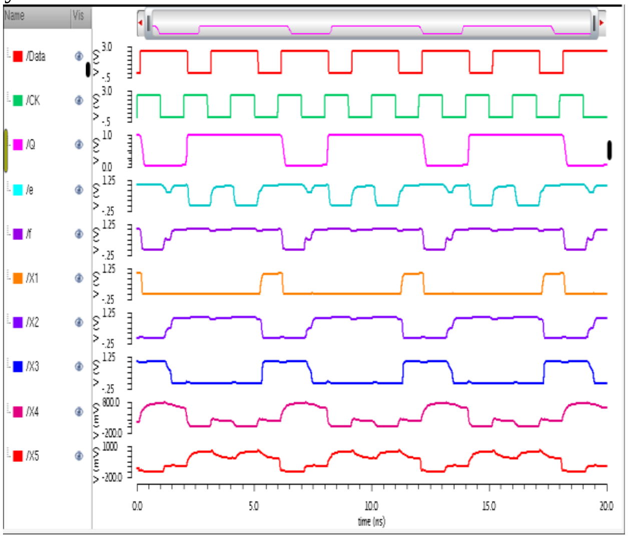

Figure 5: Simulation Waveforms of CPL FF Design at 500 MHz / 1 V

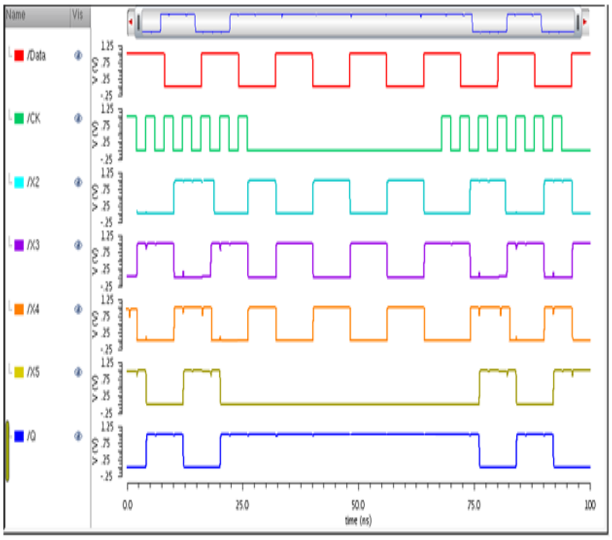

Figure 6: Sleep mode Simulation Waveforms of CPL FF Design

Suspending clock signal is standby mode and wake up procedure is resuming clock signal and new data is loaded to the FF. Once the clock is reactivated the FF starts its function immediately and logic Transitions are performed. In sleep mode simulation, the input is starting with 7 cycles and followed by 10 cycles of standby mode.

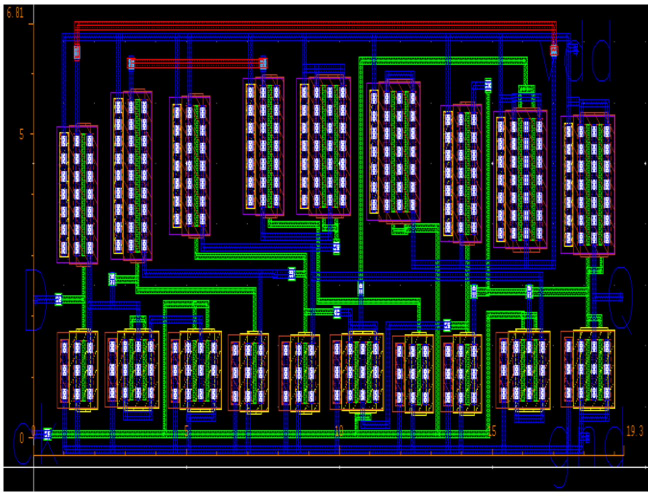

Figure 7: Layout of LRFF Design

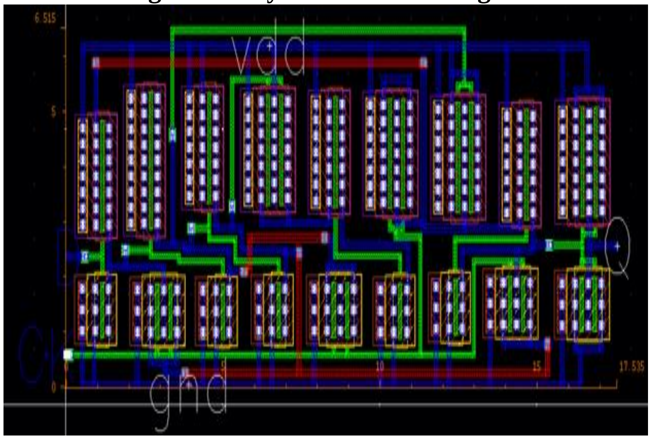

Figure 8: Layout of CPL FF Design

The performance evaluation of FF includes transistor count, layout area, power consumption at different data switching activities, PDP and various timing parameters as shown in Table 1.

Table 1: Feature Comparison of LRFF and CPL FF Design at 500 MHz/1 V

Flip-Flop Design	LRFF	CPL
Number of Transistors	19	18
Layout Area (μm^2)	131.24	113.75
Setup Time (pS)	123.4	120.5
Hold Time (pS)	10.0	10.3
CQ Delay (pS)	187.9	164.4
DQ Delay (pS)	311.3	284.9
Average power at 100% Switching Activity (μW)	45.62	43.09
Average power at 50% Switching Activity (μW)	26.33	24.27
Average power at 25% Switching activity (μW)	17.10	15.09
Average power at 12.5% Switching activity (μW)	12.39	9.65
Average power at 0% Switching activity (μW)	7.81	5.92
PDP_{CQ} at 12.5% Switching Activity (fJ)	2.32	1.58
PDP_{DQ} at 12.5% Switching Activity (fJ)	3.85	2.74

At different data switching activities the values for average power consumption, CQ delay, setup time and hold time are evaluated for both FF designs. DQ delay is the sum of the CQ delay and the setup time. PDP is a figure of merit correlated with logic gate energy efficient. It is the product of duration of the switching event data and the average power consumption. for different supply voltages power and delay are calculated.

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The below figures 9 and figure 10 shows PDPCQ and PDPDQ values subjected to various input switching activities which indicate that CPL FF design has low PDP values when compared to LRFF design. Lower the PDP higher the performance.

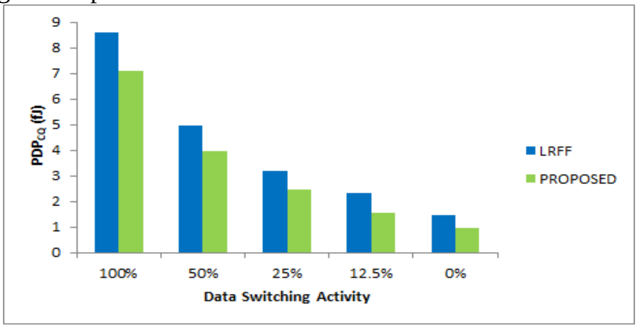

Figure 9: PDPCQ versus Data Switching Activity

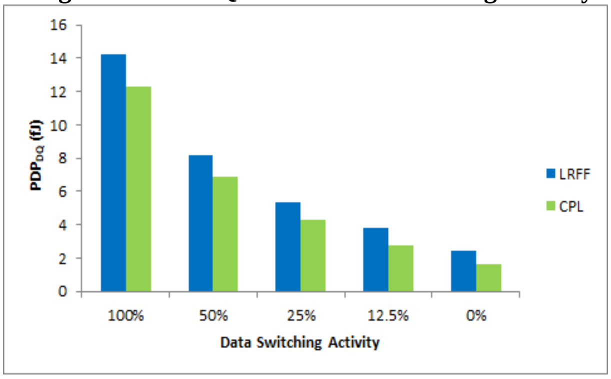

Figure 10: PDPDQ versus Data Switching Activity

The performance of the FF design is based on the power consumption and delay. CPL FF design has low power consumption than LRFF design. The below figure 11 shows power values of both LRFF design and CPL FF design at various supply voltages. CPL FF design has low power consumption than LRFF design.

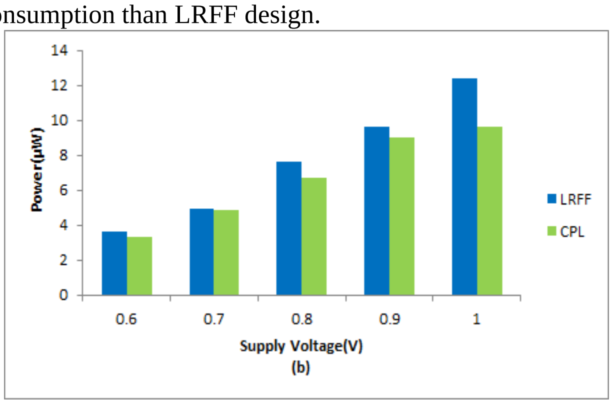

Figure 11: Power Consumption values at various Supply Voltages

The below figure 12 shows clock to Q delay values of both LRFF design and CPL FF design at various supply voltages. CPL FF design has high performance than LRFF design.

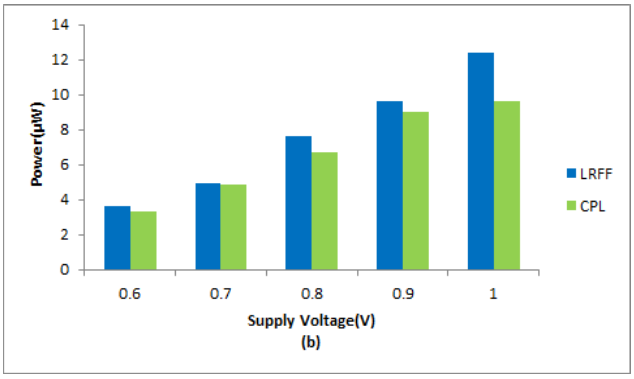

Figure 12: Clock to Q Delay values at various Supply Voltages

At different process corner simulation cases fast-fast (FF) simulation (1.2 V/ -40º C), slow-slow (SS) simulation (0.8 V/ 25º C) and typical- typical (TT) simulation (1 V/ 25º C) the values of PDPCQ are measured and shown below in figure 13. Process corners are used to verify the robustness of integrated circuit design. Process corner analysis is used to know effect of process variations on speed of transistor during switching activity from one logic state to another.

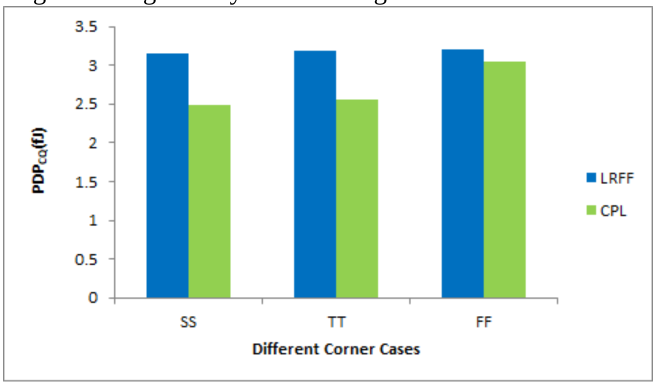

Figure 13: PDP performance at different corner cases

V. CONCLUSION

A new 18-transistor FF is designed using logic structure reduction consisting of complementary pass-transistor logic style and static CMOS logic style. The circuit complexity of the design reduced for better timing performance, low power, high speed and a small area of utilization. Simulations were performed in cadence virtuoso 90nm CMOS technology and the performance indices area, power, hold time, delay, setup time, PDP are evaluated. This design has 32% reduction in PDP when compared to existing LRFF design. The proposed design excelled existing FF design in all aspects.

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