Abstract. The design objective is to implement a Low power, High speed and High resolution Flash ADC with increased sampling rate. To make this possible the blocks of ADC are analyzed. The resistive ladder, comparator block, encoder block are the major modules of flash ADC. Firstly, the comparator block is designed so that it consumes low power. A NMOS latch based, PMOS LATCH based and a Strong ARM Latch based comparators were designed separately. A comparative analysis is made with the comparator designs. Comparators in the design is reduced to half by using time domain interpolation. Then a reference subtraction block is designed to generate the subtraction value of voltages easily and its given as input to comparator. Then a more efficient and low power consuming fat tree encoder is designed. Once all the blocks were ready, a 8 bit Flash Analog to Digital Converter was designed using 90nm CMOS technology and all the parameters such as sampling rate, power consumption, resolution were obtained and compared with other works.

I. INTRODUCTION

Fields of ADC usage include medical, radar, data acquisition.

Modules of general flash ADC

• Reference r-ladder
• Voltage input
• Comparator
• Encoder logic

To make the Flash ADC more efficient, we have dealt with some basic key issues of Flash ADC such as speed, performance, area and power consumption by using some techniques.

II. PROPOSED SYSTEM

Fig. 1. Flash ADC Block

Design Of Two Stage Dynamic Comparator With NMOS Latch

Fig. 2. Block Diagram for the Flash ADC

Fig 3. Flow for the Comparative Analysis of the Comparator

Fig 4. Twostage Dynamic Comparator with NMOS Latch

Fig. 5. Block Diagram for the Flash ADC
To set the gain higher, the transistor M3,4 are chosen to have an appropriate size. But the delay parameters are controlled by offset which can be overcome by a pmos latch.

Fig 5. Schematic Of NMOS Latch Based Comparator In Cadence

Fig 6. Output Obtained For Precharge And Evaluation

Fig 7. Power Consumption Of Nmos Latch Based Comparator
Design Of Two Stage Dynamic Comparator With PMOS Latch

Fig 8. Twostage dynamic comparator with pmos latch and local clock generator.

Fig 9. Dynamic Comparator With Pmos Latch And Local Clock Generator

Fig 10. Output Obtained For Pmos Latch Based Comparator
A optimum delay is being defined in this type of comparator. It consists of a preamplifier stage where a local generator is designed which plays a major role. In the evaluation phase a predetermined delay is defined.

**Fig 11. Power Consumption Of Design Based On Pmos Latch**

*Design Of Two Stage Dynamic Comparator With Strong Arm Latch*

The strong ARM latch does consumes zero static power, rail to rail output is directly produced, the input referred offset arises from one differential pair. This makes the Strong ARM latch popular.

**Fig 12. Comparator Based On Strong Arm Latch**
In the reset phase, clock is low and the nodes A, B, C, D is precharged to vdd where transistor M2 is off. In the next phase-amplification mode, clock goes high, transistor M1 and M2 are on. This phase provides voltage gain.

Fig 13. Output Obtained For Strong Armlatch Based Comparator

Fig 14. Power Consumption Of The Design
Comparitive Analysis Of Powerconsumption Among The Comparators

Since ARMLATCH BASED comparator is consuming the least performance and has improved speed, we prefer this comparator for our proposed ADC design.

**TABLE 1.**

<table>
<thead>
<tr>
<th>S.NO</th>
<th>COMPARATOR TYPE</th>
<th>POWERCONSUMPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>NMOS LATCH BASED</td>
<td>886.43 μW</td>
</tr>
<tr>
<td>2.</td>
<td>PMOS LATCH BASED</td>
<td>249.253 μW</td>
</tr>
<tr>
<td>3.</td>
<td>ARM LATCH BASED</td>
<td>134.16 μW</td>
</tr>
</tbody>
</table>

Thus, we prefer the Strong ARM Latch comparator (Lowest power consuming) in the proposed Flash ADC design.

**III. TIME DOMAIN INTERPOLATION OF THE COMPARATOR:**

Its performing interpolation on a sequence of time domain samples. The time-domain interpolation follows the fact that, \( V_{in} \) +ve, here required for the flash adc is normally \( 2^N - 1 \). But after time domain domain interpolation it has been halved as \( 1/2(2^N - 1) \).

![Fig 15. Time Domain Interpolation Unit In Cadence](image1)

![Fig 16. Output Obtained For The Time Domain Interpolation](image2)
IV. FAT TREE ENCODER & RESULTS

It is preferred that is highly suitable for ultrahigh speed
flash ADCs and the speed is improved by a factor of 2.

Fig 17. Fat Tree Encoder Block

V. PROPOSED 8BIT FLASH ADC

The Reference generated is subtracted with the voltage
input and is fed to the comparator. The output generated
from the comparator, which is of digital bits and its encoded
by using fat tree encoder. This fat tree encoder has higher
performs, speed and the area it consumes is lower. Thus the
Flash ADC is analyzed by the transient response in cadence
and the power consumed, sampling rate, resolution and SNR
are being calculated.
A 1000 Mhz Low Power And High Speed 8-Bit Flash ADC Architecture Using 90nm CMOS Technology

Fig 19. 8BIT Flash ADC

Fig 20. Analog Input Fed

Fig 21. Converted Output Of The ADC
Fig 22. Power Plot For The Designed ADC

VI. CONCLUSION

TABLE 2.

<table>
<thead>
<tr>
<th>PARAMETERS ANALYZED</th>
<th>PROPOSED DESIGN</th>
</tr>
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<tbody>
<tr>
<td>Resolution</td>
<td>8</td>
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<tr>
<td>Power consumption</td>
<td>6.785mW</td>
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<tr>
<td>Sampling rate</td>
<td>1000MHz</td>
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<tr>
<td>SNR</td>
<td>49.92dB</td>
</tr>
<tr>
<td>Architecture</td>
<td>Time domain interpolated ADC</td>
</tr>
<tr>
<td>Technology</td>
<td>90 nm</td>
</tr>
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</table>

VII. COMPARITIVE ANALYSIS

This research paper analyzes the Flash ADC the parameters transient response, power consumed, sampling rate, resolution and SNR using Cadence EDA. And also we compare the different parameters analysed using 90nm technology. By comparing with existing methods, this circuit provides higher SNR. In future we analyse by using different technology (i.e 45nm, 65nm).

IX. REFERENCES

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