Design a High Speed Multiplier using Two Phase PPA

Gajula Lakshminarayana, Moparthy Gurunadha Babu, Anupama A. Deshpande

Abstract— Basically, multiplier is an efficient superconductor logic which performs various switching operation. Here different types of adders are analysed using different methodologies. In this paper we introduced a multiplier using proposed PPA. It uses parallel prefix adders in their reduction phase and it is an effective system for faster results and optimised. The entire operation of proposed system depends upon three stages they are multiplier partial product generation, reduction stages and parallel prefix adder which is discussed in below sections. The delay gets reduced by achieving low logical depth in the system. So the Proposed system reduces the delay. From the proposed system we can observe that there is a reduction in delay and complexity. Compared to ripple carry adder and carry save adder, proposed system gives better results.

KEYWORDS: PPA, VLSI, DSP, Partial Product Generation (PPG).

I. INTRODUCTION

As we know that in the areas of system on chip and VLSI designs, the low power circuit designs is an important issue. In the sub micro regions, the transistor produces the leakage currents which are very significant in nature. This leakage current is controlled by introducing the new designs. Two logics are used mainly to improve the performance, adiabatic logic and asynchronous logic. Compared to the static CMOS logic design, the adiabatic Logic uses less power to perform the operations. So adiabatic logic is most used in low power applications. Here to solve the problems of heavy global clock loading and clock skew, asynchronous and synchronous circuit's designs are used. Compared to synchronous circuits, the asynchronous circuits produce more power consumption.

As we know that addition, multiplication and subtraction operations are performed in any system. While executing the multiplication operations, large numbers of problems are obtained related to computations. Because of this changes are occurred in the speed of the system. In DSP systems multiplier plays an important role. But in DSP system mostly they perform filtering and convolution operations. Instead of that the multiplier operation plays very crucial role in DSP systems.

Different types of adders are proposed before. Depend upon the parameters adder is used. But if the speed is main constraint then we supposed to use this parallel prefix adder. In very large scale integrated circuits, parallel prefix adder is mostly used. The parallel prefix structures allow trade-offs to obtain required logic levels. Depending upon the adder performance the digital signal processor produces accurate results.

Basically, ripple carry adder is obtained from the general purpose processors and DSP processors. Repetitive additions are performed by using multiplier operand. But using propagation, the quality, Delay, and area is measured. In ripple carry adder first the carry propagation is overlapped and next addition operation is performed. But the ripple carry adder produces large delay in the system. To overcome this delay problem parallel prefix adder is invented. This adder produces faster operations, reduces power consumption and delay. To add more number of numbers together, powerful adders should be used.

Basically, parallel prefix adder produces high speed multi operands. The scaling down of device dimensions into the Nano-meter range is likely to result in significantly higher defect rates during the manufacturing process of IC's. With significantly increased defect rates, defect tolerance mechanisms are necessitated to guarantee a reasonable yield. Post manufacturing reconfiguration techniques to bypass defects are already applied in memory systems and FPGA's. However, such low-cost defect tolerance techniques rely heavily on the relative independence of operations of the homogeneous components, such as LUT and memory cells. Logic systems, on the other hand, usually constitute heterogeneous components with strong dependencies among each other. This makes it hard to realize fine-grained, low-cost defect tolerance schemes for a high level of defect rate.

The advantages of proposed system is given as 1) compared to CMOS, the PPA multiplier produces low power consumption, 2) frequency range is from 5-10 GHZ, 3) compared to conventional RSFQ logic, the PPA multiplier is very simple.

.II. LITERATURE SURVEY

The simplest way to perform multiplication is to use adders and gates. Digital multiplier is a great event arithmetic unit used in DSP. There are various types of multipliers are existed. Basically, the addition operation is performed effectively in electronic applications. The main component used in adder is ALU which is defined as

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arithmetic and logic unit and it consists of multiple adders. Depend on the numerical expressions like Excess code. Binary code decimal the adder is constructed. They perform the operation using binary numbers. For example for single bit operations two inputs are used. Let us consider half adder consists of A and B inputs and sum & carry as outputs. Here s performs the XOR operation using A and B inputs and CO will performs the AND operation using A and B inputs. This about half adder, Coming to full adder it consists of three inputs which are givens as A, B, Cin. The full adder is constructed depend on the half adders.

In ripple carry adder, multi bit adder is used. But it does not produce effective results and slower operations are performed. Coming to carry look ahead adder, it will propagate the bit position of system. in some cases the half adder produces sum output as P and carry output as G. Depend on the carry by pass adder, the length of carry is determined. By using p and g values time is determined.

In Array multiplier they are two methods 1) least significant digit and 2) most significant digit. In most significant digit the complexity of multiplier is lower. Basically, the flip flop will shift the bit positions cyclically at every cycle and produce outputs using XOR gate operations. Here less number of registers are required in exited multiplier. But here the issue is same number of gate and registers are used. because of this the dealy is increased in existed system.

Array multiplier save Fourier transistors when compared with standard method. Bit for proposed multiplier 2KM transistor is used at every digit of the system. This will save the system memory in effective way. Hence lower power consumption is obtained from the proposed design of multiplier. Almost both pin & psw are unchanged. Because of this there will be reduction in dynamic power. To reduce the critical path delay and area of a digital - serial PB multiplier in GF (2^8) the same procedure will be applied. The existed system shows that how much power is consumed on multiplier after applying factoring method.

Our first parallel prefix adder architecture depends on the architecture of adder. The 1 bit parallel-adder computes the entire process and here an exclusive-NOR gate and n bit adder is composed in the system. Carry output obtained at the end of gate. Here the time should be minimized in computation process. Because of this the speed of the operation is increased. By using recursive equation each bit position is derived. In the same way using a single row of prefix operator the addition operation of carry bit is done in parallel.

By connecting carry inputs to carry increment stage the addition operation is performed. Here the design is recursively optimized to get better efficiency. Here extra carry increment stage is not used in the operation. Depend on the prefix level the addition operation is parallel prefix operation is performed. The structure of proposed system is shown in figure (1). Carry tree adders is also known as parallel prefix adders. From below figure (1) we can observe that the system is in tree structure. The proposed system pre computes the both propagate and generate signals. Lot of families of adders are implemented by the prefix network. The calculation of parallel prefix adder is done in parallel. Coming to the black cell it generates ordered pair and coming to the grey cell it generates left signal.

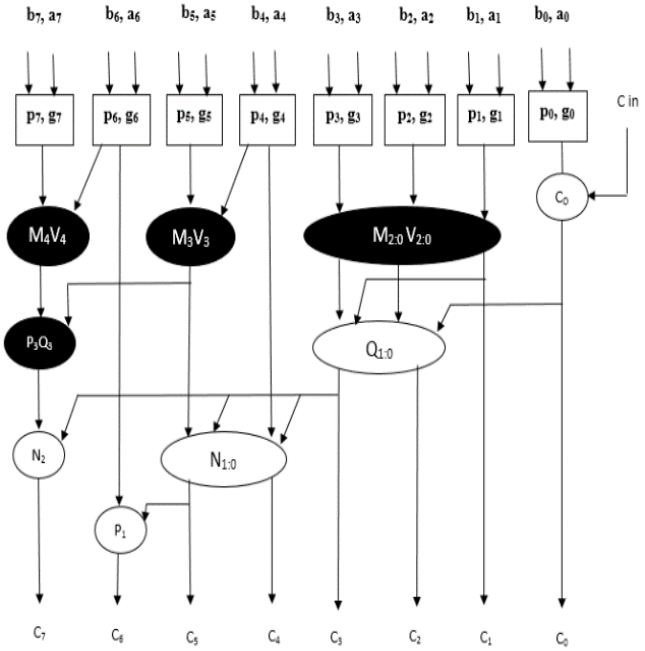

Fig. 1: Existed system

III. MULTIPLIER USING PROPOSED PPA

The main intent of parallel prefix adder is to generate the multiple bit numbers depend on the carry propagation unit. To get faster operation, the both generate and propagate signals are used. The below figure (2) shows the structure of multiplier using proposed PPA. As shown in fig (2) there are three stages to perform the entire operation. They are partial product generation, reduction stages and parallel prefix adder. Multiplicands are taken as input and output is taken as final product.

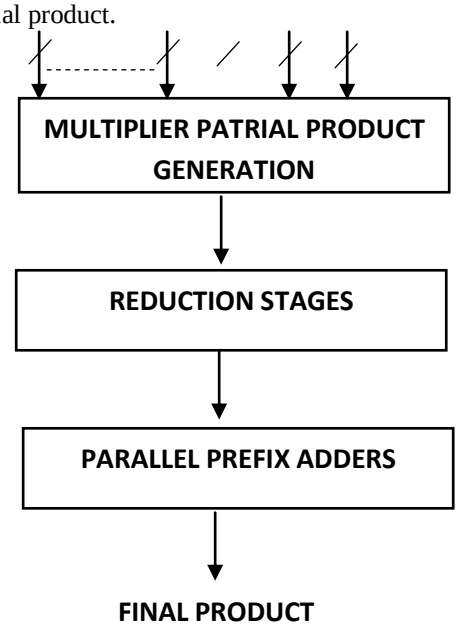

Fig.2: structure of multiplier using Proposed PPA

Many PPA architectures are existed but in this paper two low energy PPA multiplier are proposed. Highest critical paths are obtained because of increase in delay. Partial product generation gives low cost, power & delay. The generation stage compute the partial products which are grouped together. This system will rectify the problem of carry propagation in effective way. Based on the inputs given the outcome of operation is performed. As we know that the parallel prefix adder performs and executes the operation in parallel. The obtained output will be segmented into smaller pieces. There are different topologies used in parallel prefix adder, but the operator is associative. Based on topology the operation is performed.

To reduce the degree of PPA multiplier they use binary tress structure of XOR gates. The description of PPA multiplier by reducing the degree is given in detail manner. In PPA multiplier, Buffer plays important role to obtain constant cells. These constant cells divided into two logics, logic 0 or logic 1. The negative coupling coefficient is obtained by using asymmetric excitation fluxes. A complete set of combinational logic gates are obtained by introducing the 3 to 1 branch cells. Here the concept factoring of large number is not introduced. The key are generated by providing security which is more than digit length. Hence compared to others, the PPA multiplier produce prime value. Basically, the PPA multiplier is divided into logic rows which are connected together in effective way.

The below figure (3) shows the block diagram of proposed system. As discussed above that the entire operation depends on three stages.

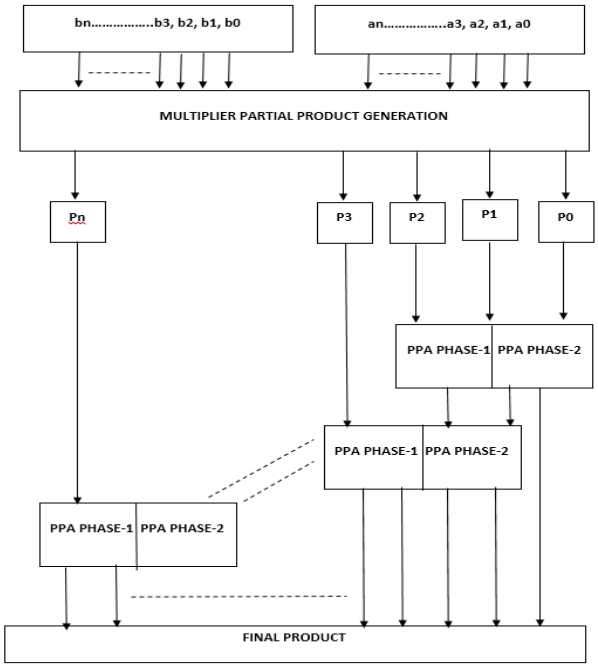

Fig. 3: Block Diagram of multiplier using proposed PPA

N inputs and N outputs are computed by using associative operator using parallel prefix circuits. The intermediate variables are added to the prefix network. Firstly N input bits are given to multiplier partial product generation. From this partial product generation, it can observe that all the inputs which are given will be multiplied. Now they can be split into propagate signals which are represented as P0, P1, P2 ….Pn. depend up on phase-1 and phase-2 the operation is continued. When compared to the results of existed system, the proposed system gives efficient results.

IV. RESULTS

In the previous section the scheme of multiplier using PPA is proposed. In this the schematic implementation, the derivation formulas has described. In traditional topologies the combinational logic design has preserved with input operands. From below figure (4) we can observe the comparison of logic delay between existed and proposed system.

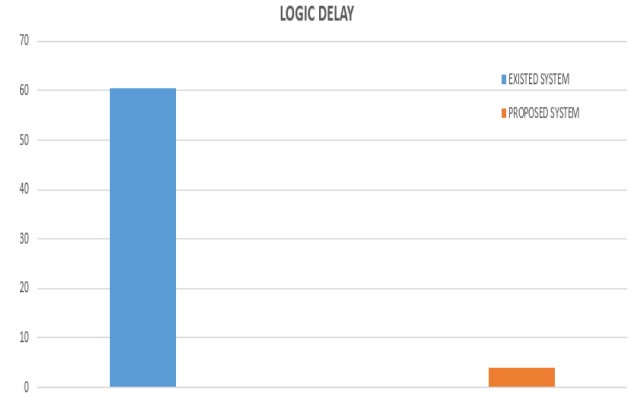

Fig. 4: Logic delay comparison of existed and proposed system

From below figure (5), we can observe the comparison of route delay of existed and proposed system.

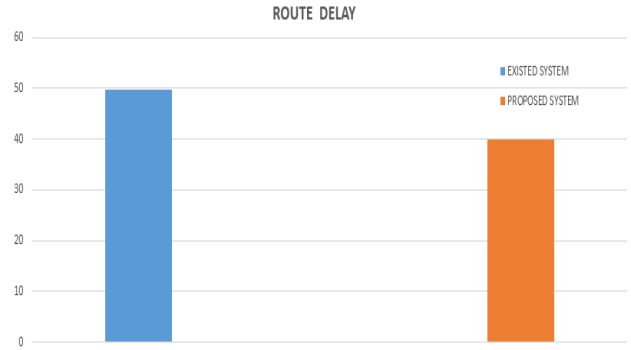

Fig. 5: Route delay comparison of existed and proposed system

From below figure (6), we can observe the comparison of overall delay of existed and proposed system.

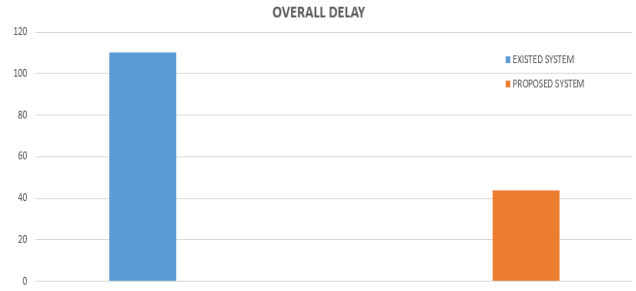

Fig. 6: Overall delay comparison of existed and proposed system

Table. 1: Delay comparison of existed and proposed system

Name	EXISTED SYSTEM	PROPOSED SYSTEM
Logic delay	60.608 ns	3.971 ns
Route delay	49.755 ns	39.86 3ns
Overall delay	110.363 ns	43.834 ns
Number of slices used	122%	4%

V. CONCLUSION

In CMOS circuits the energy stored is wasted by discharging depending on the signal present. It is not only difficult to realize CMOS technology but they also contribute to considerable power dissipation. In this paper the proposed system merges multiple logical and arithmetic functionalities. Here we presented existed system which gives poor performance delay. So a new system is proposed which works under three stages. From results it can observe that it gives the good output with better delay performance. The design methodology presented here should be applied well to a higher precision adder. The total circuit delay is better than CSA, RCA as shown in results.

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