



Design of 12-Bit SAR ADC using Split Capacitor Based DAC Architecture at 45nm CMOS Technology

Naveen I .G, Savita sonoli

Abstract: Nowadays, there is an increasing demand for Successive Approximation Register (SAR) based Analog to Digital Converter (ADC) in long battery applications like medical application, Sensors and many more. In this paper DAC circuit is designed using multiple capacitor and Multiple MUX for switching. A split based capacitor is used for boosting the speed of the architecture. In split based DAC no common mode voltage required and dynamic offset can be removed as well. In this work, 12-Bit DAC and encoder is designed using 2 Transistor MUX and 18 Transistor Full adders (12B-2TM-18TFA). 2T and 18T is used to design the MUX and FA. This entire architecture is implemented in Cadence Virtuoso 45nm CMOS technology. Simultaneously, 10B-12TM-36TFA architecture also implemented in this paper. The performance parameters like area, power, and delay, current is evaluated for both architectures. Result showed that 12B-2TM-18TFA architecture consumed less area, less power, less delay, and less current compared to 10B-12TM-36TFA.

Keywords : Analog to Digital Converter, Digital Analog Converter, Successive Approximation Register, 18T MUX, 2T MUX.

I. INTRODUCTION

SAR - ADC have become more preferred design for many low power VLSI applications in which design of capacitor based DAC play a very vital role. Analog and mixed circuit designs are too difficult to work under low voltages [1-2]. Normally, SAR-ADC is not preferred for high bandwidth applications, because it requires more clock cycle to obtain the N resolution (bit) [3]. In recent years, different techniques have been designed to lower the switching energy of capacitive DAC array [4-5] For example, Vcm based [6], switchback scheme [7], and Zhu [8] these achieve an average speed and average power of the entire design. Conventionally, Counter based digital control design [9], Capacitor switching technique [10], split capacitor DAC [11-12], histogram based [13] methods have been used earlier. But, each and every methodology have some limitation like oldest technology (180nm,90nm,65nm), require more area, consume more power (in mW), high current (mA), less resolution (less than 8-bit), architecture occupies more critical path and more number of transistors require to design the internal blocks. To overcome these

problems, 12B-2TM-18TFA design is implemented in this paper. This work is implemented on 45nm CMOS technology. Compared to existing architecture (10B-2TM-36TFA), 12B-2TM-18TFA architecture gives less area, power, delay and speed at higher resolution.

This research work is composed as follows, section 2 gives a literature survey of papers from earlier research works. The section 3 explained the proposed methodology with internal block of the entire design. The section 4 presents a brief discussion about the experimental setup and schematic outputs. The conclusion of this research work is given in section 5.

II. LITERATURE SURVEY

Xing *et al.* [14] proposed a 7-bit MS/s four-way time interleaved SAR ADC. In this paper, a partial Vcm based switching technique was implemented that requires a digital overhead from the SAR controller and achieved better conversion accuracy. This methodology has reduced the common mode variation by 50%. Reduction of noise, comparator offset and input parasitic was analyzed and verified by simulation. In this research work, the prototype fabricated in the 65nm technology, which occupies 0.025 mm² of active area. But, the usage of the external common mode voltage during DAC reset could be a problem with this technique. Large switching power and more area is required to run the entire architecture.

Zhang *et al.* [15] presented a 14-bit kS/s SAR-ADC used for biomedical application. In order to achieve enhanced linearity, a uniform geometry non-binary weighted capacitive DAC was implemented. Furthermore, in this method, a secondary bit method was used in dynamically shift decision levels for error correction. This method was implemented in 65nm CMOS technology. The ADC has consumed 1.98 μ W Power and 0.28mm² of active area. This Architecture requires number of stages to implement that increases complexity of the ADC.

Mao W, Y *et al.* [16] implemented Non-Fractional Binary Weighted Capacitive Array with Attenuation (NFBWA) capacitor method for SAR ADC. The proposed DAC method has improved the Walden Figure-of-Merit performance by 1.67 and 5.45 times. This method minimized the area and power of the capacitive array compared to Binary Weighted Attenuation (BWA) technique. The operation of the NFBWA method requires more time, which is the main limitation of this method.

Shakibae *et al.* [17] proposed a power-efficient SAR ADC system.

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In this design a new low energy capacitor switch approach is used that consumed no switching energy in first three comparison steps. Furthermore, an energy efficient split monotonic method was used for the rest of the operation. In this design switching energy consumption is reduced by 99.23% and total capacitor size is reduced by 75%. The proposed scheme reduced the power consumption of the control logic circuit. The proposed architecture is not suitable for high-resolution ADC circuits.

III. PROPOSED METHODOLOGY

In this paper, SAR DAC-ADC circuit is designed which is shown in Figure 1. This architecture contains a DAC, comparator, SAR, and an Encoder. For high sampling linearity, bootstrapped switches are used. In this work, different values of the capacitor are used to design the DAC.

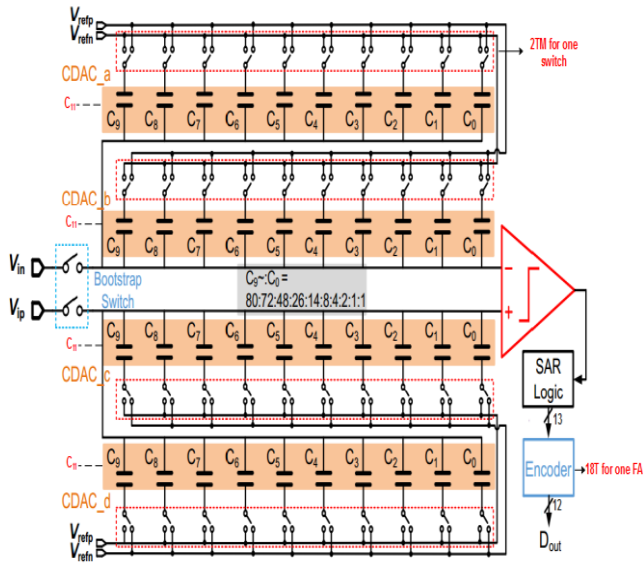


Figure 1. Overall architecture for SAR DAC- ADC circuit

In DAC design, $V_{refp}, V_{refn}, V_{in}, V_{ip}$ is connected as input terminal. V_{refp}, V_{refn} Input pulse is given as 0.9 v. V_{refp} Signal changes at positive edge of the clock and V_{refn} signal set as zero. V_{ip} and V_{in} signal is given as 0.6 v. V_{in} Signal is applied to inverting terminal and V_{ip} signal is applied to non-inverting terminal of the comparator. 12 capacitors are used to DAC, LSB capacitor value is 2.8 fF and rest of the capacitors are 10fF. V_{refp}, V_{refn} Signal is connected to the capacitor through the switch. This work used 2T MUX to design switch. One PMOS and one NMOS is used to design the single MUX. The design and operation is explained in next section.

A. Comparator

Low noise, low power with high speed comparator is an important factor to design the entire architecture. When clock clk is low, comparator will goes to reset mode and the outputs (Outp and Outn) are high. When clock clk is high, the outputs of the pre-amplifier is zero. If $V_{in} > V_{ip}$ "On" signal gives positive pulse. If $V_{in} < V_{ip}$ "Op" signal gets positive pulse. These two signals perform inverter operation and gives out_p and out_n. The signal Op and On connected to the SAR logic which is explained below section.

B. SAR Logic

Figure 2. Shows a chain of registers that are cascaded to implement the SAR. The dynamic register is needed to store the comparator outputs and to control the capacitive DAC, D-flip-flops are utilized to accomplish this objective, bringing the critical path delay to $2tdq$, tdq is the delay from the rising edge of the clock to the substantial output of a D Flip Flop.

In this Architecture, dynamic registers are used, which is activated by the comparator output. Figure 3. show the timing diagram of the dynamic register. CSN is the turnaround of the sampling signal, which is created through on-chip dividers and NAND gates. This signal is utilized for all registers to reset the outputs to their starting states. During the sampling stage, both b_i and b_i' are charged to V_{dd} . At the point when comparison finishes, the outcomes are caught and put away at b_i/b_i' . At the same time, b_{i+1}/b_{i+1}' is created to control the DAC switches. Whenever b_i/b_i' is released to low, C_i is released to turn off the current b_i register. After C_i and CK goes to low, C_{i+1} is activated to empower the following bit register. Note that Low-Threshold Voltage (LVT) gadgets are processed to further increase the speed.

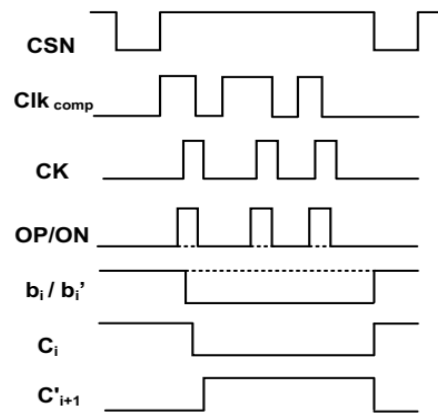


Figure 3. Timing diagram

All the outputs ($b_{i_a} / b_{i_b} / b_{i_c} / b_{i_d}$) are connected to the MUX for getting single output for each and every Control Unit (CU). These 13 CU outputs are given to the encoder as input which is explained in below section.

C. Encoder

This encoder design contains multiple Full Adder (FA) circuits. For designing single FA, 18T is required which is explained in resulting section. Table 1. presents output of the encoder based on SAR output. Output of SAR consists of 13 bit values which are delivered to the output. Based on Table.1, the SAR output is connected to the FA which delivered the encoder output. For example, B1 and B2 signals are needed to get the D2 output of the encoder. After designing the encoder, 12 bit are delivered to the output (D0 to D12). Finally, the performance parameters like area, power, delay is calculated which is explained in next section.

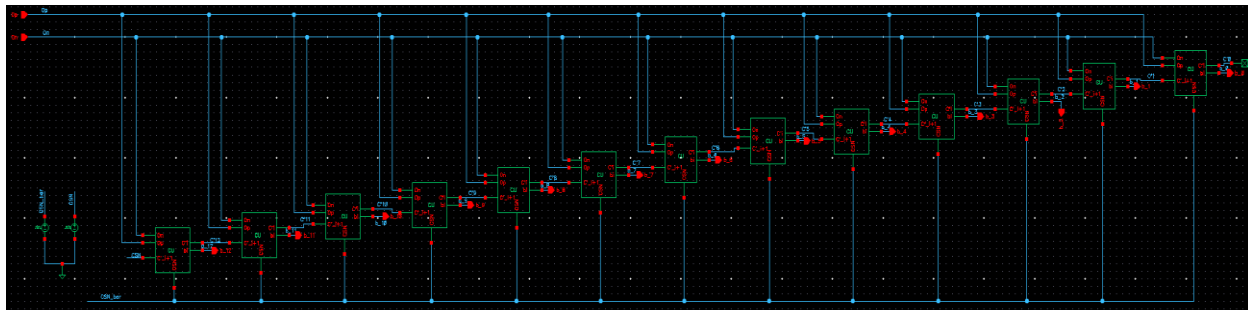


Figure 2. SAR logic diagram

Table 1. Encoder output based on SAR output

Weight	2048	1024	512	256	128	64	32	16	8	4	2	1
Binary code												
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12

IV. RESULT AND DISCUSSION

This proposed architecture was implemented in Cadence Virtuoso 45nm CMOS technology. Initially, each and every sub blocks are designed which helps to create the entire architecture cell view. For making cell view, initially the circuit design needs to be designed. Once it is finished, we have to choose “create→cell view→from cell view”.

This above step is used to convert schematic into the cell view block. Then, all the cell view is connected to make a main module block design. After the top module design, following performance has been evaluated.

A. Area

The entire area of the architecture is calculated with the help of the transistor. Single transistor width is 120nm and length is 45nm. Based on the number of transistors for every block, the area has been calculated. The number of transistor count for each and every block is shown in Table 2.

Table 2. Transistor Count for every module

Design	Transistor Count (TC)
DAC – Proposed	96
DAC- Existing	480
Comparator	19
Single CU	40
13 CU	520
11 CU	440
FA- Proposed	18
FA- Existing	36

B. Power and Current

After, running the simulation the power and current consumption of the entire architecture has been calculated. In Analog Design Environment (ADE) window, we have to calculate the power for the top module. For that have to select “Results→Print→transient operating point”. Then, we have

to click on the top module power supply, which shows the power and current value.

$$1 \text{ T Area (W * L)} = 120\text{n} * 45\text{n} = 5400\text{nm} = 5.4\mu\text{m}$$

10B-12TM-36TFA 12B-2TM-18TFA

Architecture		
Area (um ²)	6625.8	4206.6
Power (uW)	146.082	46.3671
Current (uA)	121.735	51.519
Delay (ns)	2.7029	0.9321
Technology	45nm	45nm
Bit	10	12

Table 3. Performance comparison of 10B-12TM-36TFA and 12B-2TM-18TFA method

The comparison of the 10B-12TM-36TFA and 12B-2TM-18TFA architecture is given in Table.3. In this Table, area, power, current, delay, technology, and bits are evaluated to check the performance of two different architectures. The performance has been improved in 12B-2TM-18TFA compared to 10B-12TM-36TFA. We have implemented these two architectures and the results are tabulated above.

Table 4. Power consumption for different methods

Design	R Hedayati. [18]	Akil et al. [19]	Naveen et al. [20]	J Zhong et al.[21]	R vitek et al.[22]	S Wong et al. [23]	J Tsai et al.[24]	C.H. Lee et al.[25]	10B-12TM-36TF A	12B-2TM-18TF A (Present Work)
Bit	10	9	10	12	10	10	10	10	10	12
Technology (nm)	65	180	180	65	65	65	28	90	45	45
Power (uW)	0.0124	130000	8290	6000	4300	2300	680	1970	146.08	46.367

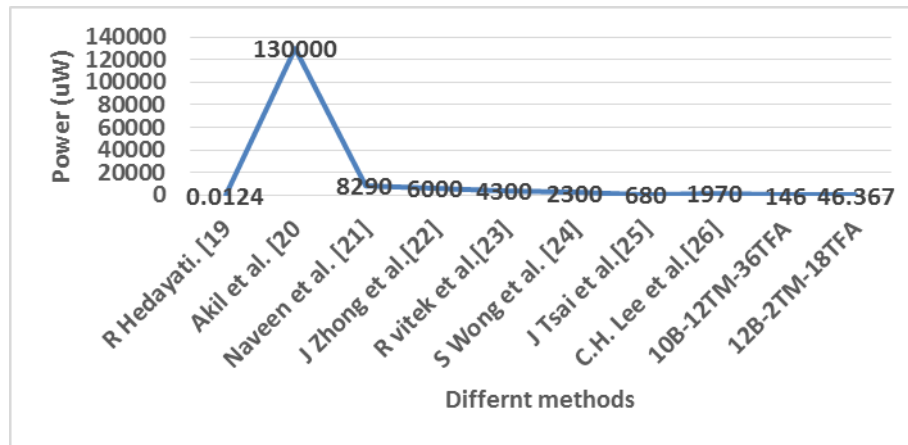


Figure 4. Power comparison for different methods

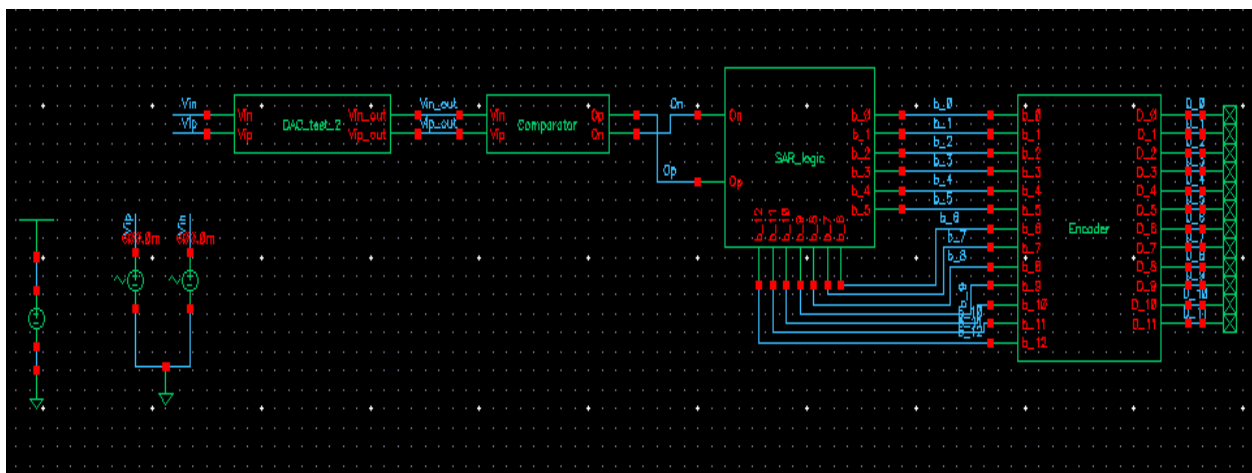


Figure 5. SAR – ADC Split Capacitor Architecture

The comparison of the power for different methods are given in Table. 4. The pictorial representation of the power consumption is shown in figure 4. Figure 5. shows the overall architecture it consists of DAC, comparator, SAR logic, and encoder. To design 12 bit DAC 48 MUX is required and each MUX needs 2 transistor, one PMOS and one NMOS is enough to design the MUX. The selection line signal is given to the gate terminal. If sel=0, PMOS will get turned ON and A is delivered to the output. If sel=1, NMOS will get turned ON and B is delivered to the output. In Existing design, i.e for 10 bit DAC 40 MUX and 12T is required to design the single MUX. In DAC, digital signal is converted into the analog signal which is given to the input of the comparator. The comparator operation, and schematic is described in the previous section. From the comparator, “Op” and “On” output has been taken which is

given to the SAR logic. The SAR logic explanation and internal block of CU also explained in the previous section. From the SAR logic, 13-bit is generated from b_0 to b_12. For 12-bit design, 13-bit has been generated as well as for 10-bit design 11-bit has been generated. These bits are given to the encoder model which is explained in the previous section.

The encoder design delivered 12-bit output. Figure 6. Shows the waveform of entire module. DAC output is represented as V_{in_out} and V_{ip_out} . These two analog signal is given to the comparator. If $V_{in_out} > V_{ip_out}$, “On” signal gives positive pulse. If $V_{in_out} < V_{ip_out}$, “Op” signal gets positive pulse. These two signals are given to the SAR logic which contains 13 CU. Each and every output of CU is represented as b_0 to b_12. There all the signals are connected to the encoder design. For 12-bit design, D_0 to D_11 signals as well as for 10-bit design, D_0 to D_9 signals are delivered to the output. output of CU is represented as b_0 to b_12. There all the signals are connected to the encoder design. For 12-bit design, D_0 to D_11 signals as well as for 10-bit design, D_0

to D_9 signals are delivered to the output. After finishing the simulation, the power, current has been calculated. The encoding output is 101010010100.

$$V_{out} = (\text{digital output value}/2^n) * V_{ref}$$

$$= (101010010100/2^{12}) * 0.9$$

$$V_{out} = 0.5950v$$

From this calculation, theoretical output value is similar to the input voltage. So, this entire architecture has been worked perfectly.

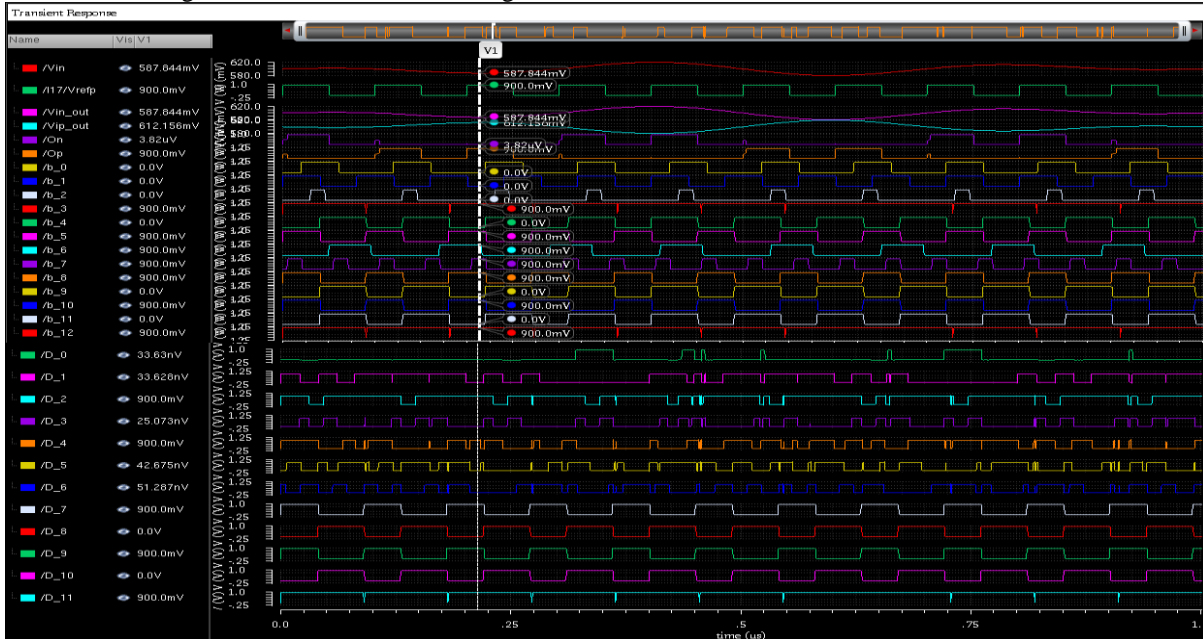


Figure.6. Output waveform

V. CONCLUSION

In this work, 12B-2TM-18TFA architecture as well as 10B-12TM-36TFA architecture have been implemented. Both the designs have been implemented in 45nm CMOS technology. The existing 10B-12TM-36TFA architecture require 12T and 36T to design the MUX and FA, on the other hand 12B-2TM-18TFA architecture require 2T and 18T to design the MUX and FA. The results have been evaluated from those two architectures. Through using 12-bit DAC in 12B-2TM-18TFA design, the area, power, current have been improved than 10-bit existing architecture. Internal schematics of each and every module has also been explained in respective sections. In 45nm, 12B-2TM-18TFA architecture consumed 4206.6 μm^2 area, 46.3671 μW power, 51.519 μA current and 0.9321 ns delay. In 12B-2TM-18TFA architecture, 36.51 % of area, 68.25% of power, 57.67 % of current and 65.51% of delay has been reduced when compared to 10B-12TM-36TFA. In future work, different library (PTM) and different technology (20nm) will be used to design different bit SAR-DAC architecture

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