Implementation of Phase Frequency Detector in Phase locked loop using Preset able modified TSPC D flip-flop

S.Praseetha,Benedict Tephila M ,Anusuya S

Abstract: ***Phase locked loop (PLL) forms an important part in many applications. Here design of PLL for frequency multiplier operation is considered. Frequency multiplier operation is implemented by using Preset able Modified Single Phase Clock (MTSPC) D flipflop logic circuits in Phase Frequency Detector (PFD). Preset able Modified Single Phase Clock (MTSPC) D flipflops functions at high speed with less power consumption. Noises in the form of glitches are introduced when a preset-able true single phase clocked D flipflop (TSPC) used in Phase Locked Loop. Preset-able modified TSPC (MTSPC) D flipflop used to overcome these glitches caused due to toggling at the output by use of PMOS. Technology applied is 90nm technology. Applications where better speed and reduced power consumption are required, this type of Phase locked loop (PLL) can be utilized.***

Index Terms: DFF, PFD, PLL, MTSPC D flipflop, TSPC D flip-flop.

I. INTRODUCTION

Phase Locked Loop has been an essential important block in wireless communication system. In order to have long battery life PLL must consume less power.PFD and VCO are two important blocks of PLL. A PFD compares input signal with that of VCO's output and produces a pulse. Output of PFD which is the phase difference between inputs used to control the VCO voltage. Flipflop forms basic component of PFD. Jitter introduced due to dead zone a phase error in PLL if static D flipflops used. Also operational speed is low. To overcome these difficulties a preset able TSPC D flipflops were introduced in PLL. Glitches were still introduced in intermediate nodes using TSPC D flipflops in PLL. Hence in this paper we implement PLL by using a preset able MTSPC D flipflop which suspends toggling. It also increases speed of operation and consumes less power. There by improving performance of the system.

The design of Phase Frequency Detector (PFD) using a MTSPC D flip-flop is considered and it is applied to the Phase Locked Loop (PLL) by 90nm technology. Reduced power consumption obtained as compared to the normal D-flipflop.

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II. PHASE LOCKED LOOP

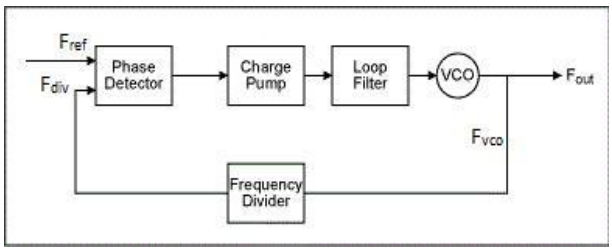

Fig.1. PLL

The PFD followed by Charge pump, Loop filter which is followed by VCO and Frequency Divider forms a PLL as shown. The PFD compares the frequency of reference signal and signal divided by frequency of VCO. The output which drives the charge pump is a pulse. This pulse is input signals phase difference. Charge pump's output is used to increase or decrease VCO control voltage or to keep it as such.

III. PHASE FREQUENCY DETECTOR

A. PFD using static D Flipflop

PFD forms an important block of PLL. It detects input signals difference in phase which is essential for many applications. Conventional PFD constructed using D flipflop has several disadvantages like high power consumption, dead zone, and low speed of operation and occupies larger area as number of transistors is more. Here inverters introduced as delay circuits to decrease the dead zone.

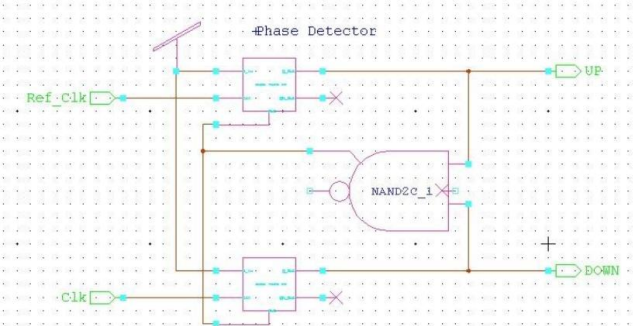

Fig.2. PFD

B. PFD using preset able TSPC D flipflop

Preset able TSPC D flipflops are constructed using less number of transistors and hence they occupy only smaller area.

To reduce the power consumption a simple modification done that reduces internal switching at some nodes of these flipflops. Only a single clock is applied for synchronization. This makes the circuit simple.

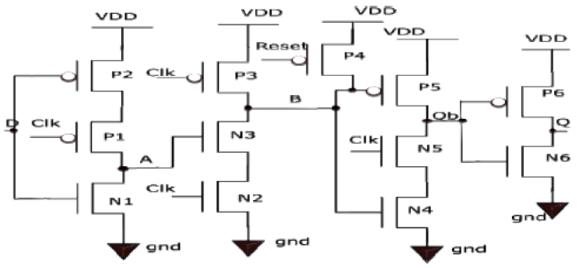

Fig.3 positive edge triggered TSPC D Flipflop

Preset able TSPC D flipflop circuit is basically constructed using Common Gate input NMOS and PMOS transistors. Propagation delay reduced by using such kind of transistors and thus phase error caused by dead zone is controlled. The input remains separated from output when low signal is available at the clock. Hence previous value is maintained at Qb when clock signal is low or high. Once clock signal makes transition from low to high the output will produce input's complement. The output maintains its high value until reset is low.

C. PFD using Preset able MTSPC D flipflop

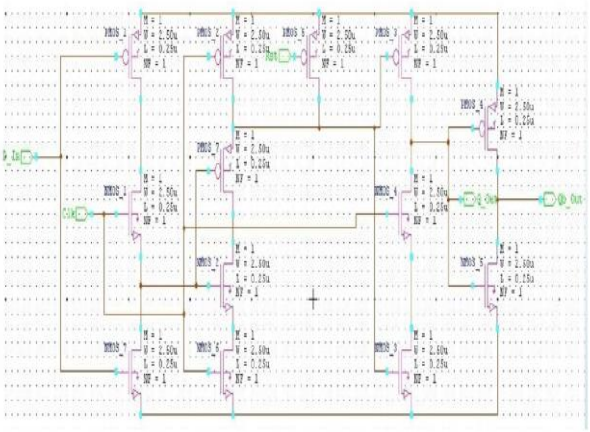

Fig.4 positive edge triggered MTSPC D Flipflop

In above TSPC D flipflop we observe that when clock signal is low, node B is pre-charged to high. When clock signal is high, node B is low. Hence when both input D and clock are low for a long time, continuous toggling occurs at node B. This causes noise to occur at output. For each time when clock goes from low to high glitches occurs which is a disadvantage in case of PLL where it goes into dead zone condition.

Previous values maintained if clock and input is low. Node b pre-charged to high when input goes high. Node b remains in high when clock goes low to high condition. Node b will become low when there is a low to high transition at clock and Qb will be high. Node Qb will be high when PMOS IS ON and preset is maintained low. Thus toggling is avoided here by addition of a PMOS. By using this MTSPC D flipflop in PLL dead zone condition can be avoided and this reduces erroneous conditions of PLL used for many applications.

IV. CHARGE PUMP

Charge pump controls the VCO voltage according to up or down signals received from PFD. NMOS and PMOS diode connected load constructs a Charge Pump. Input is up or

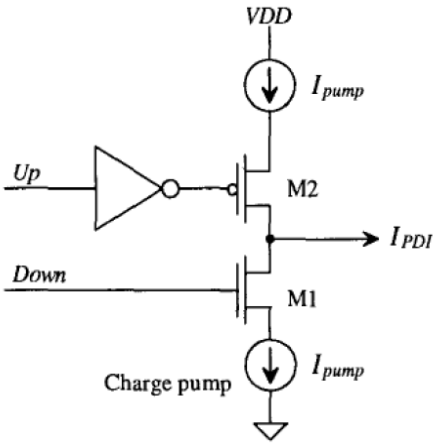

Fig.5 Charge Pump

down signal from PFD. When reference signal is high compared to feedback signal from VCO, PFD produces an up signal. This in-turn will switch on the PMOS in charge pump, charge pump then infuse current into loop filter. The output voltage is increased. When reference signal is low compared to feedback signal from VCO, PFD produces a down signal. This down signal when given as input to charge pump, switches NMOS to on condition and will make the current drop out of loop filter. The output voltage will be decreased. Equal currents have flow in both NMOS and PMOS to avoid any mismatch in current.

V. VCO AND LOOP FILTER

A voltage controlled oscillator produces an output signal in proportion to input DC voltage. The input voltage is directly related with output frequency. Frequency from few Hz to hundreds of GHz can be varied. The loop filter smoothens and integrates the error signal to produce a DC voltage to tune the VCO in the direction to eliminate the error in phase and frequency.

VI. SIMULATION RESULTS

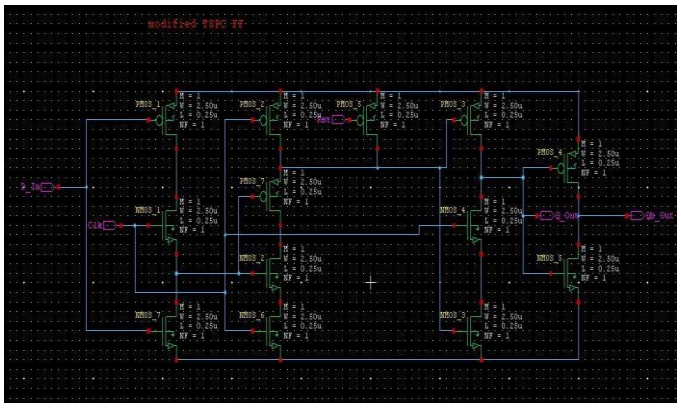

Fig.6 MTSPC D Flipflop

MTSC D flipflop constructed by adding an extra PMOS transistor using cadence virtuoso 90nm technology as shown above, inorder to remove the toggling condition. Toggle mode operation of MTSPC D flipflop is shown. The clock frequency of 4GHz is applied at a 10ns simulation time.

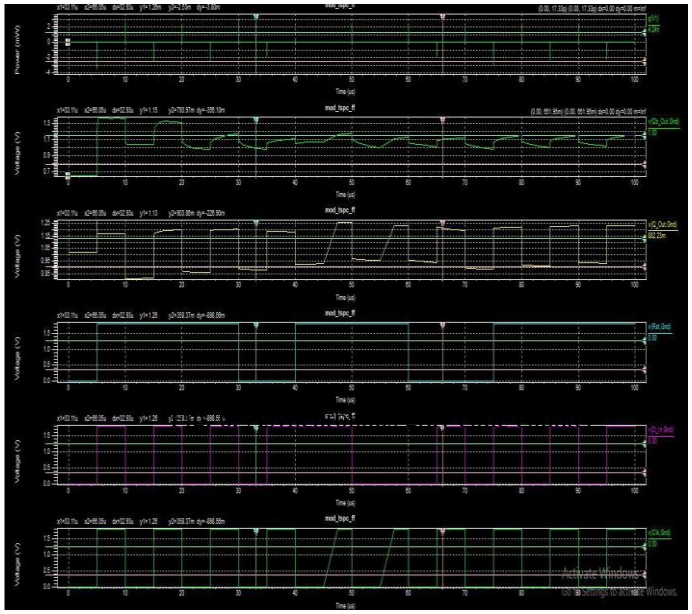

Fig.7 Output diagram of MTSPC D Flipflop

Table I. Comparison of TSPC DFF and MTSPC DFF parameters

Performance parameters	TSPC DFF	MTSPC DFF
Input clock frequency	1 GHz	1 GHz
Clock-to-Q delay (Low-to-High)	92.95 ps	61.08 ps
Clock-to-Q delay (High-to Low)	143.6 ps	122.9 ps
Average Clock-to-Q delay	118.27 ps	91.99 ps
Setup time(t_{setup})	70.13 ps	64.14 ps
Hold time(t_{hold})	≈ 0	≈ 0
Average power consumption	75.43 µW	21.83 µW

The Performance of both TSPC D flipflop and MTSPC D flipflop are compared for same clock frequency of 1 GHz. MTSC D flipflop shows good performance than TSPC D flipflop in terms of low delay and less power consumption.

VII. CONCLUSION

An efficient design of MTSPC D flipflop PFD for PLL is presented. A clocked dynamic logic is used. A single clock frequency of 1GHz was used. In conventional PLL circuit D flipflops are utilized in PFD block. This introduces glitches which is a main cause for phase errors. Hence to avoid those drawbacks a preset able MTSPC flipflops were presented in this paper. Compared to conventional TSPC flipflops these flipflops has reduced noise at the output. Power consumed by circuit constructed was less. By addition of PMOS toggling at intermediate nodes are avoided.

As MTSPC flipflop has advantages like high speed operation, low noise and less power consumption, it can be implemented in many electronic circuits where all these parameters are necessary. PLL designed using this MTSPC flipflop can be used in clock generation, frequency syntheziser and clock recovery circuits in serial data links. Thus not only for PLL other circuits where D flipflops are utilized, it can be replaced by such MTSPC flipflop to get enhanced performance.

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