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Design SSTL Based Energy Efficient Solar Charge Sensor on FPGA

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Abstract*: In this paper we have designed solar charge sensor which is used to make our battery efficient. Component is designed on Virtex 6 FPGA family and applied frequency scaling techniques. During the experiment, we have used different SSTL IO families and calculated total power consumption. In our work we have selected class I and class II from SSTL IO family. For the analysis we have used following range of frequency (20GHz, 40GHz, 60GHz and 80GHz). Firstly, we have worked with SSTL2_I and reduced total power consumption by 51.53%, in second experiment we have worked with SSTL2_I_DCI and reduced consumption of power by 47.18%. In third experiment we choose to work with SSTL2_II and reduced 51.58% in total power consumption. In fourth experiment we opted SSTL15 Io standard and downscale the total power consumption by 51.57%. In fifth we have selected SSTL15_DCI and downscale the power consumption by 49.93%. In sixth experiment we set SSTL18_I_DCI IO standard and consumption minimize by 49.20% in total power. At the end we have mark to be worked with SSTL18_II_DCI which is DCI circuit and found 48.78% reduction in total power consumption.

***Keywords*: SSTL IO standard, Low Power, Energy Efficient, 28 nm FPGA**

I. INTRODUCTION

A.Solar Charge Sensor

In our work, we are going to design efficient solar charge sensor which makes our battery efficient. As in twentieth century we are talking a lot about the energy conservation concept and we believe that solar energy is best source of energy conservation. Number of cells are built in solar charger for storing energy. This energy can use for number of things like mobile charging and running other electronics appliances.

Sensors of the Solar Charger sense the battery's voltage level and it notify to the user that now this is the time to charge the battery or the battery is sufficient to charge. When the sensor indicates that the battery is sufficiently charged, the charging of the battery will automatically stop. So there is no need of excessive charging.

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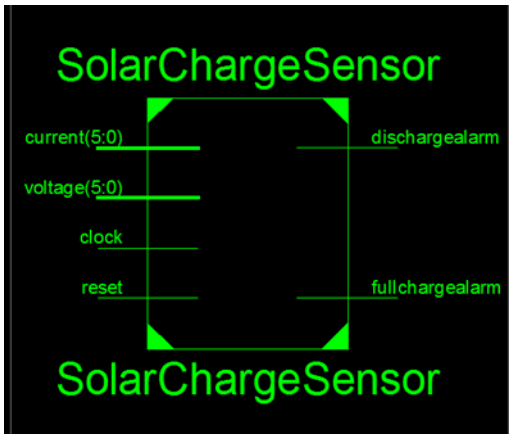

Fig.1 Top Level of Schematic of Solar Charge Sensor

In Fig.1, we have shown Top Level of Schematic of Solar Charge Sensor. This design allow to having the virtual visualization of our FPGA component.

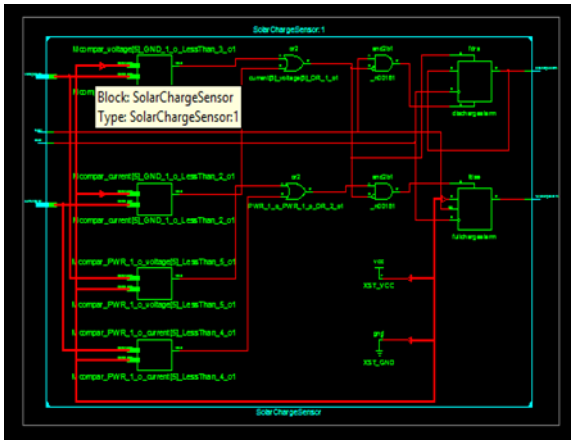

Fig.2 RTL Schematic of Solar Charge Sensor

In our Fig.2, we have shown the RTL Schematic of Solar Charge Sensor and Behavioral Model of Solar Charge Sensor shown in Fig.3.

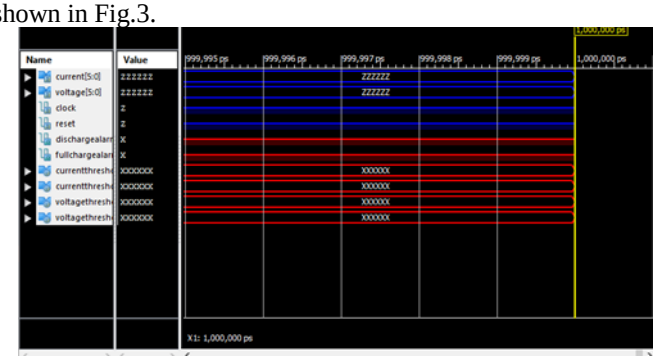

Fig.3 Behavioral Model of Solar Charge Sensor

B. SSTL (Stub-Series Terminated Logic)

SSTL stands for Stub- Series Terminated Logic. In SSTL we have two standards SSTL2 for 2.5 volt and SSTL18 for 1.8 Volt defined by JEDEC. We have two classes in SSTL2 standard Class I and Class II. In class I we have unidirectional signaling and in class II we have bidirectional signaling.

C. FPGA

Field Programming Gate Array which is also known as FPGA can be modified after the manufacture or we can say that it can be reprogrammed. To program the FPGA we used HDL languages. We have two types of HDL languages first is VHDL and second is Verilog. To create our component Solar Charge Sensor we have taken VHDL language. During design in FPGA we need to create bit file. Once we have bit file then it actually work in our virtual environment. For creating virtual environment we have used Xilinx Tool. After designing tool through FPGA we can apply number techniques on component like Voltage, frequency, Capacitance Scaling etc. In fig. 4 we have shown the design implementation of FPGA.

II. METHODOLOGY

In fig 5, we have shown our working methodology for designing stack. In first stage we design the specification of stack and in second stage, we generate RTL coding for stack. In third stage, we have applied our voltage scaling techniques on RTL coding. In fourth stage, we have done simulation and verification for our design. Later in fifth stage, we have done logic synthesis and after that in sixth stage, we designed physical layout for stack and configure it with FPGA Virtex 6 family.

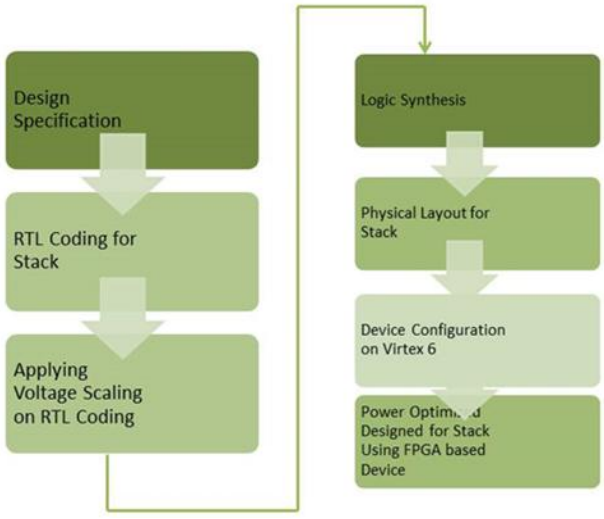

Fig.5 working methodology for designing Solar Charge Sensor

III. RESULT AND DISCUSSION

In our work we have designed Solar charge sensor on Virtex 6 FPGA family and calculate total power consumption on SSTL IO family. We have taken four different SSTL families like SSTL2_I, SSTL2_I_DCI, SSTL15 and SSTL18_II_DCI.

TABLE. 1. Experiment with SSTL2_I

	Total Clock Power	Total Logic Power	Total Signals Power	Total IOs Power	Total Leakage Power	Total Power
20GHz	0.631	0.002	0.023	0.392	1.316	2.364
40GHZ	1.262	0.003	0.046	0.555	1.336	3.202
60GHz	1.893	0.003	0.069	0.719	1.335	4.040
80GHz	2.524	0.004	0.092	0.883	1.376	4.878

In TABLE. 1, we have scaled down our frequency form 20GHz to 80 GHz and we found that there is 55.60% reduction in IO power, 4.36% reduction in leakage power and in last we found 51.53% reduction in total power consumption. Analysis also shown by fig. 6 by Graph.

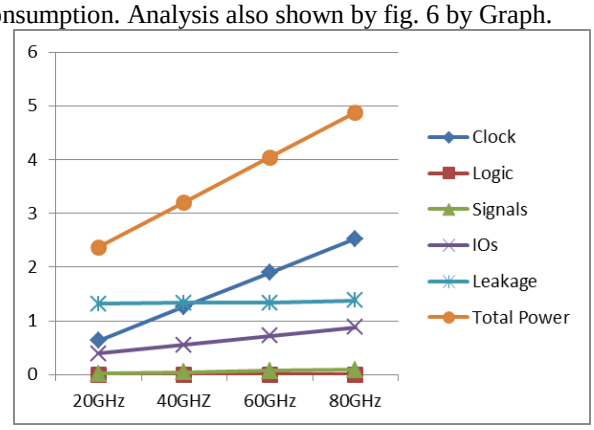

Fig. 6. Power Analysis at SSTL2_I

TABLE. 2. Experiment with SSTL2_I_DCI

	Total Clock Power	Total Logic Power	Total Signals Power	Total IOs Power	Total Leakage Power	Total Power
20GHz	0.631	0.002	0.023	0.828	1.327	2.811
40GHZ	1.262	0.003	0.046	0.991	1.346	3.648
60GHz	1.893	0.003	0.069	1.153	1.366	4.485
80GHz	2.524	0.004	0.092	1.316	1.387	5.322

In TABLE. 2, experiment done with SSTL2_I_DCI and change the frequency from 20GHz to 80 GHz. During the work we have minimize the power consumption by 47.18%. Same data we have shown through graph as shown in Fig.7.

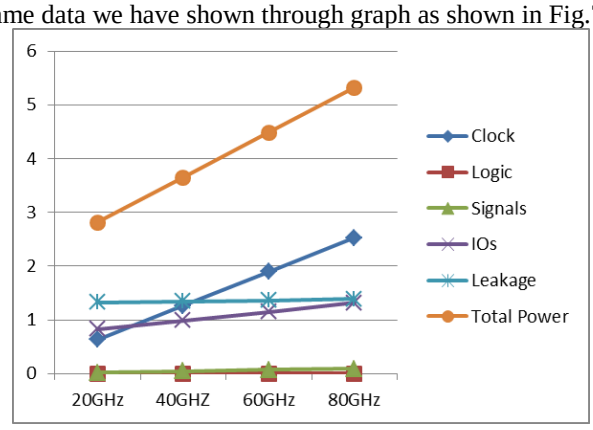

Fig. 7.Power Analysis at SSTL2_I_DCI

TABLE. 3. Working with SSTL2_II

	Total Clock Power	Total Logic Power	Total Signals Power	Total IOs Power	Total Leakage Power	Total Power
20GHz	0.631	0.002	0.023	0.400	1.317	2.373
40GHZ	1.262	0.003	0.046	0.568	1.336	3.215
60GHz	1.893	0.003	0.069	0.736	1.356	4.057
80GHz	2.524	0.004	0.092	0.904	1.376	4.900

In TABLE. 3, we have worked with SSTL2_II which is DCI circuit. During our analysis we have found that when we change the frequency from 20GHz to 80 GHz then total power is reduced 51.58%. Fig. 8 shown the same analysis by the graph.

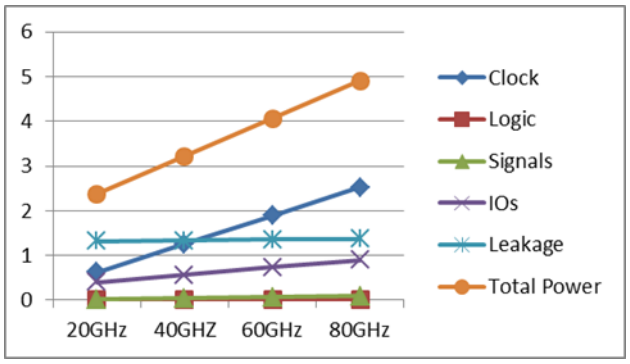

Fig. 8. Power Analysis at SSTL2_II

TABLE. 4. Working with SSTL15

	Total Clock Power	Total Logic Power	Total Signals Power	Total IOs Power	Total Leakage Power	Total Power
20GHz	0.631	0.002	0.023	0.384	1.315	2.355
40GHZ	1.262	0.003	0.046	0.545	1.334	3.191
60GHz	1.893	0.003	0.069	0.707	1.354	4.027
80GHz	2.524	0.004	0.092	0.869	1.374	4.863

In TABLE. 4, we have worked with SSTL15 which comes under class II standard. Here we have reduced the power consumption by 51.57% when we changed the frequency from 20 GHz to 80 GHz. Same data we have analyzed through graph in Fig. 9.

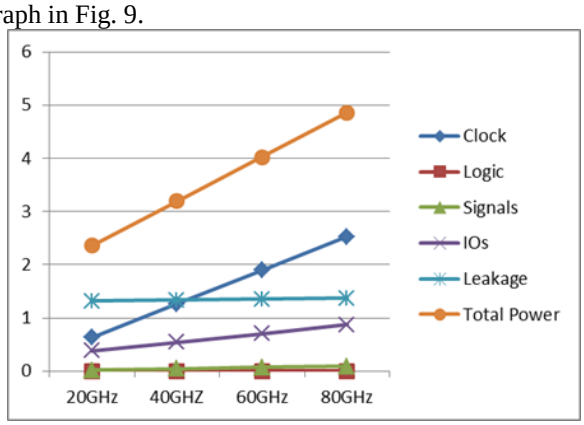

Fig. 9. Power Analysis at SSTL15

TABLE.5.Working with SSTL18_II_DCI

	Total Clock Power	Total Logic Power	Total Signals Power	Total IOs Power	Total Leakage Power	Total Power
20GHz	0.631	0.002	0.023	0.657	1.322	2.636
40GHZ	1.262	0.003	0.046	0.820	1.341	3.472
60GHz	1.893	0.003	0.069	0.983	1.361	4.309
80GHz	2.524	0.004	0.092	1.145	1.382	5.147

Now we have used SSTL18_II_DCI in TABLE. 5. Here when we altered the frequency form 20GHz to 80 GHz then reduced the total power consumption by 48.78%. Fig. 10 shows the same analysis by the below graph.

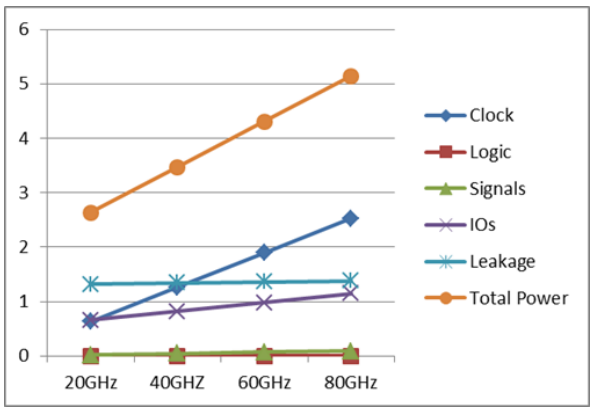

Fig. 10. Power Analysis at SSTL18_II_DCI

TABLE. 6 .Working with SSTL18_I_DCI

	Total Clock Power	Total Logic Power	Total Signals Power	Total IOs Power	Total Leakage Power	Total Power
20GHz	0.631	0.002	0.023	0.621	1.321	2.589
40GHZ	1.262	0.003	0.046	0.773	1.340	3.424
60GHz	1.893	0.003	0.069	0.935	1.360	4.260
80GHz	2.524	0.004	0.092	1.096	1.380	5.097

SSTL18_I_DCI is used for the experiment in TABLE. 6 which is DCI circuit. In our work we have altered the frequency form 20GHz to 80 GHz and found that there is 43.33% reduction in IO power, 4.27% reduction in leakage power and total power is reduced by 49.20%. Fig. 11 shows the graph analysis for the same.

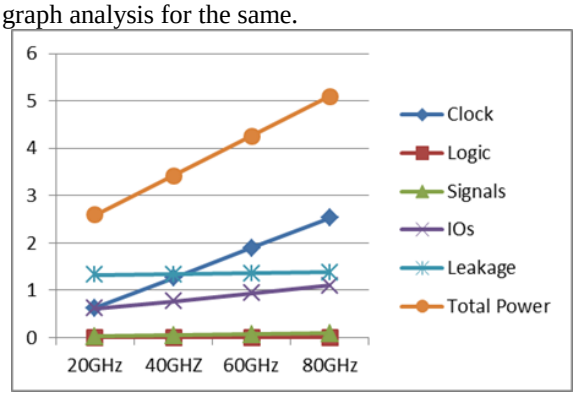

Fig. 11.Power Analysis at SSTL18_I_DCI

TABLE.7. Working with SSTL15_DCI

	Total Clock Power	Total Logic Power	Total Signals Power	Total IOs Power	Total Leakage Power	Total Power
20GHz	0.631	0.002	0.023	0.541	1.319	2.516
40GHZ	1.262	0.003	0.046	0.703	1.338	3.352
60GHz	1.893	0.003	0.069	0.865	1.358	4.188
80GHz	2.524	0.004	0.092	1.027	1.378	5.025

Here for the experiment we have used SSTL15_DCI in TABLE. 7, which is DCI circuit. In our work when we have altered the frequency form 20GHz to 80 GHz and found that there is 47.32% reduction in IO power, 4.28% reduction in leakage power and total power is reduced by 49.93% Same analysis we have discussed by graph as shown in Fig. 12.

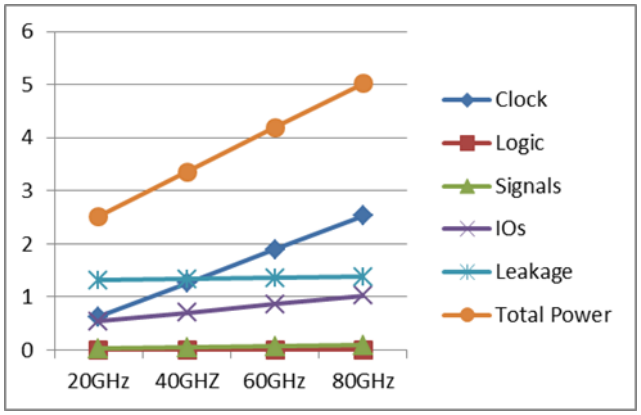

Fig. 12.Power Analysis at SSTL15_DCI

IV. CONCLUSION

We have analyzed our result on the basis of percentage reduction in IO power, Leakage power and Total Power consumption. We worked with SSTL2_I, SSTL2_I_DCI,SSTL2_II,SSTL15, SSTL18_II_DCI ,SSTL18_I_DCI IO,SSTL15_DCI family by scaling down our frequency form 20GHz to 80 GHz and found 51.53%, 47.18%, 51.58%,51.57%,48.78%,49.20%, 49.93% reduction in total power consumption respectively. From these results, we found that SSTL2_IIis better IO resources among these families. We have also observed that reduction in Clock, Logic and Signal power consumption remain same for all SSTL families.

V. FUTURE WORK

Here we have used Virtex-6 FPGA family for the implementation of our design, but we can redesign our Solar Charge Sensor with different FPGA family like Virtex 7, Virtex 6, Virtex 5 or we can also apply different- different techniques for calculating total power consumption and try to minimize the power consumption.

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