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Leakage Current Analysis of 6T & 7T-SRAM using FINFETs at 22nm Technology

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Abstract: ***Persistent scaling of planar MOSFET results in increase in transistor package density and performance of chip. However at nanometer regime , it has become a very challenging issue due to the increase in the short channel effects. In nano-scaled MOSFETs, the channel loses control from gate terminal due to potential at drain. Due to this, it is difficult to turn off MOSFET completely which inturn leads to leakage currents. Since cache memory occupies more area of processors, it is difficult to reduce leakage power in microprocessors. Double gate transistors have become replacement for MOS transistors at nano level. Since FINFETs have double gates, the leakage currents can be controlled effectively than planar MOSFET. In this paper, leakage currents of 6T & 7T-SRAM memory cell are analyzed using FINFETs at 22nm technology in hspice software***

Keywords: CMOS, FINFET, SCE, SRAM.

I. INTRODUCTION

The major concern in battery-operated portable devices is increase in power consumption due to increase in transistor package density and operating frequency at nano scale. The power consumption in non-portable electronic systems is also significant due to problems existing in packaging and also cost for cooling the systems. Thus, the main design concern in semiconductor industry is to obtain performance requirements with low power consumption.

The unceasing scaling of MOS transistors with every new process technology has provided enhanced system performance for years.

However, continuous miniaturizing of MOS transistor is not a good choice above 22nm technology due to limitations in fabrication [1].

The significant design difficulties at nano regime are: (a) Reduction of short channel effects and (b) minimization of device to device inconsistency to increase yield. Double gate transistors have evolved as an alternative to solve the problems posed due to continuous miniaturization[2]. The steps involved in FINFET fabrication are similar to that of planar MOS transistors. This enables manufacturing industry to fabricate rapidly.

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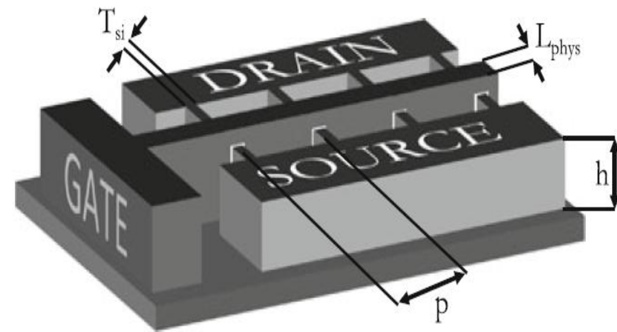

Fig 1.Multi-fin FINFET

Fig.1 illustrate the construction of a multiple-fin DG-FET. The FinFET transistor comprises of a tinny silicon body having thickness T_{Si}. It is surrounded by a gate electrode. Here, the ON current in FINFET flows parallel to the wafer plane. And the channel is formed vertical to the plane. Due to this structure, FINFET is named as quasi-planar device. The front and back doors of the DG-FET are frequently controlled severally by drawing endlessly the entryway conductor at the most elevated of the channel. The effective gate width of DG-transistor is $2nh$, where n is the number of fins and h height of fin. Transistor with high ON current can be obtained by using more number of fins. The pitch 'p' of the fin is made as small as half of the lithography pitch using lithography techniques [3].

II. THREE MODES OF FINFET

A. Shorted Gate:

In this mode, the 2 gates of FINFET are connected along resulting in a three-terminal device [4]. This acts as direct standby for typical CMOS devices.

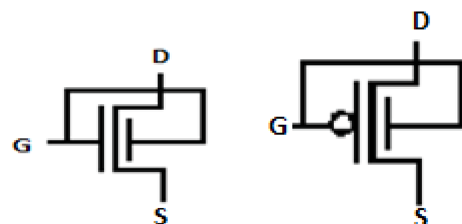

Fig.2 N & P-Type Shorted Gate DG-FET

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B. Independent Gate:

Here, the upper part of the gate is carved out to provide two separate gates [5]. Since, the two gates can be controlled independently; IG-FINFET offers more design possibilities.

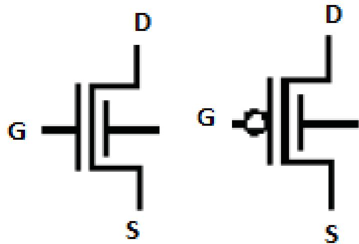

Fig.3 N & P-Type IG DG-FET

C. Low Power:

In this mode, the threshold voltage of FINFET transistor can be altered by employing a low voltage to n-type FinFET and high voltage to p-type FinFET. This reduces the static power consumption with delay increment [1]. The hybrid IG/LP-DGFET combines both LP and IG modes.

DG-FETs have the following advantages over planar MOS transistors [6]:

1) Reduced leakage currents
2) Admirable sub-threshold slope
3) Applicable for Radio frequency applications
4) High performance.
5) Lower power consumption
6) Exceptional electrostatic control over the channel

III. FINFET BASED SRAM

Static Random Access Memory is a volatile memory which holds information as far as power supply is provided. It offers quick access to information and is extremely consistent Static RAM clusters are customarily utilized as reserve memory in high-end processor chips and in Application-Specific Integrated Circuits (ASICs). These occupy an outsized portion of the die space. Giant arrays of quick Static RAM facilitate improve the performance of the system [7].

The basic 6T-Static RAM memory cell is shown in Fig.4. Typical 6T static RAM memory consists of two CMOS inverters connected back to back and 2 NMOS transistors called access transistors that act as gates to access information in memory cell. These back connected inverters form a latch and work as storage element. The word line exerts pass transistors to store information into cell. The drain terminals of pass transistors are connected to memory cell and source terminals are coupled to BL &
BLB. The access transistors are deactivated once the word line is made low. At this moment, scan or write operations can't be performed. At this state, memory cell will hold data bits, because the line voltages stay at V_{dd} and gnd. Once the word line is set to high, the pass transistors are activated and write operations is performed.

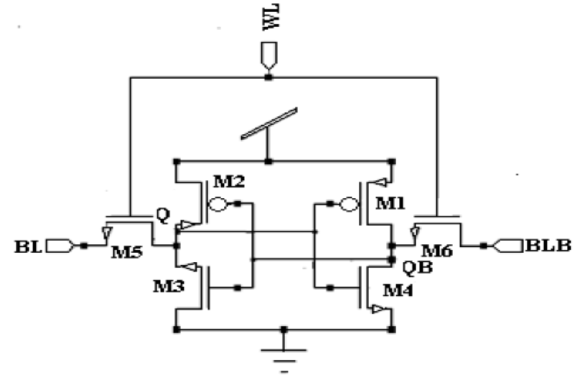

Fig. 4 Conventional 6T-SRAM Memory

CMOS Scaling technology helps tons in coming up with the economical SRAMs however, thinning out on the far side 32nm, such a lot of limitations found in CMOS like sub threshold currents, gate tunneling currents becomes additional sensitive to short channel effects & variations in threshold voltage. In high-end processor chips, high performance digital systems, bio-medical instruments, medical specialty implants all needs economical SRAM having less power consumption and high performance. It becomes essential to design economical low power Static RAMs with acceptable stability and small size, since these occupy more area in processor chip.

To reduce the Short Channel Effects, multi-gate transistors are evolved [8, 9]. The processing steps for FINFET fabrication are similar to that of conventional MOS transistors. Since this structure has full control over the channel, it offers reduced SCEs. FINFET SRAM provides higher results than panar bulk CMOS SRAM.

IV. SIMULATION RESULTS

Here, 6T&7T FinFET Static RAM cell is designed in shorted-gate mode and simulated using Hspice at 22nm technology

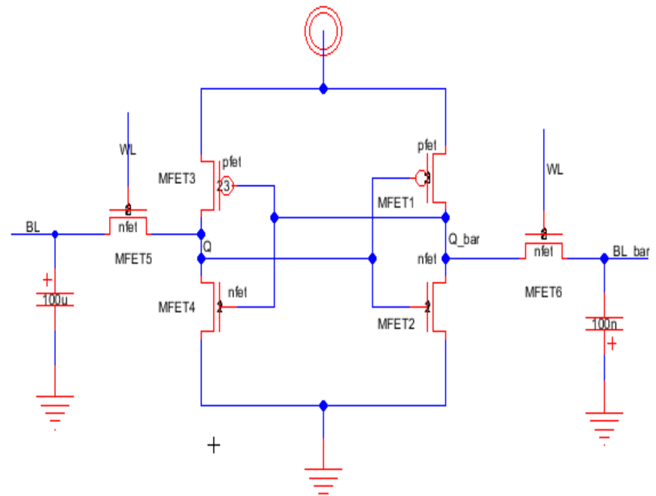

Fig. 5. Schematic of 6T-SRAM Memory

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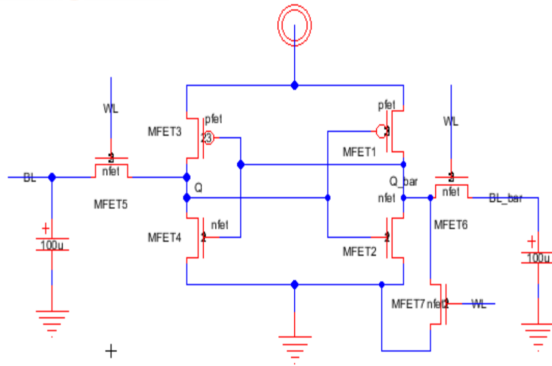

Fig. 6. Schematic of 7T-SRAM Memory

Fig. 7. 6T- Read output waveform

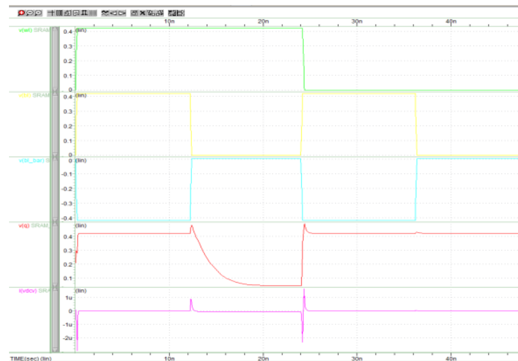

Fig. .8. 7T- Read output waveform

Table I: Leakage Power of 6T&7T SRAM using FINFET

Design	*Area (um^2)*	*Total Power(w)*	*Leakage power(w)*	*Leakage current(A)*	*Delay*
7T-SRAM – Read	2.1	1.26u	0.126u	0.0378u	400ps
7T-SRAM – write		0.042u			
6T-SRAM – Read	1.8	1.68u	0.0168u	0.0357u	300ps
6T-SRAM – write		0.033u			
1 bit 7T-SRAM cell	6	33.6u	2.1u	28.56u	0.4ns
1 bit 6T-SRAM cell	5.7	29.4u	1.68u	26.88u	0.2ns

V.CONCLUSION

In CMOS circuits, flow of static currents at nano scale has become a significant contributor to overall power consumption due to short channel effects. FinFET based SRAMs can be used as a substitute to the conventional CMOS devices. FinFET are suitable for nano-scale memory circuits because of minimized Short Channel Effects (SCE). In this paper, 6T &7T- SRAM is designed using FINFET at 22nm technology. The simulation show that FINFET designs offer low power consumption and high performance at nano-regime beyond 45nm.

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