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Beamforming Algorithm Architectures for Medical Ultrasound

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***Abstract*— Medical ultrasound scanners are amongst the most sophisticated signal processing machines in use today. The Beamformer is the brain of whole signal processing system of the scanner [1]. Beamforming allows message transmission or reception to be directed or spatially selective. It is used in receiving beamforming to concentrate the noise signals obtained in the region of concern as reflections from various tissue structures. This paper reviews the various receive beamformer architectures implemented in FPGA/ASIC for ultrasound imaging.**

Most of the receive beamformers are implemented using the standard technique Delay and Sum. Beamforming in ultrasound instruments for medical imaging has traditionally been implemented using analog delay lines. The concept of dynamic focusing in near field has resulted more complex analog delay structures and were replaced by digital structures. By the availability of high-speed analog to digital converters, and VLSI Technology improvements have now made real time implementation of digital beamformers feasible. The current innovations involve hybrid beamformers utilizing the pros of both analog and digital structures. This paper discusses the evolution of beamforming architectures from analog to digital environment and the current beamformer designs. The changes in beamformer designs in order to be compatible to high frequency probes and yield improved imaging performance, resource optimization, etc. are discussed.

Keywords—Medical Ultrasound, Beamforming, Signal Processing, ADC, Imaging, DAS, Adaptive Beamforming.

I. INTRODUCTION

The application of ultrasound to medical diagnosis has seen continuous development and growth over several decades. Medical ultrasound (also referred to as diagnostic sonography or ultrasonography) is an ultrasound-based safe and effective testing method. Beamformer is the brain of the ultrasound scanner which is used for the directional transmission and reception of the signal. Beamforming is the process of using multiple sound waves to steer and focus a beam of sound. The Transmit beam former generates sound waves focused along desired scan lines. Once the received signals reach the Rx beam former, the signals are scaled and appropriately delayed to permit a coherent summation of the signals.

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Contributions from all elements must arrive simultaneously at the signal summer in an attempt to obtain a big echo message from a location at a necessary receive focus. This is accomplished through higher electronic delays for components nearer to the group centre.

This new signal represents the beam formed signal for one or more focal points along a particular specific scan line. Earlier, array systems involve simple implementation of beamformer functions without focusing.

Later, beamformer design was modified by including focusing. Several limitations were there such as limited focal region and high side lobe levels. These issues were solved by using high f-number and apodization. It dramatically improved the performance. But high value of f-number results in some drawbacks. So dynamic focusing was introduced to reduce f-number during receive beamforming and to keep it as a constant until it runs out of aperture. Implementation of dynamic focusing in analog beam- former needs use of coarse and fine delay. The cost variations associated with these systems led to the digital beamformer design. At the beginning the digital beamformers did not have much significant impact as it requires A/D converters with very large number of bits and a very high sampling rate. As time progresses there is a dramatic increases in gate counts of ASIC's and drastic improvements in the Tools for ASIC Development which also facilitated the digital beamformer designs. With the advancement in technologies there has been a tremendous change in the beamformer design and architecture. This paper discusses about various beamformer designs and architectures.

II. BEAMFORMING ALGORITHMS

A. METHOD AND APPARATUS FOR MULTI-BEAM BEAMFORMER BASED ON REAL-TIME CALCULATION OF TIME DELAY AND PIPELINE DESIGN

To realize the time delays of signal in receive channels earlier digital beamformers mainly uses the delay parameters that are calculated and stored in advance. Even though the method is simple in structure, it is required to add a relatively large RAM externally on the FPGA. It is a suitable solution for a single-beam system. However, it requires too much time for updating the RAM content due to the large capacity of the external RAM for a multi-beam system, so that it is not suitable for the multi-beam system. Therefore, in the multi- beam system, real-time calculation of the delay parameters is widely used. In this paper, the time delay of every channel required for the beamforming is calculated in real time by means of pipeline design[2], and the focusing parameters needed to be stored are only the parameters related to the probe and the direction of scan line.

The architecture of a delay circuit of one channel is depicted in the figure 1. Under the control of write control unit, the write address counter generates a linear write address for the i^{th} channel echo signal after passing through the analog frontend and the ADC conversion. The echo signal i is continuously written into the dual port RAM. An initial count value is set into the read address counter at the beginning, which we call coarse delay. The coarse delay represents the offset of the first read echo signal data with respect to the write address, and is also the integer portion of the i^{th} channel delay amount that is represented by sampling clock cycle. The fraction portion of the delay amount of the i^{th} echo signal is also called as fine delay, that is, the portion smaller than a sampling clock cycle is done by the interpolation circuit. It uses the read data corresponding to the integer portion and the next data to obtain the intermediate data of them by means of interpolation. The interpolation coefficient is given by the read controller. Every time that the accumulated fine delay reaches a whole delay unit, the read address counter will stop counting once, which we call stalling. The stalling is controlled by the read controller according to the delay parameters generated by the delay parameter generator. Because the delay should be adjusted dynamically, the delay parameter generator should obtain the data from the data bus dynamically, and distribute the delay parameter of each channel to the read controller and the write controller in each channel. The echo signals after delay control are sent to the summing unit for the final beam-forming. The summing unit is a multi-channel signal adder. The real-time calculation of the delay parameters require more hardware, especially for the probe in different shape, the design solution will become very complicated.

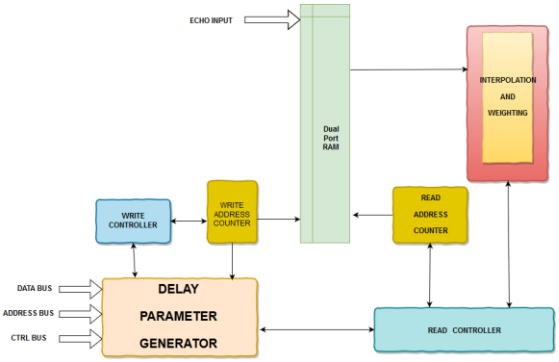

Fig. 1. Delay Line Circuit

B. AN OPTIMIZED ULTRASOUND DIGITAL BEAMFORMER WITH DYNAMIC FOCUSING IMPLEMENTED ON FPGA

To improve resolution of ultrasound scanners we require very accurate values of delays which will result in a superior Ultrasound image. The limitations of standard Analog to Digital Converters (ADCs) is putting across us the problem of time difference between two samples. We need to investigate two methods to improve ADC for its problem which is defined as time delay accuracy. First method is using phase rotations, otherwise called as direct sampled in-phase/quadrature (DSIQ) technique for beamforming. The problem of the above methods is that its results in a low quality image for a narrow band input. Second method of improving the time delay is the use of an interpolation filter. The fundamental requirement of an interpolation-based filter is that it requires up-sampling before performing a low-pass filter operation, which demands a high operating frequency in the Digital Signal Processing Section. We cannot use this model or method as we are suggesting a low cost FPGA solution which is not possible as resource utilization for the above method will explode to higher levels. Here we suggest a more efficient method which uses a poly phase filter to achieve the low cost FPGA model[3]. When we think about hardware the implementation of delay units is less complex when compared to the conventional method wherein which the delay for dynamic focusing, is calculated continuously. Considering the memory-utilization and memory limitations we have, we can only use pseudo-dynamic focusing methods in our related works. In this architecture we process only delay information which is updated for some pre-determined depths of investigations.

In this paper we discuss about a dynamic digital beamformer for an ultrasound system which is resource-optimized, based on a FPGA[3]. A 64-channel receive beamformer is implemented on the FPGA (Altera Arria V Family). A novel method to achieve resource optimization and to improve spatial and contrast resolution, here we used a full dynamic beamforming. The above mentioned architecture is implemented by summing the bulk (coarse) delay and fractional (fine) delay. A frequency 40 MHz is used as sampling frequency and the beamformer has a enhanced the temporal resolution which is achieved by a 240 MHz poly phase filter, while we do some relaxing on the Analog-to-Digital converter (ADC) bandwidth requirement.

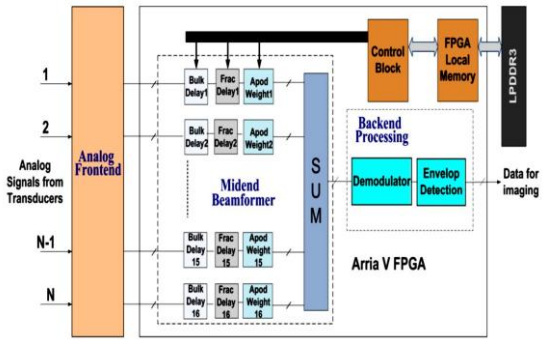

Figure.2. Architecture of Digital Beamformer Architecture

The proposed architecture for a 64-channel ultrasound beamformer is shown in Figure 2. The analog front end portion receives the analog signals and the converts it into digital, here we use 64 transducers to receive the echo signals. Here in this architecture each channel path can process a signal from the corresponding transducer and has the techniques to delay the signal. The Mid-End beamformer and Back-End processing are the essential parts of the Digital Signal Processing block in this architecture. Delaying the signals and the alignment of signals before it goes to the summer block is the responsibility of the Mid-End Block.

The summed signal is demodulated and envelope detection is performed. Control block of the architecture generates control signals by using locally pre-computed data, due to the limitation of the space, local memory is updated by each scan-line. We uses an external memory to store all the delay values. The Mid-end block contains 64 paths, the control blocks generates delays for each path, dynamically depending on the control signals. We have two delay blocks, Bulk Delay and Fractional Delay Blocks. The signals are delayed using these two blocks, sequentially.

In addition in each path we add an apodization weight also to the signal. Bulk delay block delays the signal by an integer multiple of sampling period. Fractional delay block is nothing but a poly phase filter, this block performs interpolation of data without up-sampling. The apodization block supplements the different weights to different channels as this block multiplies the coefficients with signals.

Bulk Delay

In the architecture Bulk part is implemented using technique of delaying the signals by an integer number which correspond to the sampling period. A FIFO buffer is used to implement this particular architecture. The bulk delay therefore has a buffered output signal if the desired duration in control is equal to the amount of signals stored in the FIFO buffer. We had implemented the FIFO Block using Simulink which we will call as a variable integer delay block. The total delay should be reduced by 1 to prevent updating of input signals in an attempt to maintain the sampled sample. The desired delays for all channels increase monotonously if we focus the points from near to far along a scan-line. The registers are required to reject the last repeated signals ensure the correctness of the functionality of the poly-phase filter. We also will introduce a new clock-gating scheme on the fractional delay part to ensure the correctness of the logic. The pipeline Enable signal will be pulled down to gate the clock, when the bulk delay is increased by 1. This will result in fractional delay will be stalled in one cycle to reject data input in the pipeline[2].

Fine Delay

The interpolation functionality through an economical poly-phase filter implementation, thereby preventive the necessity for up sampling through fractional delay. The poly- phase delay filter is meant supported the 48-tap low-pass filter that may be accustomed play the role of the interpolation low-pass filter, rather than victimization associate up-sampling and down-sampling methodology, the poly-phase filter are going to be accustomed directly access interpolated signals Fig. 3. Simulink Model for Bulk and Fractional Delay without ever-changing the sampling rate. this system has been enforced with seventh order finite impulse response (FIR) filter with six groups of coefficients. every of them represents a desired interpolating position. The cluster of coefficients is chosen by the management signals supported desired section. The registers store all seven previous sample signals. This calculation is beneath the idea that the desired resolution should be a minimum of λ/16 and therefore the most first harmonic is twelve Mc with a forty Mc frequency. Basically, the quantity of filter constant teams is calculated to satisfy the desired resolution as explicit in (1).

$$RFR = F_{max} * 16/F_s \quad (1)$$

RFR is the required resolution for the frequency, Fmax the max frequency and Fs the frequency of sampling. The amount of group n coefficients should meet the necessary resolution (2).

$$RF\ R <= 1/F_s * n \quad (2)$$

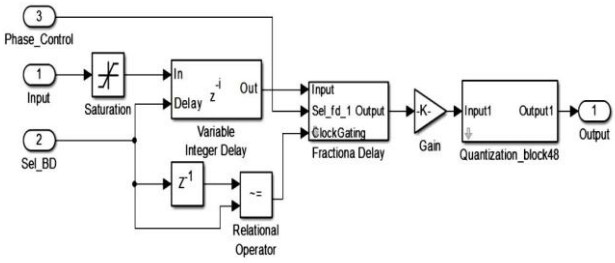

Figure.3. Simulink Model for Bulk and Fractional Delay

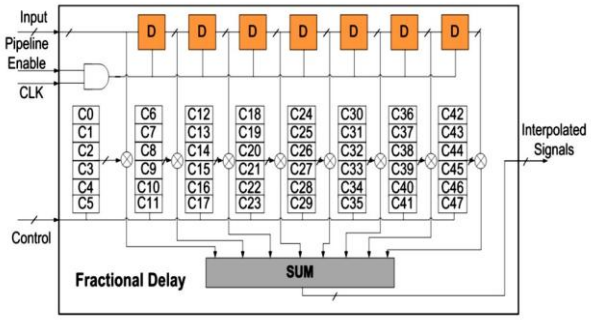

Figure.4. Block Diagram- Poly Phase Fractional Delay Filter

Memory

The suggested fresh system would only place the times for the current scan-line instead of old tradition method of storing all delays for a framework in local storage. Delays re-updated by the micro-controller to each scan line; all delays are in external DDR3 memory. A dual buffering system as shown in Fig 5 is used to enhance efficiency. The architecture needs two local memories, one for providing delay information and the other providing buffering information. The delta-coding scheme is used in the architecture to save the space which is required to save delay information. The memory for each channel is estimated as 41Kb, assuming a 64 2 scan line and 5200-sampling- point ultrasound mode, which when compared against the conventional method is 7.6 Mb .The conventional method uses a 7.6 Mega Bytes of Data , if we assume a 64x2 scanline and 5200 Sampling point ultrasound mode, but here we require only 41 Kilobytes of Data, hence the memory is saved hugely if we use this architecture.

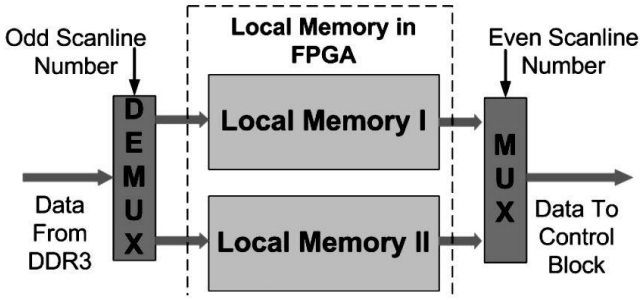

Figure.5 Architecture of Local Memory Management.

C. ULTRASOUND DIGITAL BEAMFORMER FOR HIGH-FREQUENCY LINEAR ARRAY TRANSDUCERS-A REAL- TIME ANALYSIS

This paper presents a digital beamformer for high frequency (20 MHz) which uses a linear ultrasonic arrays in real-time. Here, the system can handle up to 64-element linear array transducers and excite 16 channels and receive simultaneously at 100 MHz sampling frequency with 8-bit precision[4]. A Real-Ttime Digital Beamformer based on FPGA has been proposed. FPGA Architecture of the Real-Time Beamformer contains digitization, delaying, and summation of RF Signals. The Echoes from 16 adjacent transducer elements are digitized to do the beamforming in digital domain. Fine delays as small as 2 ns is implemented using Fractional Delay Filtering technique. This beamforming architecture gives a frame rate of 30 frames per second. Dynamic receive focusing and receive apodization are used in the architecture provides great flexibility for beamforming.

Architecture

Our architecture follow a strategy which combines coarse and fine delay structure. A programmable delay structure is used to implement the coarse delay, which is an integer multiple of the clock period. The fine delay structure is modeled using 4-tap FD FIR Filter. We has selected a Xilinx Virtex II Series FPGA Chip which supports 564 I/O's and 1584 KB of RAM. Figure. 6 shows the coarse delay structure implemented in the beamformer[4]. The sampling rate is determined by the time interval between two samples. Here we use the 100 MHz ADCs and the operating frequency is 100 MHz Delay coefficients are 4-bits each , out of which one bit will controls the condition of each multiplexer, the multiplexer decides whether delay has to added or not. As an example we will take 60 ns as the delay to be introduced, the corresponding 4-bit delay coefficient is '0110'. The first bit of the multiplexer is '0', which means data will not flow over the 8 clock delay unit. The total delay in the data path is 40 ns + 20 ns = 60 ns is hence calculated. All delays can be expressed by B4*8 + B3*4 + B2* 2 + B1* 1 for 16 clock cycles or less. We can extend the delay larger than 16 clock cycles by adding one more bits in the binary coefficient.

The structure of the fine delay of this architecture is depicted in Figure. 7. The fine delay from 2 ns to 8 ns are implemented using Digital Filter Structures which are distributed arithmetic FIR filters, which use full-parallel, fixed coefficient FIR Filters. An 8:1 bus multiplexer is used to select the fine delay according to the delay coefficient after the filter banks. The delay coefficients are pre-calculated and stored in the state machine for the fine delay and coarse delay.

Figure 8 describes a 8 channel dynamic receive focusing beamformer, delay values of 16 adjacent channels are shown in symmetry. Different focal depths has different receive delay values, which is dynamically calculated in this architecture. Real-Time calculation of the delay coefficients are very complex, so we store the delays in FPGA and are updated in time according to the depth of the echoes. A 10-bit counter triggers the transition between two states. Dynamic receive focusing can be implemented with integer multiples of 0.5 mm step as the structure demands re-configuration. The maximum depth for dynamic focusing is 8 mm as we use 16 states each of 0.5 mm step. The FD filters outputs are summed to obtain the Final beamformed data. The Hardware complexity of the 16 channel beamformer is very less compared to standard beamformers.

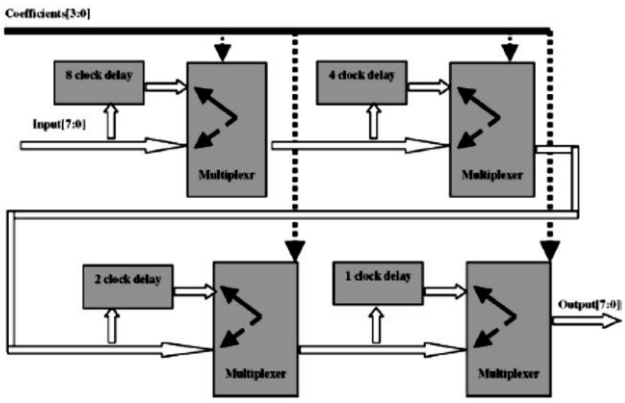

Figure.6 Coarse Delay Structure.

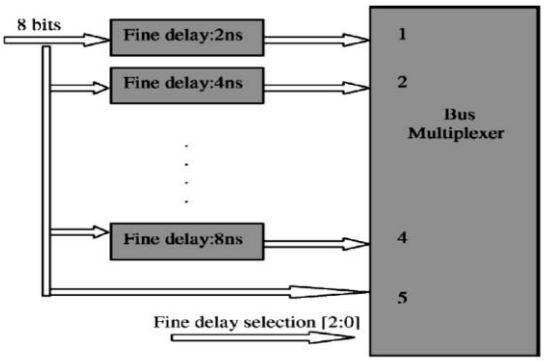

Figure.7 Fine Delay Structure.

III. DELAY PULSE CIRCUIT USED FOR BEAMFORMING

A delay pulse circuit can work with both digital receive beamforming for ultrasound phased array system and driving array transducers with a resolution of 1 ns is developed in this article.

To meet the resolution requirements this circuit can supply pulses of 1 ns resolution, through the Phase shifting technique of the Phase locked loop(PLL) built-in the FPGA Chips[5] .Six phase clocks with 1 ns phase difference are generated, which are used to drive channel counters which in turn generates delay pulses of each channels. Architecture of digital receive beamforming (1 ns delay resolution) is also presented based on this circuit. The phase shifting technique of PLL is utilized to generate six clocks with 6 ns periods and 1 ns phase difference. These six clocks are used to drive the A/D Converters according to the receive focal points, clocks are non-uniform sampling clocks.

A low cost FPGA is selected to implement this circuit. A. The results of the simulation and its comparison with standard circuits show that a considerable improvement is there in the performance. A uniform sampling clock is used to spilt the delay of the beamformer into an integer multiple and a fractional part of the sampling period, we implemented the integral part with a memory delay line and the fractional part can be realized by interpolation filtering.

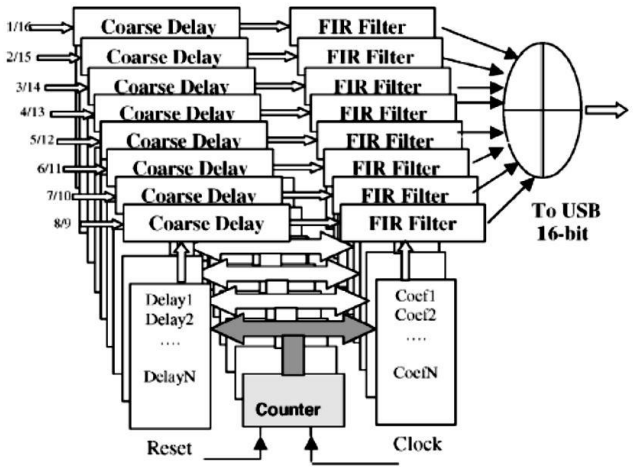

Figure.8 Fine Delay Block Diagram of Beamformer.

A. Realization of a Delay Pulse Circuit

We have to choose the FPGA for realization of the delay I. pulse circuit with great care. We need one which is having shortest delays of intrinsic gates and interconnection. FPGA should have appropriate granularity and functionality of the basic logic blocks[6]. It should have a PLL which is built in, which supports advanced clock shift capability to provide programmable phase shifting. The architecture is depicted in the Figure 9. The input to PLL is a clk-25MHz clock, the outputs are three clock signals with a period of 6 ns. They are clk-out [0] (with 0 degree phase shift), clk-out [1] (with 60 degree phase shift) and clk-out [2] (with 120 degree phase shift) respectively. Three clock signals are derived from these with a period of 6 ns by inverting each of them . The clocks are named as clk-out [3] (with 180 degree phase shift), clk-out [4] (with 240 degree phase shift) and clk-out [5] (with 300 degree phase shift) respectively. In order to achieve a 1ns time resolution, each of the six clock signals clk-out [0,. . . , 5] has a period of 6ns but separated by 1ns from each other. 1ns time resolution is obtained using PLL and inverters by using the above architecture.

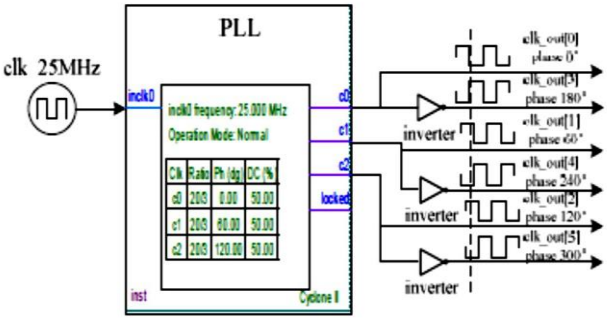

Figure.9 FPGA Delay Pulse Circuit with 1ns Resolution.

B. Transmit Beamforming- Delay Circuit

For the Transmition we need to generate trigger pulse with 1ns resolution. We use a combination of coarse and fine delay structure is adopted here. The coarse delay structure is accomplished by multiplying the signal with integer multiples of the clock periods[6]. A 16-bit counter is used to store the coarse delay. With the help of 6-to-1 clock multiplexer, we select from one of six shifted clocks and the fine delay is obtained. The appropriate clock for the counter is selected to obtain the 1ns resolution.

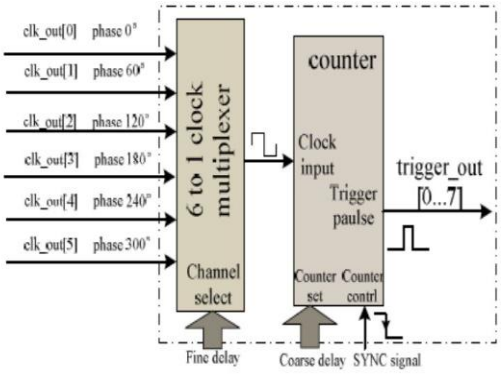

Figure.10 Transmit Delay Pulse Circuit.

Receive Beamforming- Delay Circuit

The receive beamforming architecture is shown as Figure 11. This design employs the phase shifting with the PLL to meet the resolution requirements, since PLL is built-in inside FPGA no extra logic is required for achieving this. The coarse and fine delays blocks are having the same architecture as transmit block. 1/4 frequency divider is used to derive the sample clock for our A/D converter. FIFO registers are used to store the Analog signals that are sampled by non-uniform sampling clocks, they are summed to produce the output signal.

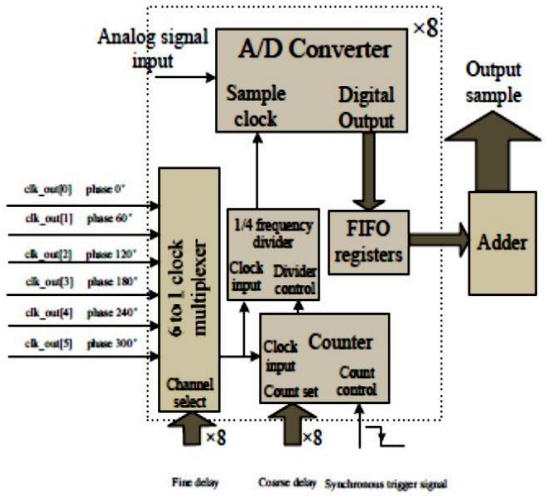

Figure.11 Logic Structure Implemented Receive Beamformer.

IV. COMPACT FPGA BEAMFORMER ARCHITECTURE

Delay and Sum Beamformer (DAS) beamformer architecture and implementation with non-uniform sampling is discussed in this paper. Front end electronics is the most fundamental block of the system in terms of area(size), power consumption and cost, so simplifying this block is of the prime importance. Hence Digital Beamforming based on the non-uniform sampling achieves sampling and focusing simultaneously, so this goal of simplifying the front-end electronics is hence achieved. FPGAs are used to implement the compact architecture, FPGAs contains the clock generators, memories, buffers, adders etc. The digital beamformer has been tested on Altera Quartus EDA Synthesis and Implementation Tool and Stratix Devices are used to implement the same.

Architecture

The Beamformer architecture is depicted in Figure 12. Here, a Pipelined Sampled-Delay Focusing (PSDF) scheme is implemented[7]. Every channel has three blocks which performs the basic functions

- Time Gain Control Amplifier (TGC)
- 8 bit converter (ADC)
- FIFO memory

In this scheme we need to focus only on the samples where focus of the beam is required. A non-uniform sampling is used with different sampling clocks at each element to achieve this. Sampling and delaying has to be done simultaneously in order to perform this operation, this a main change from the conventional beamformers which performs these operations separately. PSDF Architecture's sampling rate is determined by the distance between imaging points, it can also be defined as the minimum sampling rate for the envelope detection of our focused signal.

For an ultrasonic transducer with a bandwidth equal to its central frequency, there is a dramatic reduction in hardware requirements compared with the conventional uniform sampling methods. PSDF scheme's minimum sampling frequency can be 9 MHz or 3 MHz, when fo = 3 MHz

The structural complexity of the beamformer is further reduced as we uses the FIFO memories which will eliminates the operations for addressing the sampled signals . The FPGA implementation of an efficient dynamic focusing system based on the PSDF scheme is proposed, which has proved to be efficient from both the hardware and signal processing point of view. Memory used in the scheme is the best possible when compared against all the beamforming schemes. Sampling rate and the depth of investigation is the main factor contributing to the FIFO memory size. For example , a depth of 30cm and the sampling rate is 30 MHz estimated FIFO Size is 12000. The most critical block of this system is the non-uniform sampling clock generator(SCG).

The sampling clock generator (SCG) can be realized using a simple circuit using an iterative "in the circuit" calculating for the delay information. An algorithm called mid-point algorithm is used to implement the sampling clock generator. Mid-point algorithm is used to generate sampling clock for each channel and simplify the evaluation of delay values in real time.

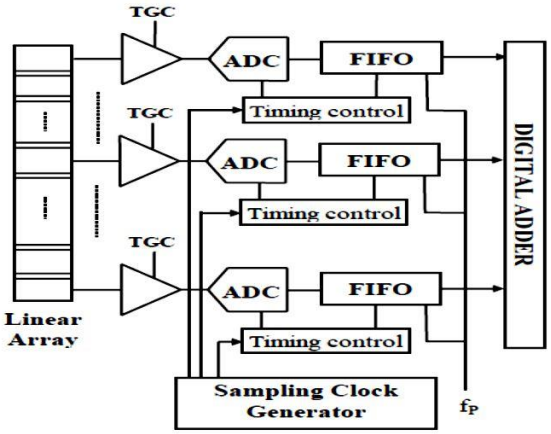

Figure.12 Compact FPGA Beamformer Architecture.

This particular algorithm will provides us an important reduction in hardware when compared against standard methods of beamforming. Elimination of the addressing operation for sampled signals as we use FIFO memories, further reduces the structural complexity of the beamformer.

V. AN HYBRID BEAMFORMER(HBF)

Here we propose an analog-digital hybrid single chip receive beamformer .The 2-Dimensional transducer has a large number of transducer arrays (72 128 array=9216), so we cannot use digital beamforming because a large number of ADCs are required and wiring inside probe becomes non realizable. Analog beamforming is the solution for this, we need to perform analog beamforming at least for the front end electronics stage of the 2D transducer.

Here we use a Capacitive micromachined ultrasonic transducers (CMUT) as the transducers where the energy transduction is due to change in capacitance. we can easily construct 2D and 3D transducer arrays using these transducers as they are micromachined. It can also provide higher frequency of operation because of small size. An analog-digital-hybrid architecture will achieve the wide dynamic range of delay time and small chip-area with a non-uniform sampling scheme. The architecture of RX beamformer has Eight analog beamformers (ABF) followed by a single Digital Beamformer (DBF), which is shown in Figure 13. Analog Beamformer does the focusing operation for the adjacent 8 channels to generate an analog output signal. These Eight analog output signals from the Eight beamformers are applied as inputs to the DBF. The DBF converts the Eight analog input signals into the Eight digital signals, and then performs the focusing operation on the 8 digital signals to generate a digital output signal for every focal point.

The Hybrid Beamformer (HBF), by utilizing an uniform ABF sampling system and an area efficient digital storage (FIFO) in the DBF, will reduce the area in the device. In comparison with the uniform sample ABF, this job suggests an area reduction of around 84.

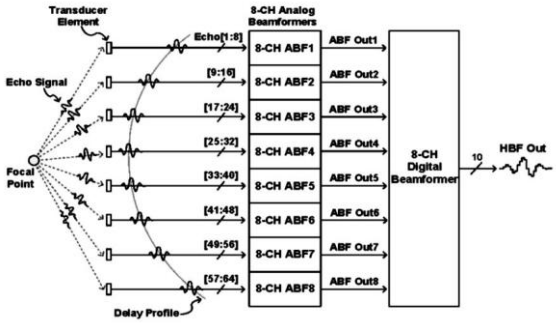

Figure.13 Single Chip Hybrid Beamformer with 64 channels.

VI. MULTI-CHANNEL BEAMFORMER

A highly compact medical ultrasound beamformer architecture is proposed in this paper. All known novel principles has been used to form this architecture, which has created a simple and low power circuitry[8].

The proposed architecture is shown in Figure 14[8]. Every transducer element emits an RF signal s(t) on which time gain compensation is performed using a variable gain amplifier. The signal s(t) is converted to digital signal q[n] in the DSM block, which is then passed to circular buffer. We then multiply the signal with apodization coefficient ie weights of that channel and then summed accordingly from all channels. The summed output is then filtered to get in-phase and the quadrature components sI[n] and sQ[n] respectively.

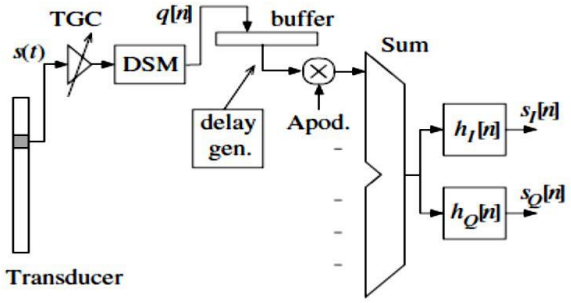

Figure.14 Multi-Channel Beamformer

VII.CONCLUSION

Medical ultrasound is a diagnostic imaging technique based on the application of ultrasound. Beamformer is the brain of the ultrasound scanner which is used for the directional transmission and reception of the signal. The evolution of beamforming architectures from analog to digital environment and various beamformer designs and architectures in order to be compatible to high frequency probes and yield improved imaging performance, resource optimization, etc. were discussed in this paper.

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