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Mathematical Modeling and Simulation of Junction less Dual Material Double Gate MOSFET with Various Work Functions

S. Darwin, T.S. Arun Samuel, E. Muthu Kumaran, J. Deny

Abstract*: *In view of the 2-Dimensional game plan of Poisson's condition, a material science-based model of Double Gate Dual Material Junction less (DGDMJNL) Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is made. The advantages of different work capacities connected to the metals in DMDGJNL MOSFET are exhibited and the potential at the inside and qualities of the electric field is uncovered. The proposed model exhibits explicitly demonstrates the effect of the work in electrostatic potential and electric field. It is exhibited that the execution of DMDGJNL MOSFET can be changed by adjusting the channel length extents of control door and shield entryway. The model is assessed by its figured results and those got from a 3D TCAD test system for numerical outcomes.

Keywords: **Junction less dual material gate, Poisson's equation, electric field, central potential, work functions**

I. INTRODUCTION

In nano scale Integrated Circuits (ICs) Junction less metal oxide transistor assumes a predominant job in view of its electrical attributes and its basic handling instruments with intersection-based metal oxide semiconductors. In these gadgets the entire substrate is of same doping, because of this the arrangement of P-N intersection is jumped out [1]. The subthershold properties can be improved by utilizing changes entryway types, for example, front and base door, all around doors, trigate and triple doors [2-4]. This diverse structure offers better authority over the door and the scientists demonstrate an unmistakable fascination for Junction less Double Gate MOSFET [5-7].

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***** Correspondence Author
S.Darwin*, Assistant Professor, Department of ECE, Dr. Sivanthi Aditanar College of Engineering, Tiruchendur, Tamilnadu, India, darwin.me11@gmail.com
Dr.T.S.Arun Samuel, Associate Professor, Department of ECE, National Engineering College, Kovilpatti, Tamilnadu, India, arunsamuel2002@gmail.com
Dr.E.Muthu Kumaran, Assistant Professor, Department of ECE, Dr.B.R.Ambedkar Institute of Technology, Port Blair, Andaman & Nicobar Islands, India, reachemk@gmail.com
Dr. J. Deny, Associate Professor, Department of ECE, Kalasalingam Academy of Research and Education, Tamilnadu, India, Prof.j.deny@gmail.com

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Regardless, junction less gadget depends upon the mass technique for conduction, the huge doping center in the silicon channel diminishes bearer transportability, achieving the corruption in the effectiveness of transporter transport.

Furthermore, Drain Induced Barrier Lowering (DIBL), because of short channel sway, turns out to be increasingly genuine with the contracting of the silicon channel length [8-9]. To overcome these issues, an entryway with double material (DMG) structure has been acquainted and associated with improve the execution of junction less MOSFET. Starting late, a novel structure called Dual material with front and base entryways (DMDGJNL) MOSFET has been proposed, and its electrical qualities have been investigated with the assistance of (3D) recreations for numerical results. What's more, poly-Si entryways have been superseded by the metal doors when the gadget estimation has been scaled down to nanometer. The displacing with metal entryways is an immediate consequence of the effect of poly-Si door exhaustion with high-k entryway dielectrics and Vth fluctuations of slender body gadgets.

In this paper, the metal entryway work towards the gadget execution has been inquired about and the reproduced yields were plotted for different metal work capacity esteems. In spite of the fact that, the presentation can be assessed for dielectrics with high k esteems as entryway oxide material. The work basically considers the focal potential favorable circumstances offered by the DMDG JNL MOSFET by using the estimate of illustrative methods. The investigative model is made using two-dimensional course of action of Poisson condition. The models that had been fused into these reenactments were Auger recombination and Shockley-Read-Hall recombination models. This paper is sorted as: Section II exhibits a deduction model of this work. Area III holds the outcomes and exchange and segment IV contains finishes of this work.

II. MODEL DERIVATION

The DMDGJNL MOSFET and its directions is appeared in figure1. The entryways with various kind of metals M1 and M2 called the control door and Shield entryway. The source side metal work (M1) is lower than the channel side entryway metal (M2). The length L1 and L2 speak to the length of the entryway close to source side (M1) and shield door close to deplete area (M2).

Dismissing the effect of the charges which is fixed in the oxide district on the electrostatics of the channel, the channel is believed to be totally depleted in the system of subthreshold. The whole utilization charge is totally overwhelmed by the door with this presumption.

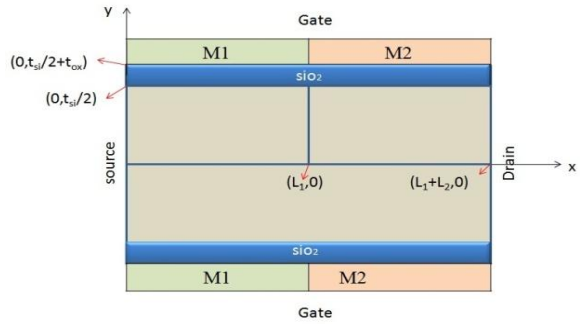

Fig. 1 Schematic view of DMDGJNL-MOSFET

A. Central Potential

The 2D Poisson's equation of DMDGJNL MOSFET is

$$\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2}=\frac{qN_d}{\varepsilon_{si}} \tag{1}$$

Where q is the electronic charge, N_d is the donor concentration of the semiconductor, ε_{si} is the permittivity of the silicon body respectively.

The 2D channel potential using a parabolic potential method [15] can be expressed as

$$\varphi(x,y)=A_1x+A_2(x)y+A_3(x)y^2 \tag{2}$$

The electrostatic potential under metal gate M1 and M2 with different work functions are

$$\varphi_1(x,y)=A_{11}(x)+A_{21}(x)y+A_{31}(x)y^2;\ \ 0\le x\le L_1 \tag{3}$$

$$\varphi_2(x,y)=A_{12}(x)+A_{22}(x)y+A_{32}(x)y^2;\ \ L_1\le x\le L_1+L_2 \tag{4}$$

The channel boundary conditions are

(i) The symmetry nature of the potential in the silicon channel along y direction, the field (electric) at y=0 must be zero under the gate M1.

$$\frac{\partial\varphi_1(x,y)}{\partial y}|_{y=0}=0; \tag{5}$$

(ii) Under gate M1, the junction point between top/bottom gate oxide and channel electric flux is continuous

$$\frac{\partial\varphi_1(x,y)}{\partial y}|_{y=\frac{tsi}{2}}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\varphi_{sp1}(x)-(V_{gs}-V_{fb1})}{t_{ox}} \tag{6}$$

(iii) The central potential $\varphi_{cen1}(x)$ is the function of

$$\varphi_{cen1}(x)=\varphi_1(x,0) \tag{7}$$

Where t_{si} is the silicon film thickness, tox is the gate oxide thickness, ε_{ox} is the relative permittivity of silicon dioxide, $\varphi_{sp1}(x)$ is the surface potential of silicon channel.

$$\varphi_{sp1}(x)=\varphi_1(x,y)|_{y=\frac{tsi}{2}}=A_{11}(x)+A_{21}(x)\frac{t_{si}}{2}+A_{31}(x)\frac{t_{si}^2}{4} \tag{8}$$

Under metal gate M1, the channel flat band voltage is denoted byV_{fb1},

$$V_{fb1}=\varphi_{ms1}=\varphi_{m1}-\varphi_{silicon} \tag{9}$$

$$\varphi_{silicon}=\chi+\frac{E_g}{2}-V_t.\log(\frac{N_d}{n_i}) \tag{10}$$

Where χ is the electron affinity, φ_{m1} is the metal gate M1 work function, $\varphi_{silicon}$ is the work function of silicon, silicon band gap E_g, n_i is the intrinsic concentration of carriers and V_t is the Voltage due to temperature (thermal).

The values of $A_{11}(x), A_{21}(x)$and$A_{31}(x)$ are obtained from the boundary conditions (5) – (7) in equation (3).

$$A_{11}(x)=\varphi_{cen1}(x) \tag{11}$$

$$A_{21}(x)=0 \tag{12}$$

$$A_{31}(x)=-\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\varphi_{sp1}(x)-(V_{gs}-V_{fb1})}{t_{ox}} \tag{13}$$

The 2D channel potential

$$\varphi_1(x,y)=\varphi_{cen1}(x)-\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}}\frac{\varphi_{sp1}(x)-(V_{gs}-V_{fb1})}{t_{ox}}.y^2 \tag{14}$$

$$\varphi_{sp1}(x)=\frac{4\varphi_{cen1}(x)\varepsilon_{si}t_{ox}+t_{si}\varepsilon_{ox}(V_{gs}-V_{fb1})}{4\varepsilon_{si}t_{ox}+t_{si}\varepsilon_{ox}} \tag{15}$$

Substituting the equations (14) & (15) in equation (1)

The semi 2D scaling equation for JL DMDG MOSFET

$$\frac{\partial^2\varphi_{cen1}(x)}{\partial x^2}-\frac{1}{\lambda^2}(\varphi_{cen1}(x)-\varphi_{c1})=0 \tag{16}$$

Where λ is the scale length and under the metal gate M1, φ_{c1} is the long channel potential for centre.

$$\frac{1}{\lambda^2}=\frac{8\varepsilon_{ox}}{4t_{si}\varepsilon_{si}t_{ox}+\varepsilon_{ox}t_{si}^2} \tag{17}$$

$$\varphi_{c1}=V_{gs}-\omega_1 \tag{18}$$

$$\omega_1=V_{fb1}+\frac{qN_dt_{si}t_{ox}}{2\varepsilon_{ox}}+\frac{qN_dt_{si}^2}{8\varepsilon_{si}} \tag{19}$$

By differential condition equation (2)

$$\varphi(x,y=0)=\varphi_{cen1}(x)=i_1e^{\frac{1}{\lambda}x}+j_1e^{-\frac{1}{\lambda}x}+\psi_{c1};\ 0\le x\le L_1 \tag{20}$$

$$\varphi(x,y=0)=\varphi_{cen1}(x)=i_2e^{\frac{1}{\lambda}x}+j_2e^{-\frac{1}{\lambda}x}+\psi_{c2};\ L_1\le x\le L_1+L_2 \tag{21}$$

From the following boundary conditions the values of i_1, j_1, i_2, j_2 are found out.

1. Zero electrostatic potential at source end

$$\varphi_{cen1}(x=0)=0 \tag{22}$$

2. At the junction of two dissimilar gate material the potential is in the form of continuous nature

$$\varphi_{cen1}(x=L_1)=\varphi_{cen2}(x=L_1) \tag{23}$$

3. At the junction of two different material gates the electric flux is continuous

$$\frac{d\varphi_{c1}(x)}{dx}|_{x=L_1}=\frac{d\varphi_{cen2}(x)}{dx}|_{x=L_1} \tag{24}$$

4. At the drain end Vds the potential is

$$\varphi_{2c}(x)|_{x=L_1+L_2}=V_{ds} \tag{25}$$

The coefficients of i_1, j_1, i_2, j_2 can be expressed as

$$i_1=\frac{e^{-\frac{L}{\lambda}}\varphi_{cen1}+V_{ds}-\varphi_{cen2}+(\varphi_{cen2}-\varphi_{cen1})\cosh(\frac{L_2}{\lambda})}{2\sinh(\frac{L}{\lambda})} \tag{26}$$

$$i2=\frac{e^{-\frac{L}{\lambda}}\varphi_{cen1ds}-\varphi_{cen2}(\varphi_{cen2}-\varphi_{cen1})\cosh(\frac{L_2}{\lambda})e^{-\frac{L}{\lambda}}}{2\sinh(\frac{L}{\lambda})} \tag{27}$$

$$j_1 = \frac{e^{-\frac{L}{\lambda}}\varphi_{cen1} - V_{ds} + \varphi_{cen2} - (\varphi_{cen2} - \varphi_{cen1})\cosh(\frac{L_2}{\lambda})}{2\sinh(\frac{L}{\lambda})} \quad (28)$$

$$j_2 = \frac{e^{-\frac{L}{\lambda}}\varphi_{cen1} - V_{ds} + \varphi_{cen2} - (\varphi_{cen2} - \varphi_{cen1})\cosh(\frac{L_2}{\lambda})e^{\frac{L}{\lambda}}}{2\sinh(\frac{L}{\lambda})} \quad (29)$$

B. Electric Field

If we differentiate the central potential the required electric field distribution for the device is obtained. The electric field can be expressed as

$$E_{cen1}(x) = -\frac{d\varphi_{cen1}(x)}{dx} = -\frac{1}{\lambda}(i_1 e^{\frac{1}{\lambda}x} - j_1(e^{-\frac{1}{\lambda}x}); 0 \le x \le L_1 \quad (30)$$

$$E_{cen2}(x) = -\frac{d\varphi_{cen2}(x)}{dx} = -\frac{1}{\lambda}(i_2 e^{\frac{1}{\lambda}x} - j_2(e^{-\frac{1}{\lambda}x}); L_1 \le x \le L_1 + L_2 \quad (31)$$

III. RESULTS AND DISCUSSIONS

To check the exactness of the scientific model, 2D device simulations have been performed by TCAD Sentaurus tool. The DMDGJNL MOSFET analytical model has been evaluated with software simulation results.

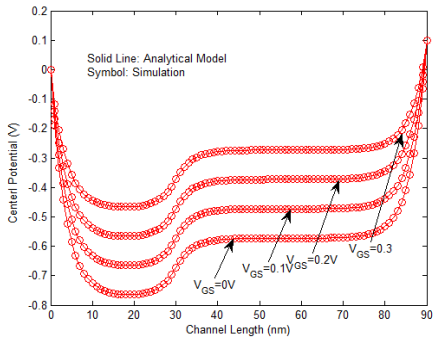

Fig.2 Potential profiles of DMDGJNL MOSFET of channel length L_1=30nm and L_2=60nm with different gate voltages.

The Figure 2. Demonstrate the central potential profile for various gate voltages for DMDGJNL MOSFET with various length ratios of gate (L_1:L_2=1:2). In the figure 2 there is a step central potential for JL DMDG MOSFET with high work function for metal M1 the minimum channel central potential occurs beneath M1 and there are no such variation in case of electrostatic potential under the material (M2) for a drain side bias. In view of the fact that, top gate material (M2) with less work function value, prevents the variation arise due to drain voltage caused by (DIBL) and reduce SCE's.

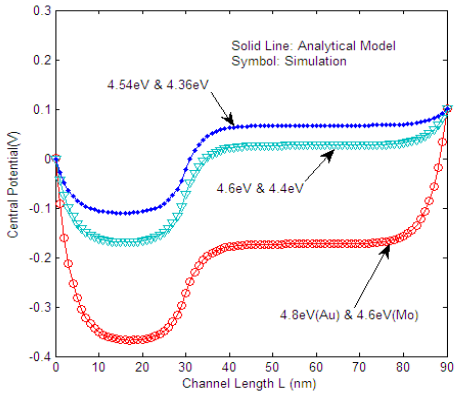

Fig. 3 potential for various metal work functions of M1 and M2

Figure 3 depict the calculated electrostatic potential of various metal work function values for φ_{m1},φ_{m2}. It is evident from the figure that junctionless transistors are faster to achieve the full depletion comparable to that of junction transistors at the same work function.

Figure 4 represents the changes in the lateral field (electric) distribution of DMDGJNL MOSFET of channel length ratio 2:1 for different metal work function values. The electric field is present on the device at any drain voltage

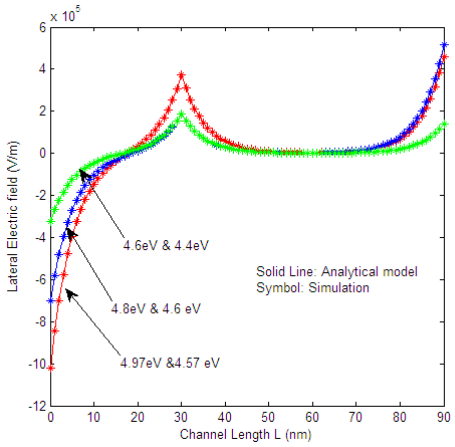

Fig.4 Electric field characteristics of DMDGJNL-MOSFET for channel length L1=30nm and L2=60nm with different metal work functions

Figure 5 plotted the central electric field for various drain voltages V_{ds}. The DMG structure having metal M2 (low work function) can adequately preclude the base focal potential from being dragged by expanding channel varies 0.1 V to 0.6 V. Subsequently, the potential below M2 is prepared to ingest the electric field initiated by the change in drain bias and attainably control the DIBL.

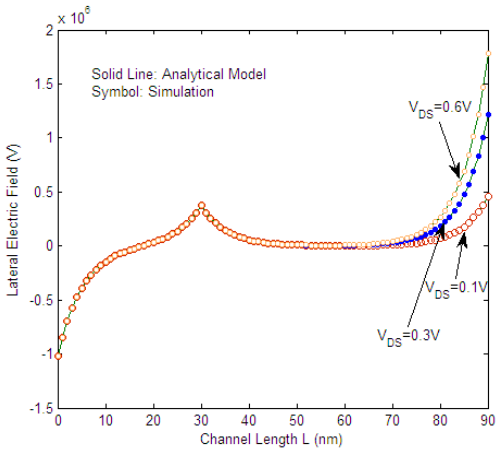

Fig.5 Electric field characteristics of DMDGJNL MOSFET with different V_{DS} voltages

IV. CONCLUSION

In this paper we evaluated the DMDGJNL MOSFET structure based on analytical and simulation results. The analytical model depends on 2D- Poisson's condition solved using a parabolic approximation.

The investigative articulations of central potential and electric field (lateral) are inferred. Further, different metal gate work function combinations have been proposed to evaluate the electrostatic potential and electric field of JLDMDG MOSFET. We noted that the metal gates reduced the short channel effects also perfectly work with high-k gate dielectrics compared to poly-Si gate.

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AUTHORS PROFILE

Darwin S received B.E degree in Electronics and Communication Engineering from Anna University (2007) and M.E degree in VLSI Design from Anna University, India (2011). He is currently working towards the Ph.D degree under Anna University with semiconductor device modeling as the area of specialization. His research interest includes modeling and simulation of multigate junction less transistors file which contains their education details, their publications, research work, membership, achievements, with photo that will be maximum 200-400 words.

T.S. Arun Samuel received his Bachelors of Engineering degree from the department of Electronics and Communication from Madurai Kamaraj University, Madurai, India and Master's Degree in Computer and Communication from Anna University, Chennai in 2004 and 2006 respectively. He has obtained his Ph.D degree in nanoelectronics at Anna University, India. From 2006 to 2011, he worked as a lecturer in Francis Xavier Engineering College, Tirunelveli, Tamilnadu, India. Currently he is a Associate Professor in National Engineering College, Kovilpatti, India. He has published more than 25 research papers as sole author in the field of device modeling and simulation. His research interests include Multi gate transistors and Tunnel Field effect Transistors.

Dr. E. Muthu Kumaran, received his Bachelors, Masters and Ph.D Degrees in Electronics and Communication Engineering from from Anna University, Chennai in 2005, 2008 and 2015 respectively. He is having more than 14 years of teaching and research experience worked in various engineering colleges and universities. Currently he is an Assistant Professor in Dr. B.R. Ambedkar Institute of Technology, Port Blair, Andaman and Nicobar Islands, India. He has undertaken various funded major research projects and published more than 10 research papers in International and national journals. His research interests include Medical Electronics, Bio Inspired Algorithms, IoT, Instrumentation and VLSI. profile which contains their education details, their publications, research work, membership, achievements, with photo that will be maximum 200-400 words.

Dr. J. Deny received the B.E. degree in electronics and communication engineering from Anna University, in 2010, the M.Tech. degree in digital communication and networks from the Kalasalingam Academy of Research and Education, in 2012, and the Ph.D. degree in image processing and network security from the Bharath Institute of Higher Education and Research, in 2017. He is currently an IEDC Coordinator/Associate Professor with the Department of ECE, Kalasalingam Academy of Research and Education. He has published more than 50 research papers in various international conferences/international journals indexed in Scopus, SCI, and Web of Science. His research interests include image processing, network security, and innovation techniques in entrepreneurship. He was a member of IAENG, IACSIT, SDIWC, IAEME, CSTA, ACM, ISEEE, and IAAM. He has been serving as an Editorial and Reviewer Board Member of more than 30 reputed journals.