International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-8 Issue-12, October 2019

Methods for Increasing the Radiation Resistance of 3D Integration Memory Modules for Aerospace Applications

R. S. Litvinenko, I.V. Prokofiev, V.M. Matveev

Abstract*: Space radiation effects in electronics are significantly important during the development of devices for aerospace applications. Radiation tolerant component base significantly lag behind the commercial chips with regard to operating speed, memory capacity and etc. The issue of commercial memory use in information storage devices is especially acute in conditions of high radiation. Within the framework on development of micromodule 3D integration technology for onboard equipment for aerospace applications, the study of the radiation effects influence on the operation of commercial NAND-Flash chips and methods of counteracting these effects are carried out.

Keywords*: 3D integration, heavy charged particles, micromodule, radiation tolerant memory.

I. INTRODUCTION

Ensuring radiation resistance is one of the main challenges facing the aerospace industry. Consequently, the problem of reliable assessment of durability at the design stage of the spacecraft is a problem of paramount importance. A significant decrease in the production of radiation-resistant component base and a reduction in the number of manufacturers of such products on the market led to the use of commercial quality electronic components in spacecraft. The main reason for this is economic: the price of commercial products is 10-100 times lower than radiation-resistant ones.

Currently, the design of a miniature storage device for commercial applications is not a difficult task. Over the past decade, the density of flash memory has increased by 10 times and exceeded this parameter in hard drives. However, in conditions of increased radiation exposure, the use of commercial memory without the use of protection measures becomes impossible. The problem is that the life cycle of commercial chips is 2 to 3 years, while the cycle of radiation-resistant components can be 15 years or more [1].

Revised Manuscript Received on October 30, 2019.
***** Correspondence Author
R.S. Litvinenko*, Science Manufacturing Complex "Technological centre", Moscow, Zelenograd, Russia.
I.V. Prokofiev, Science Manufacturing Complex "Technological centre", Moscow, Zelenograd, Russia.
V.M. Matveev, Science Manufacturing Complex "Technological centre", Moscow, Zelenograd, Russia.

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC-BY-NC-ND license http://creativecommons.org/licenses/by-nc-nd/4.0/

Thus, the final product for aerospace applications is obviously outdated and imposes significant limitations on the capabilities of on-Board equipment. In addition to low speed and high energy consumption, the use of radiation-resistant components increases the size of the equipment, which is critical for objects placed into orbit. Therefore, the issue of the possibility of using commercial memory for space applications is an relevant task.

II. LITERATURE REVIEW

Effects of ionizing radiation from outer space on spacecraft, including galactic space rays, solar cosmic rays and electron-proton irradiation of natural radiation belts of the Earth, puts the task of developing ways to reduce the degradation of electrical parameters of the electronic component base.

The occurrence of a parasitic thyristor in chips based on CMOS structures is due to latching under the influence of the passage of fast heavy charged particles (HCP), forming ionized (conductive) channels in the structure. Certain external factors, in particular exposure to HCP, can lead to the formation and fixation of this thyristor in the open state under the action of the supply voltage, which causes a rapid increase in current consumption, followed by thermal destruction of the chip. Failure of electronic digital devices are preceded by an avalanche increase in current through HCP exposed element. A significant increase in current occurs in the first 10 ms after contact with charged particle. If the device is de-energized at this point, the avalanche process can be depressed. Most often after short-term power-off element is workable and a potential catastrophic failure becomes a single failure. In order to avoid a long break in the work duration of power interruption must be commensurate with the possible duration of the avalanche-like process and the charges life time.

Non-volatile memory devices that can be used in the high radiation space environment space are confined to relatively small EEPROM devices. These devices are manufactured according to specialized radiation hardened process technologies. These special process technologies are expensive and are typically a few generations behind commercial processes. Moreover, the resultant radiation hardened memory cell area is larger than the cell area of a commercial memory. As a result, the memory capacity of these hardened devices is limited to a few Mb. Existing high density commercial flash memories cannot be used in space applications because of their low radiation tolerance.

Even as process technology scaling for commercial flash memories improve total ionizing dose (TID) and single event latchup (SEL) tolerance, the same process changes generally increase device susceptibility to single event upsets (SEUs) and single event functional interrupts (SEFIs) [2].

TID effects can be dealed by shielding the device. Shielding allows to absorb the main part of the particles with low energy. The layer of 2 mm aluminium reduces the accumulated dose of space radiation 100 times, but to reduce the dose 100 times more, it will be necessary to use the protection with a thickness of 8 mm. This paradox is easily explained by the fact that the composition of space rays is non-uniform. When low-energy particles are hold in a thin screen, high-energy particles can easily penetrate it. Moreover, high-energy particles are able to knock particles out of the screen material, thereby creating secondary radiation.

One of the most effective methods against SEU effects is modular redundancy. It is implemented by duplication of elements. When a SEU is occurred the true value of the information bit is chosen by voting. As a rule this method allows to avoid most SEUs in data storage but increases the dimensions of the device and reduces the operating speed.

III. METHODS

3D integration technology developed in the SMC "Technological centre" allows using memory of any type. Thus, the technology allows not only to reduce the area of the module, but also to combine various elements, as well as methods of protection against radiation without significant money and time costs.

The developed technology is based on splitting the structure of the device into separate elements (technological substrates) for their assembly into a stack and subsequent sealing compound to ensure the mechanical strength of the micromodule. The main idea of the technology is to create inter-stack switching (interconnections between technological substrates) on the side surface of the micromodule by coating the micromodule with a conductive metal and then forming a topological pattern [3,4].

Memory module block-scheme is shown on figure 1.

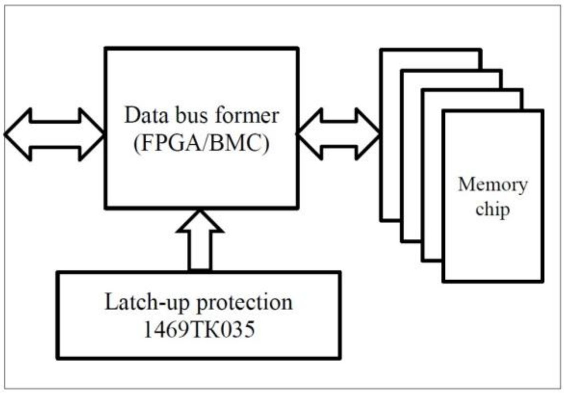


Figure 1 – Memory micromodule block-scheme

The module uses the following methods to counteract radiation:

- *latch-up protection* (implemented by 1469TK035 chip, developed by SMC “Technological centre”);
- *radiation resistant chip for data bus former* (developed on base matrix crystal technology by SMC “Technological centre”);
- *modular redundancy* (4 NAND Flash chips with high radiation resistance [5] are used);
- *radiation-resistant compound* for extra shielding;
- *correcting codes* (can be implemented using the controller of the module or using the external device [6]).

The module breadboard is shown on figure 2.

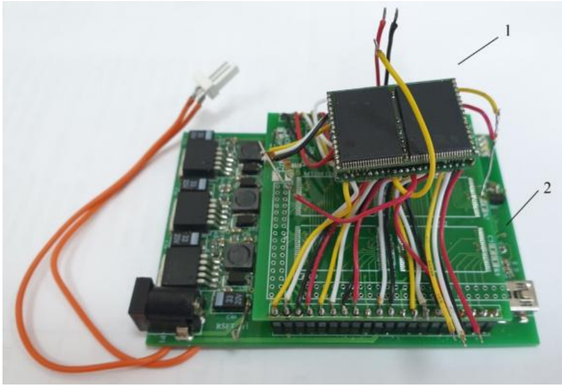


Figure 2 – Memory module breadboard during electrical testing

1 – Memory module; 2 – Measuring tooling

The memory module is implemented as microassembly with two stacks (levels) – memory stack and control stack. The micromodule dimensions are 16x23x10 mm. The supply voltage is 3.3V, capacity 128Gb, reading time 25 ns.

IV. CONCLUSIONS

The article presents the most topical questions of the memory micromodule development for use in the onboard equipment for aerospace applications. The use of commercial memory in high radiation environment is possible under certain conditions. First of all the memory chip is supposed to originally have a significant radiation tolerance. In this case the use of latch-up protection chip, modular redundancy, shielding and error-correcting codes can allow the device functioning in high radiation environment. The research showed that the most typical cause of catastrophic failures of microelectronic devices in high radiation environment is the latch-up (thyristor) effect. The short-term power off is the most effective method to deal with the thyristor effect. It is planned to deepen the research towards radiation tolerant compounds.

ACKNOWLEDGMENT

The work is carried out with the financial support of the Ministry of Education and Science of Russia under Agreement no. 14.574.21.0155 (unique identifier of applied research RFMEFI57417X0155). The work was carried out using the equipment of CCU “Functional testing and diagnostics of micro - and nanosystem technique" on the basis of SMC "Technological centre".

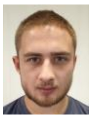
REFERENCES

1. S. Pollesky, V. Zhdanov, M. Artuhova Ensuring The Radiation Resistance Of Spacecraft In The Design // Components and Technologies. Vol. 9. 2010. P. 93-98.
2. Nikbil Gupta ; Bert Vermeire ; Hugh Barnaby Design of a 1 Gb Radiation Hardened NAND flash memory // Non-Volatile Memory Technology Symposium. Albuquerque, NM, USA. 10-13 Nov. 2007.
3. R.S. Litvinenko, I.V. Prokofiev Development of the information storage micromodule for spacecrafts with latch-up effect protection // International journal of engineering and technology. 7 (4.7) (2018) 184-187.
4. K. Kondo, R. Akolkar, D. P. Barkey, W.-P.Dow, M. Hayase, M. Koyanagi, S. Mathad, P. Ramm, F. Roozeboom, S. Shingubara Processing Materials of 3D Interconnects, Damascene, and Electronics Packaging 6 // The Electrochemical Society. Vol. 64. No. 40.
5. B. Vandevelde ; N. Chatry ; N. Sukhaseum Impact of multiple write cycles on the radiation sensitivity of NAND flash memory devices // 2016 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS). 19-23 Sept. 2016
6. Matveev V. M., Litvinenko R. S. The Error-Correcting Coding In Information Storage Modules With Increased Radiation Resistance // International journal of engineering and technology. 7 (4.7) (2018) 180-183.

AUTHORS PROFILE

R.S. Litvinenko, engineer-constructor in Science Manufacturing Complex "Technological centre", Moscow, Zelenograd since 2012. He has 7+ years of industry experience. He has got Master's Degree in Moscow Institute of Electronic Technology. He has published more than 20 papers in International and National journals. His area of Interest is pressure and tactile sensing, microassemblies and 3D integration technologies.

I.V. Prokofiev, senior research scientist in Science Manufacturing Complex "Technological centre", Moscow, Zelenograd since 1995. He has 35+ years of industry experience. He has got Master's Degree in Moscow Institute of Electronic Technology. He has published more than 50 papers in International and National journals. His area of Interest is gas sensing, transceivers, microassemblies and 3D integration technologies.



V.M. Matveev engineer in Science Manufacturing Complex "Technological centre", Moscow, Zelenograd since 2017. He has 2+ years of industry experience. He has got Master's Degree in Moscow Institute of Electronic Technology. He has published more than 10 papers in International and National journals. His area of Interest is magnetic sensing, microassemblies and 3D integration technologies.