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A High Speed Latched Circuit for Flash ADC

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Abstract*: Practically all electronic systems are realized using integrated circuit(IC) chips. The IC design requires digital signals, but however the physical signals available routinely are either continuous time varying signals or corrupted discrete voltages. These continuous time varying input signals are converted to full voltage swing digital signals by means of a comparator circuit. The comparators use regenerative feedback to transform the output to a full scale digital signal. The core specifications considered in this comparator implementation are power dissipation (P_D), propagation delay (t_P), output offset voltage and slew rate. The circuit is simulated in CMOS 180nm technology using Tanner EDA tool. The high speed latched comparator circuit is powered with a 1.8V DC power supply and the obtained results show that it operates at 1.67GHz, slew rate is 126 V/µS and the dynamic power dissipation is found to be 0.328mW.

Keywords: Cross-coupled, DC power, latch, Propagation delay, Slew rate, and transistor sizing.

I. INTRODUCTION

The need for continual improvements in functional speed and little power consumption of ultra-high speed serial links such as ultra wideband receiver have attracted many researchers to work in the area of gigahertz speed and medium resolution level data converter circuits. Analog to Digital Converter (ADC) circuits are found nearly in all electronic systems such as high-speed line receiver circuits, clock and data signal restoration circuit, threshold voltage detection circuits, peak voltage detectors, zero-crossing detector circuits, high speed instrumentation, logic level shifting circuits, frequency translation circuits, satellite broadband communication systems, various oscilloscopes and X-band radar system. The key specifications to be considered in the design and implementation of these systems comprise such as high operating seeds, longer battery operating time, low power, high resolution, less noise generation and reduced silicon area.

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In order to implement wireless portable systems with such specifications, the design of an ADC circuit is very much crucial and very much indispensable. In general, ADC circuits are needed to transform the time-varying input analog voltages into a binary data bit sequences. Various architectures such as Flash type, Two-Step flash, Sub-ranging type, Pipelined, Sigma-Delta (Σ-Δ) type, Folding type, Dual slope type, Successive approximation register type and Time-interleaved are available in the collected works to perform analog to digital conversion. Flash converter circuits extremely fast and are well appropriate for large bandwidth applications. But the disadvantage is that they operate at high power. The important component in flash converter is the comparator circuit which draws appreciable current during bit conversion and occupies mores chip area. For instance, if the resolution of the flash architecture increases, then it directly affects the size of the chip, and circuit complexity. Also as the chip size increases, problems related to signal and clock routing becomes noticeable.

Basically a CMOS analog comparator is a circuit used to match two signals and generates which of the input voltages are greater. A comparator circuit in its simplest form comprises of a conventional MOS transistor differential pair with a NMOSFET or PMOSFET current mirror circuit as an active-load, an amplifier stage implemented using common source (CS) configuration and one or more CMOS inverter circuits connected at the output side, which work as an additional amplification stage. The performance of a CMOS comparator circuit can be improved by proper scaling of the dimensions of MOS transistors. Nevertheless, the scaling procedure of CMOS transistors are not implemented directly, as it necessitates high channel doping, gate induced drain leakage and band to band tunneling across the junction. Reducing the aspect ratio of the MOS transistor leads to lowering of several important specifications of the comparing circuit. Also it results in the increased values of offset voltage and major changes in the (1/f) noise levels. One of technique to reduce power consumption of a CMOS transistor circuit is to use V_{DD} voltage reduction technique. In a CMOS realization, the power expression is directly proportional to $(V_{DD})^2$. Conversely, dropping the power supply voltage (V_{DD}) will severely enhance the delay time. Also to compensate for the lowering in power supply voltages (V_{DD}), aspect ratio of MOS transistors are further improved and this would source increased currents in the circuit and large occupied circuit area. The important specifications to be considered in the design this CMOS comparator circuit are input voltage range, resolution, conversion rate, circuit area and power consumption. Sometimes a comparator circuit is also called as a one-bit ADC.

Different type of comparator circuit architectures exist such as Pre-amplifier based latched comparator (i.e. open loop comparator circuit combined with dynamic regenerative latch), Open loop comparators (i.e. operational amplifiers without compensation) and finally fully dynamic latched comparator circuits. The regenerative type of comparator circuits utilizes positive feedback mechanism, similar to the bi-stable circuits such as flip-flops or sense amplifiers, for comparison between two voltages. Sometimes a combination of regenerative comparator circuit and open-loop comparator circuits are used to achieve better important characteristics such as ultra speed signal comparison. In this work, a dynamic latched comparator circuit is designed and simulated using Tanner EDA tools in CMOS 180nm technology.

The selection of comparator architecture is based on the type of analog to digital converter architecture. Figure 1, shows the block schematic of a general latch type comparator circuit. It contains three stages specifically the input pre-amplification stage, a positive feedback amplifier stage or the decision stage and finally an output buffer stage circuit. The preamplifier stage basically consists of a NMOS differential circuit pair with PMOS active load. The size of the input MOS differential transistor pair is chosen in accordance with the transconductance (g_m) and input resistance of the MOS differential pair. The gain of the preamplifier stage can be improved further by resizing the widths of PMOS transistors at the output side. The following stage is a decision circuit and it should be able to discriminate very low amplitude signals of the range (μV to few mV). By introducing hysteresis in the circuit, the circuit is capable to discriminate noisy outputs. Also regenerative feedback is employed in decision circuit which is accomplished by cross coupling of two NMOS transistors. The last connected stage is an output buffer circuit or post-amplifier circuit. This stage is employed to produce an output logic signal (either high or low). The output stage should take a differential signal at its input and should not suffer from slew rate limitations.

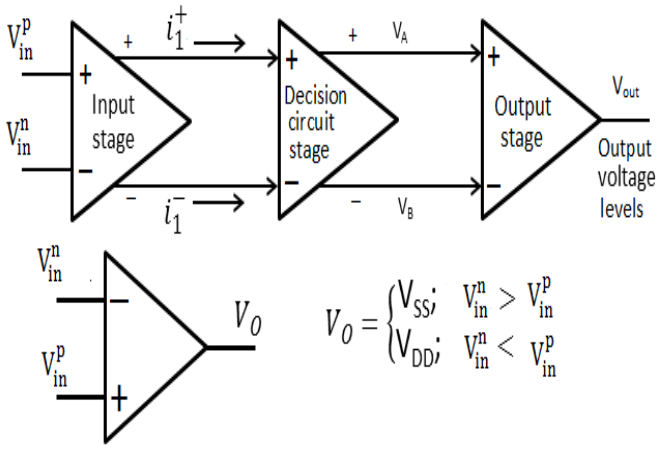

Fig. 1. Comparator block diagram and symbol

S. B. Mashhadi *et al.* described about the analysis of dynamic comparators using analytical expressions and explored its various trades-offs with respect to low power dissipation as well as faster operation at small supply voltages [1]. V.Savani *et al.* presented a novel design of dynamic latched comparing that can exhibit high-speed operation, consumes less-power fits in a smaller chip area. The technique is based on a new shared charge logic based reset method [2]. The design of a high speed differential clocked comparator employing bandwidth variation method is employed by Y.Okinawa *et al.* [3]. A comparator based on differential configuration is analyzed and simulated for use in a successive approximation register (SAR) type ADC is presented in [4]. P. M. Figueiredo *et al.* proposed two kick-back noise lowering techniques for CMOS latch comparator circuits and implemented the same in 180nm technology and the results have been validated [5]. A high speed comparator for use in a four bit pipelined converter to be implemented on an I-UWB receiver is given in [6]. It uses a comparator sharing technique. L. Kouhalvandi *et al.* described an offset voltage cancellation technique in comparator circuits, which resulted in reduced kick-back noise [7]. The design procedure and simulation of multistage preamplifiers for use in high speed comparators is explained by W.Shirai *et al.* [8]. A high speed comparator design for use in a 10-bit pipelined ADC is given in [9]. In this proposed work an high speed latched comparator is designed and simulated.

This paper is written as follows: Section-I gives the introduction about the importance of comparator circuit, the working design of comparator is accessible in section-II and Section-III presents the circuit simulation values of various parameters observed from the designed comparator circuit. Lastly Section -IV concludes the overall paper.

II. LATCHED COMPARATOR SCHEMATIC

A comparator circuit is mostly used for translating analog voltages to output digital signals. In a Flash ADC, the comparator circuit at the input side is the power hungry component and most area consuming component [10]. So the design and analysis of comparator circuit is the most critical module in the final implementation of a Flash ADC, as the circuit functioning speed and the resolution levels of the Flash ADC circuit is strongly dependent on the CMOS comparator circuit [11]. The starting or the input stage is used to enhance the differential input signal to a suitable voltage level and also to achieve the overall high voltage gain of the circuit. This is accomplished by the diode connected active loads at the drain side of input differential transistors $\mathbf{M_{in}^+}$ and $\mathbf{M_{in}^-}$. The input signals $\mathbf{V_{in}^p}$ and $\mathbf{V_{in}^n}$ are converted into corresponding output currents at output stage of first stage and designated as $\mathbf{i_1^+}$ and $\mathbf{i_1^-}$. These currents drive the decision circuitry (M_5, M_7, M_9 and M_{10}). The decision circuit utilizes positive feedback and is a bi-stable cross coupled circuit. This stage essentially is capable of discriminating signals as low as (5-8) mV. Let's assume that a differential signal is applied at the input transistors, so this forces an unbalanced current to flow in two differential branches at the output side of first stage.

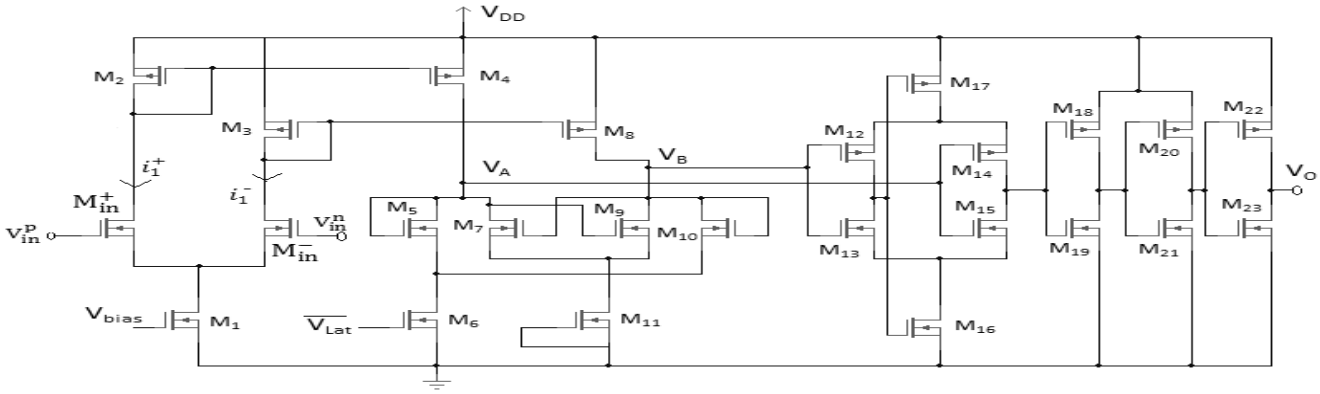

Fig. 2. Schematic diagram of latched comparator

Now suppose if latch voltage (V_{lat}) is made logic low, then the transistor M_6 is turned ON and the diode connected transistors M_5 and M_{10} will be made to conduct and a finite voltage appears at the drain terminals of M_5, M_7, M_9 and M_{10}. Further assume that the current flowing into the drain of M_9 and M_{10} increases by a small margin, then the voltage V_B becomes greater than V_A. Since the gate of M_7 is connected to node B, then the transistor M_7 takes current from M_5, further decreasing the voltage V_A, that drives the gate of transistor M_9. In this way the voltage difference V_{BA} keeps increasing more at a rapid rate. From this it can be said that a slight variation in the voltage levels at the input side can result in a high voltage at the drain terminals of the transistor. The circuit stage following the decision stage is used to translate the output voltage into binary logic signal and this stage should not suffer from slew rate limitations. The fully complementary self-biased CMOS differential amplifier (CSDA) is used. It is realized using two conventional CMOS amplifiers. The current mirror loads from both the amplifiers are deleted and interconnecting both the gate and drain terminals together. In CSDA connection, the transistors M_{16} and M_{17} operate in triode region. The voltages at the drain of M_{14} and M_{19} are designed very near to the operating supply voltage V_{DD}. The output voltage swing is dependent on these two voltages. Lastly to provide more voltage gain and make the comparator more accurate, simple inverter circuits are connected in cascade at the output side.

III. SIMULATION RESULTS

In this proposed work, high speed comparator circuit design is simulated in CMOS 180nm technology using Tanner EDA tool. The offset voltage (V_{io}) is measured by shorting together the input terminals of the circuit and computing the voltage available at the output side of the comparator circuit. The simulated offset response is displayed in figure 3. In this circuit, 0.4V was taken as the reference voltage. So the voltage above reference voltage is taken as logic high and the voltage below the reference voltage is taken as logic low. The simulated transient response of high speed latched comparator is shown in figure 4. The circuit is powered with a dc voltage of 1.8V. The parameters such as rise time, fall time, propagation delay, operating speed, power consumption and slew rate were measured using transient analysis. The static power dissipation (P_{stat}) of the comparator circuit is calculated mathematically by the product of bias currents in the circuit and the power supply voltage V_{DD}. The calculation of dynamic power dissipation (P_{dyn}) is based on the currents flowing through the transistors, when they are switched between on and off states and vice-versa.

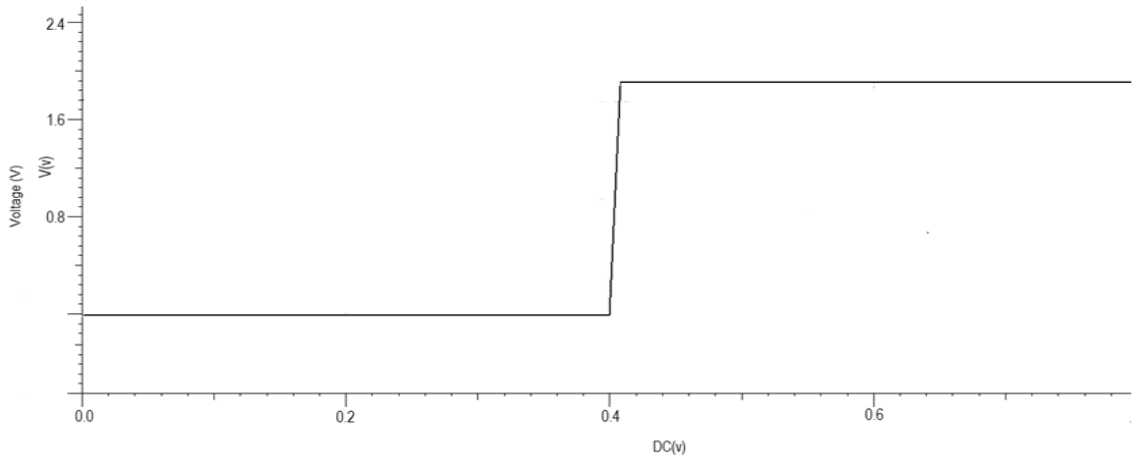

Fig. 3. Offset voltage response

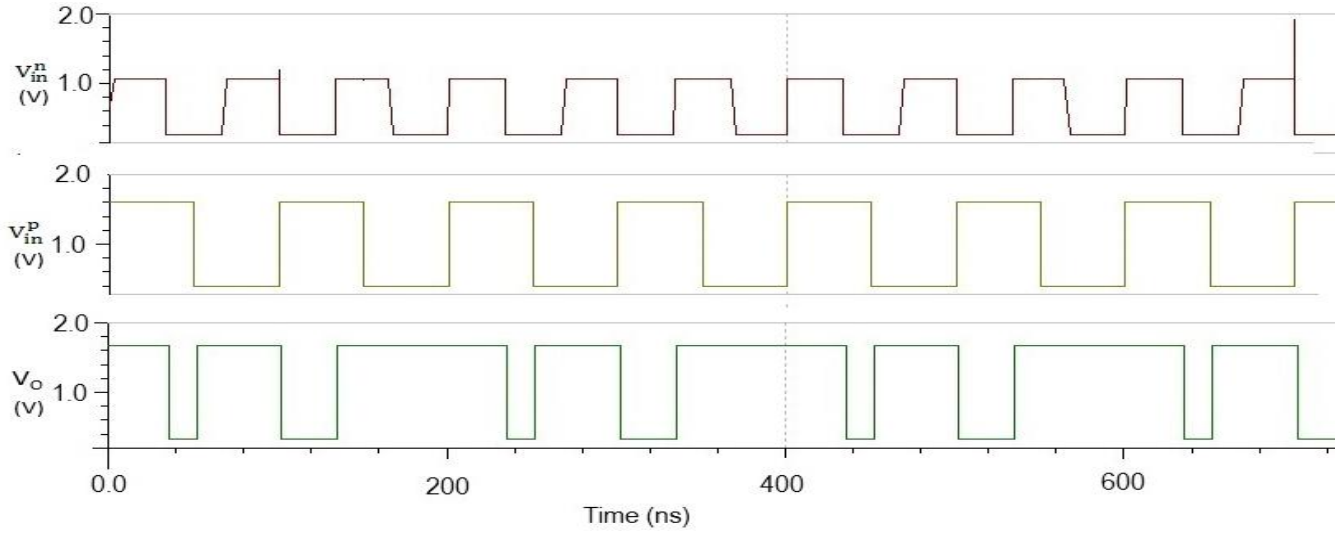

Fig.4. Transient analysis response

The power dissipation is measured as 0.328mW. The rise time (t_r) is calculated to be (0.628-0.142) ns=0.486ns, whereas fall time (t_f) is calculated to be (2.846-2.138) ns= 0.408 ns. The propagation delay of the circuit is calculated as the average of the two values i.e. (0.486+0.708)/2=0.597ns. The operating speed is calculated to be 1.67 GHz. The power-delay product is calculated to be 195.81fJ while the slew rate is calculated as 126 V/µS.

IV. CONCLUSION

A novel latch comparator utilizing regenerative feedback is proposed in this paper. The circuit arrangement proposed in this paper exhibits high speed, moderate power dissipation and low offset voltage as demanded by flash analog to digital converters. Use of auto-zeroing techniques, decreases the offset voltage and power consumption has also been reduced. The simulation of the latch comparator circuit was carried out in 180nm technology using Tanner EDA tool with a 1.8V power supply and the obtained results show that it operates at 1.67GHz and the dynamic power dissipation is found to be 0.328mW. The offset voltage is measured to be 246µV. Still further the latched comparator circuit is made to operate at higher frequencies by altering the aspect ratio of transistors.

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