

For the switch power both the charging and discharging occurs for dissipation. We have number of capacitors in CMOS circuits. In CMOS transistor we have both and interconnect capacitances which are called as parasitic capacitances. When the circuit is normally operating normally the power is observed by capacitors which are in number present in CMOS transistor so, they can charge and discharge accordingly. This power consumption by parasitic capacitances tends to dissipation of power which we call as the switching power dissipation. There are two types of networks we have in CMOS transistor they are P-MOS and N-MOS and the networks we use are pull-up Network which is made of pMOS and pull-down network which is made of nMOS. As given in fig.3&4

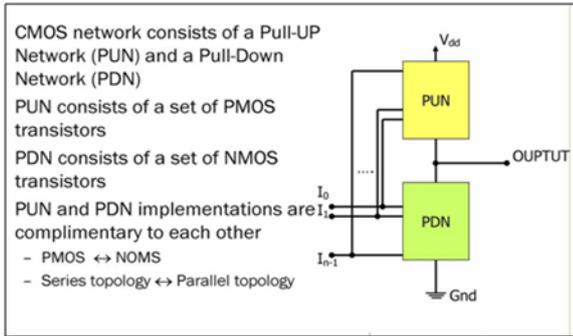


Figure 3: P-MOS and N-MOS Networks

We have millions of nodes of capacitive circuits then we call it as complex CMOS circuit, we have dissipation of power even when apply switching then nodes are charged and discharged. By the PMOS device of P- channel pull up network the capacitors of nodes are charged, similarly discharge is through N-MOS transistors n-channel devices in the pull-down network [2]. We express the dissipation of power is as shown in equation below.

$$P_{dyn} = \alpha C_L V_{DD}^2 f$$

Here power consumption is denoted as P, active factor is denoted as α , capacitance switched load is C, we have frequency of clock representation as f and V as the voltage supply. In our system the clock has activity factor as $\alpha = 1$, because for every duty cycle it rises and falls. 0.5 is the active factor value of the data probably. In the load of right dissipation of power Dynamic can be effectively computed when at the nodes capacitance of the right load is estimated by considering in the activity factors [2].

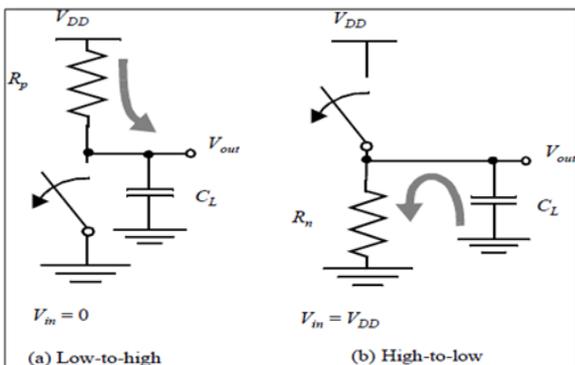


Figure 4: inverter of CMOS

Power dissipation of short circuit is known which also known as dynamic dissipation of power was a Second type. We have open circuit when we on the path of PMOS

network when in CMOS circuit the output is 1. While we open the path of NMOS network when we have zero output. The in other hand the network path of pMOS is closed [4]. In short we can say that there is no path directly from supply to ground. As given in figure 5. It an inverter which has simple circuit; the NMOS is on when we have 1 in the input, PMOS is on when we have zero input but we don't have path between low and high inputs normally between the supply voltage to ground. No path should be present for short circuit. When there is a slow change in input from 0 to 1 then through the transistor short circuit flows. We have a passing current in transistor which is an short circuit current if we have a change in input slowly from low to high or else 1 to 0 then definitely a region is there in between where both transistors are on.

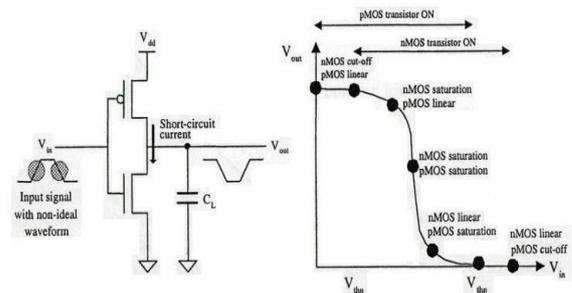


Figure 5: CMOS inverter short-circuit current

If voltage of input is much more than voltage of threshold of transistor NMOS type and similarly smaller than the V_{DD} threshold voltage minus the PMOS transistor type threshold voltage, so, both the transistor types will be on for that input time and then had a path of short circuit for that time of the input both the transistors will be on, and as a consequence there is a short circuit path from supply to ground [5]. And it's called as dissipation of power in short circuit. because of direct current path as shown in figure below characteristics as the formula elaborates the dissipation power of short-circuit excluding the load output in an invert designed of CMOS, here gain factor is β , the time of inverter fall or rise is given as τ and signal period of input is T.

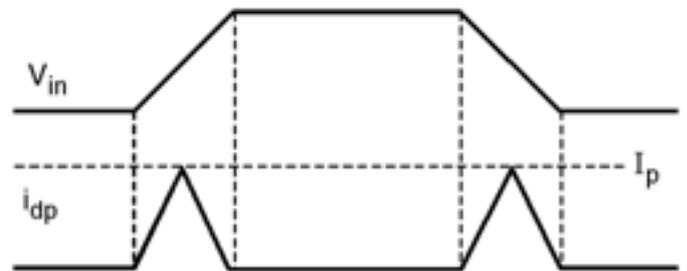


Figure 6: characteristics of voltage and current

We have frequency dependence very strongly and also we have dependence on rise and fall time. We definitely have 20% dissipation power of short circuit which resulted due to slow time of rise on nodes significantly for loaded inverters. Keeping fast edges in all is a good practice when we consider the dissipation of power.

If we assume that we have very high capacitance of load as an first case as shown in figure below, in that case we have a large significant fall time of output which is greater than the rise time of input. So, we get Zero value maximum for current of short circuit. Now as shown in figure below the case of reverse operation is, where we have capacitance of output very small, and we have very less time of fall in output than input rise time. PMOS transistor device drain to source voltage is equals to V_{DD} for most periods of the transition, so the short circuit current is maximum. By doing the fall and rise time of output higher than counter part of input which tends to the minimum dissipation of short circuit leaded by this analysis which has concluded [3].

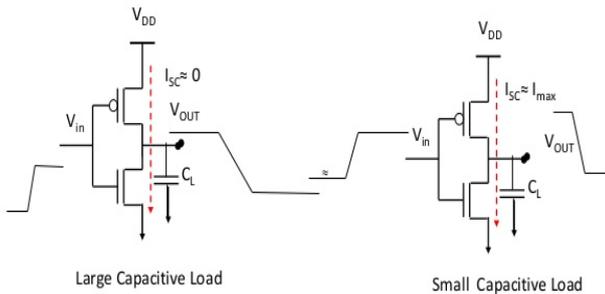


Figure 7: short circuit capacitance load

Or else if we increase the time of fall or rise in the output that can cause currents short circuit by slowing down the circuit as given in waveform in below figure.8..

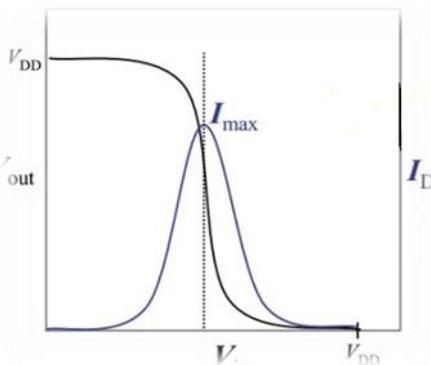


Figure 8: CMOS inverter short-circuit

We also call the power of standby is essentially known as Leakage power dissipation. Dissipation of power is the result of voltage supply connection of the circuit as there is no change in input that tends to dissipation of power. It's very important due to its leakage current. Its an typical transistor of MOS type where the leakage current is mentioned as I1 to I5 contribution diagram on fig.9.

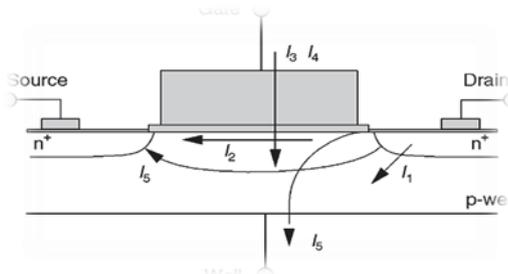


Figure 9: current due to leakage contribution

As shown in figure the Complementary MOS is a combination of NMOS and PMOS. We can form substrate of P and N type by the n-Well and p-type substrate combination. So, it is considered as a diode. There will be some reverse current in bias because the diode is reversed. By using the equation we can calculate the static consumption of power.

$$P_s = V_{CC} \times I_{CC}$$

Where: V_{CC} = supply voltage, I_{CC} = current into a device
Based on the temperature our leakage current is present, depending on density of current saturation which is reverse and device area which is active. We have to carefully consider all the transistors present in the chip. In today's IC's we use to have millions –trillions of transistors.

III. RESULTS

When we sum currents which all passes through it. The current is of 0.1 microns for more than 1 million transistors. This current will become thousand times when we use 1 billion transistors, which is quite heavy and that can't be ignored. If there is less number of transistors then we can ignore, but if the chip contains maximum number of transistors then diodes reverse bias current will quite heavy. when the threshold voltage V_T increases the channel gets activated and when channel gets increased pinch-off condition occurs due to the reverse leakage current the power dissipation occurs. The simulation results for power consumption with temperature dependent carriers are as shown in figure.10 below.

IV. CONCLUSIONS

We need a balance in efficiency of power and performance which is the aim of Electronic design. In this paper tried to connect and represent various IC's with number of low-power designs of general purpose to relate different solutions. Now a day's basic need is to have low power consumption devices and less power dissipation also in every system. So, we have parallelization and pipelining techniques for reduction of power. For achieving our goals its very important to have methodology of Low-power. Cost will definitely reduce if we can reduce the dissipation of power in accordance to cooling and packing reduction so, system performance will be improved overall.

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